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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908jl3ecpe

List of Chapters

Chapter 5
System Integration Module (SIM)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA)	Read:	0	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:				Unaffected by reset				
$0001	Port B Data Register (PTB)	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:				Unaffected by reset				
$0002	Unimplemented	Read:								
		Write:								
$0003	Port D Data Register (PTD)	Read:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
		Write:								
		Reset:				Unaffected by reset				
$0004	Data Direction Register A (DDRA)	Read:	0	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB)	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006	Unimplemented	Read:								
		Write:								
$0007	Data Direction Register D (DDRD)	Read:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0008 ↓ $0009	Unimplemented	Read:								
		Write:								
$000A	Port D Control Register (PDCR)	Read:	0	0	0	0	SLOWD7	SLOWD6	PTDPU7	PTDPU6
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000B ↓ $000C	Unimplemented	Read:								
		Write:								
$000D	Port A Input Pull-up Enable Register (PTAPUE)	Read:	PTA6EN	PTAPUE6	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000E ↓ $0019	Unimplemented	Read:								
		Write:								

☐ = Unimplemented   R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 4)

Z — Zero Flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of $00.

1 = Zero result
0 = Non-zero result

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7
0 = No carry out of bit 7

4.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

4.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

4.5.1 Wait Mode

The WAIT instruction:
- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

4.5.2 Stop Mode

The STOP instruction:
- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

4.6 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:
- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC:$FFFD or with $FEFC:$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.
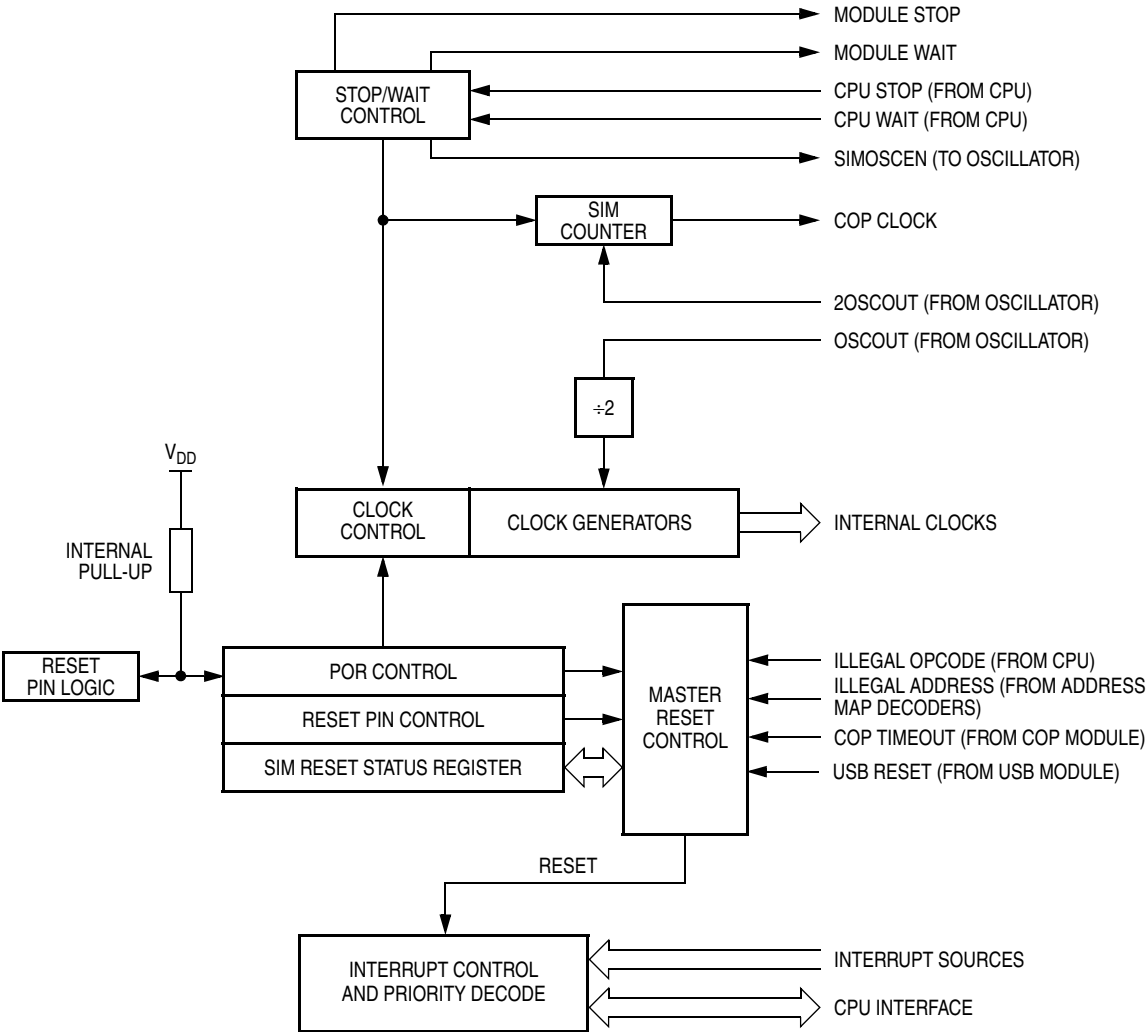
Figure 5-1. SIM Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE00	Break Status Register (BSR)	Read:	R	R	R	R	R	R	SBSW	R
		Write:							NOTE	
		Reset:	0	0	0	0	0	0	0	0

Note: Writing a 0 clears SBSW.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE01	Reset Status Register (RSR)	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
$FE02	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
$FE03	Break Flag Control Register (BFCR)	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							

☐ = Unimplemented ☐ R ☐ = Reserved

Figure 5-2. SIM I/O Register Summary

Table 5-3. Interrupt Sources

Priority	Source	Flag	MASK[1]	INT Register Flag	Vector Address
Highest	Reset	—	—	—	$FFFE–$FFFF
	SWI Instruction	—	—	—	$FFFC–$FFFD
	IRQ Pin	IRQF	IMASK	IF1	$FFFA–$FFFB
	Timer Channel 0 Interrupt	CH0F	CH0IE	IF3	$FFF6–$FFF7
	Timer Channel 1 Interrupt	CH1F	CH1IE	IF4	$FFF4–$FFF5
	Timer Overflow Interrupt	TOF	TOIE	IF5	$FFF2–$FFF3
	Keyboard Interrupt	KEYF	IMASKK	IF14	$FFE0–$FFE1
Lowest	ADC Conversion Complete Interrupt	COCO	AIEN	IF15	$FFDE–$FFDF

1. The I bit in the condition code register is a global mask for all interrupts sources except the SWI instruction.

5.5.2.1 Interrupt Status Register 1

Address: $FE04

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	IF5	IF4	IF3	0	IF1	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R	= Reserved

Figure 5-12. Interrupt Status Register 1 (INT1)

IF1, IF3 to IF5 — Interrupt Flags
These flags indicate the presence of interrupt requests from the sources shown in Table 5-3.
1 = Interrupt request present
0 = No interrupt request present

Bit 0, 1, 3 and 7 — Always read 0

5.5.2.2 Interrupt Status Register 2

Address: $FE05

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IF14	0	0	0	0	0	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R	= Reserved

Figure 5-13. Interrupt Status Register 2 (INT2)

8.4 Functional Description

Figure 8-1 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The two TIM channels are programmable independently as input capture or output compare channels.
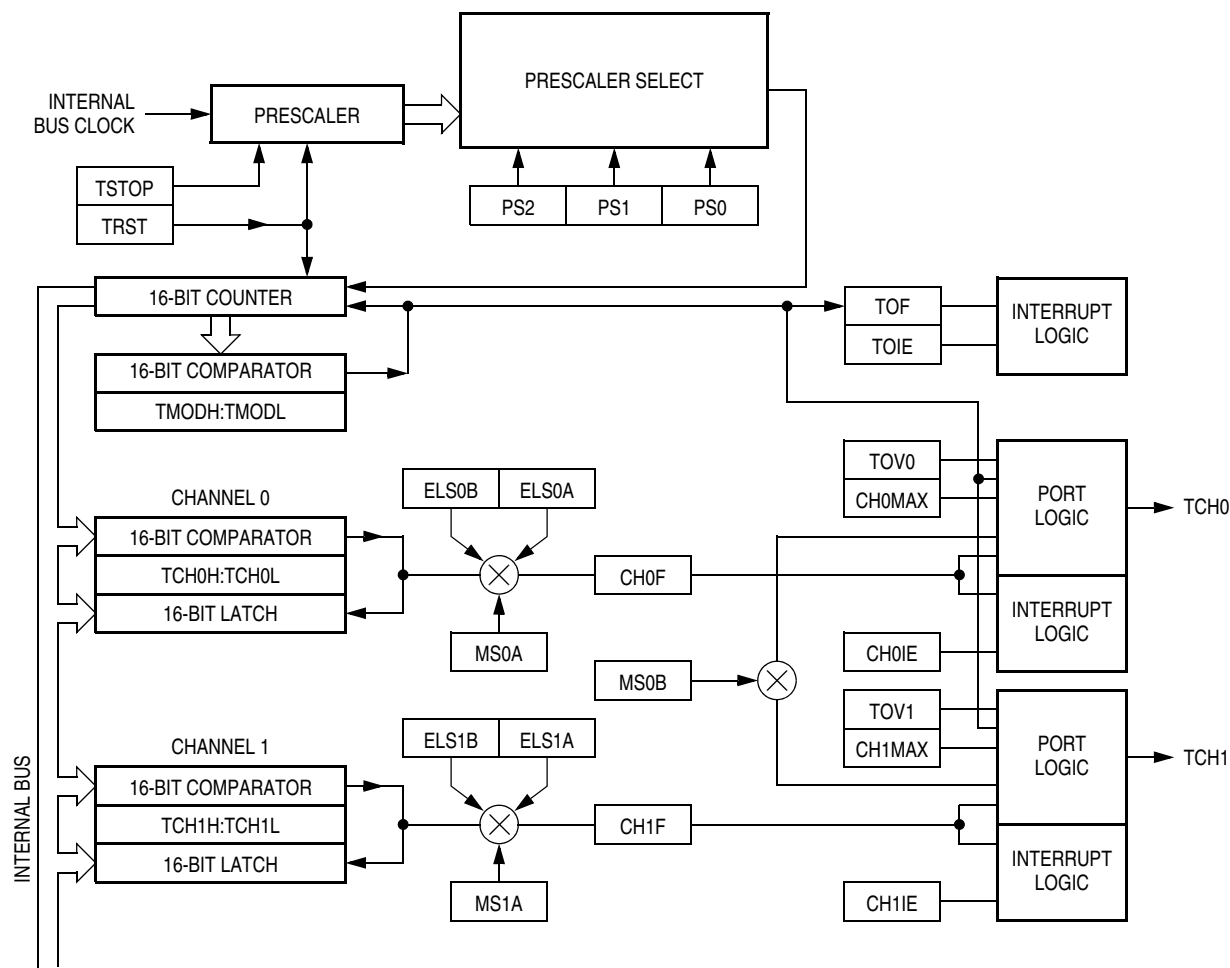

Figure 8-1. TIM Block Diagram

8.4.4.3 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use the following initialization procedure:

1. In the TIM status and control register (TSC):
    a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
    b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH:TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH:TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):
    a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB:MSxA. (See Table 8-3.)
    b. Write 1 to the toggle-on-overflow bit, TOVx.
    c. Write 1:0 (to clear output on compare) or 1:1 (to set output on compare) to the edge/level select bits, ELSxB:ELSxA. The output action on compare must force the output to the complement of the pulse width level. (See Table 8-3.)

> **NOTE**
> *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare can also cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

5. In the TIM status control register (TSC), clear the TIM stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H:TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSC0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0% duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100% duty cycle output. (See 8.9.4 TIM Channel Status and Control Registers (TSC0:TSC1).)

8.9.4 TIM Channel Status and Control Registers (TSC0:TSC1)

Each of the TIM channel status and control registers does the following:
- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIM overflow
- Selects 0% and 100% PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

Address: $0025   TSC0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Address: $0028   TSC1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

☐ = Unimplemented

Figure 8-7. TIM Channel Status and Control Registers (TSC0:TSC1)

CHxF — Channel x Flag Bit
When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM counter registers matches the value in the TIM channel x registers.

When TIM CPU interrupt requests are enabled (CHxIE=1), clear CHxF by reading the TIM channel x status and control register with CHxF set and then writing a zero to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing zero to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a one to CHxF has no effect.
   1 = Input capture or output compare on channel x
   0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit
This read/write bit enables TIM CPU interrupt service requests on channel x. Reset clears the CHxIE bit.
   1 = Channel x CPU interrupt requests enabled
   0 = Channel x CPU interrupt requests disabled

8.9.5 TIM Channel Registers (TCH0H/L:TCH1H/L)

These read/write registers contain the captured TIM counter value of the input capture function or the output compare value of the output compare function. The state of the TIM channel registers after reset is unknown.

In input capture mode (MSxB:MSxA = 0:0), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode (MSxB:MSxA ≠ 0:0), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.

Address: $0026   TCH0H

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Reset:				Indeterminate after reset				

Address: $0027   TCH0L

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reset:				Indeterminate after reset				

Address: $0029   TCH1H

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Reset:				Indeterminate after reset				

Address: $02A   TCH1L

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reset:				Indeterminate after reset				

Figure 8-9. TIM Channel Registers (TCH0H/L:TCH1H/L)

10.2.3 Port A Input Pull-up Enable Register (PTAPUE)

The port A input pull-up enable register (PTAPUE) contains a software configurable pull-up device for each of the seven port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx be configured as input. Each pull-up device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output.

Address:	$000D							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTA6EN	PTAPUE6	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
Reset:	0	0	0	0	0	0	0	0

Figure 10-5. Port A Input Pull-up Enable Register (PTAPUE)

PTA6EN — Enable PTA6 on OSC2
   This read/write bit configures the OSC2 pin function when RC oscillator option is selected. This bit has no effect for X-tal oscillator option.
      1 = OSC2 pin configured for PTA6 I/O, and has all the interrupt and pull-up functions
      0 = OSC2 pin outputs the RC oscillator clock (RCCLK)

PTAPUE[6:0] — Port A Input Pull-up Enable Bits
   These read/write bits are software programmable to enable pull-up devices on port A pins
      1 = Corresponding port A pin configured to have internal pull-up if its DDRA bit is set to 0
      0 = Pull-up device is disconnected on the corresponding port A pin regardless of the state of its DDRA bit

Table 10-2 summarizes the operation of the port A pins.

Table 10-2. Port A Pin Functions

PTAPUE Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	0	X[1]	Input, V_{DD}[2]	DDRA[6:0]	Pin	PTA[6:0][3]
0	0	X	Input, Hi-Z[4]	DDRA[6:0]	Pin	PTA[6:0][3]
X	1	X	Output	DDRA[6:0]	PTA[6:0]	PTA[6:0]

1. X = Don't care.
2. I/O pin pulled to V_{DD} by internal pull-up.
3. Writing affects data register, but does not affect input.
4. Hi-Z = High Impedance.
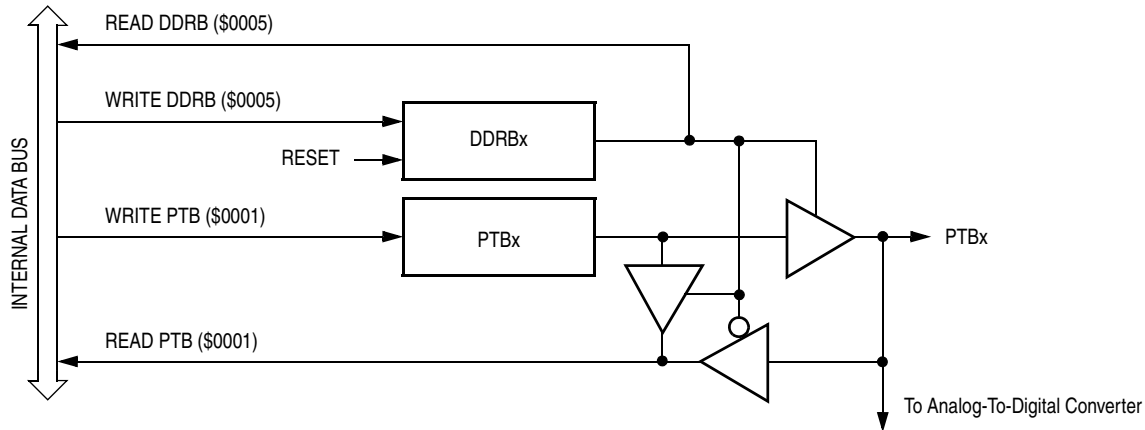
Figure 10-8. Port B I/O Circuit

When DDRBx is a 1, reading address $0001 reads the PTBx data latch. When DDRBx is a 0, reading address $0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 10-3 summarizes the operation of the port B pins.

Table 10-3. Port B Pin Functions

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
			Read/Write	Read	Write
0	X[1]	Input, Hi-Z[2]	DDRB[7:0]	Pin	PTB[7:0][3]
1	X	Output	DDRB[7:0]	Pin	PTB[7:0]

1. X = don't care.
2. Hi-Z = high impedance.
3. Writing affects data register, but does not affect the input.

11.5 IRQ Status and Control Register (INTSCR)

The IRQ status and control register (INTSCR) controls and monitors operation of the IRQ module. The INTSCR has the following functions:
- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks IRQ and interrupt request
- Controls triggering sensitivity of the $\overline{\text{IRQ}}$ interrupt pin

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF		IMASK	MODE
Write:						ACK	IMASK	MODE
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-3. IRQ Status and Control Register (INTSCR)

IRQF — IRQ Flag
This read-only status bit is high when the IRQ interrupt is pending.
1 = $\overline{\text{IRQ}}$ interrupt pending
0 = $\overline{\text{IRQ}}$ interrupt not pending

ACK — IRQ Interrupt Request Acknowledge Bit
Writing a one to this write-only bit clears the IRQ latch. ACK always reads as zero. Reset clears ACK.

IMASK — IRQ Interrupt Mask Bit
Writing a one to this read/write bit disables IRQ interrupt requests. Reset clears IMASK.
1 = IRQ interrupt requests disabled
0 = IRQ interrupt requests enabled

MODE — IRQ Edge/Level Select Bit
This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin. Reset clears MODE.
1 = $\overline{\text{IRQ}}$ interrupt requests on falling edges and low levels
0 = $\overline{\text{IRQ}}$ interrupt requests on falling edges only

Address: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	R	R	LVIT1	LVIT0	R	R	R
Write:	IRQPUD	R	R	LVIT1	LVIT0	R	R	R
Reset:	0	0	0	Not affected	Not affected	0	0	0
POR:	0	0	0	0	0	0	0	0

R = Reserved

Figure 11-4. Configuration Register 2 (CONFIG2)

IRQPUD — $\overline{\text{IRQ}}$ Pin Pull-up control bit
1 = Internal pull-up is disconnected
0 = Internal pull-up is connected between $\overline{\text{IRQ}}$ pin and V_{DD}

MC68HC908JL3E Family Data Sheet, Rev. 4

13.3.7 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register 1.

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	COPRS	R	R	LVID	R	SSREC	STOP	COPD
Reset:	0	0	0	0	0	0	0	0

R	= Reserved

Figure 13-2. Configuration Register 1 (CONFIG1)

COPRS — COP Rate Select Bit
COPRS selects the COP timeout period. Reset clears COPRS.
    1 = COP timeout period is $8176 \times 2OSCOUT$ cycles
    0 = COP timeout period is $262,128 \times 2OSCOUT$ cycles

COPD — COP Disable Bit
COPD disables the COP module.
    1 = COP module disabled
    0 = COP module enabled

13.4 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:				Low byte of reset vector				
Write:				Clear COP counter				
Reset:				Unaffected by reset				

Figure 13-3. COP Control Register (COPCTL)

13.5 Interrupts

The COP does not generate CPU interrupt requests.

13.6 Monitor Mode

The COP is disabled in monitor mode when V_{TST} is present on the $\overline{IRQ}$ pin or on the $\overline{RST}$ pin.

13.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

Chapter 14
Low Voltage Inhibit (LVI)

14.1 Introduction

This section describes the low-voltage inhibit module (LVI), which monitors the voltage on the V_{DD} pin and generates a reset when the V_{DD} voltage falls to the LVI trip (LVI_{TRIP}) voltage.

14.2 Features

Features of the LVI module include the following:
- Selectable LVI trip voltage
- Selectable LVI circuit disable

14.3 Functional Description

Figure 14-1 shows the structure of the LVI module. The LVI is enabled after a reset. The LVI module contains a bandgap reference circuit and comparator. Setting LVI disable bit (LVID) disables the LVI to monitor V_{DD} voltage. The LVI trip voltage selection bits (LVIT1, LVIT0) determine at which V_{DD} level the LVI module should take actions.

The LVI module generates one output signal:

LVI Reset — an reset signal will be generated to reset the CPU when V_{DD} drops to below the set trip point.
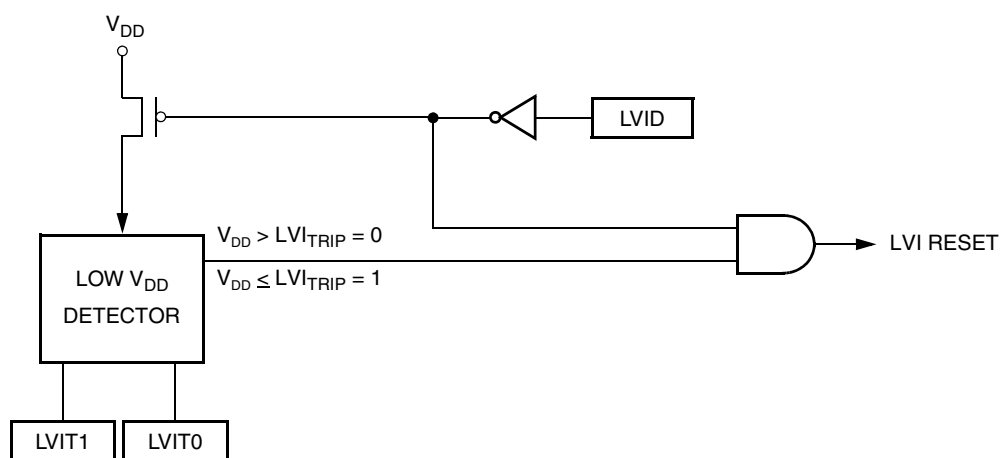

Figure 14-1. LVI Module Block Diagram

Chapter 16
Electrical Specifications

16.1 Introduction

This section contains electrical and timing specifications.

16.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

> **NOTE**
> *This device is not guaranteed to operate properly at the maximum ratings. Refer to 16.5 5V DC Electrical Characteristics and 16.8 3V DC Electrical Characteristics for guaranteed operating conditions.*

Table 16-1. Absolute Maximum Ratings

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +6.0	V
Input voltage	V_{IN}	V_{SS}−0.3 to V_{DD} +0.3	V
Mode entry voltage, $\overline{IRQ}$ pin	V_{TST}	V_{SS}−0.3 to +8.5	V
Maximum current per pin excluding V_{DD} and V_{SS}	I	±25	mA
Storage temperature	T_{STG}	−55 to +150	°C
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA

1. Voltages referenced to V_{SS}.

> **NOTE**
> *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}.)*

NOTES:

1. POSITIONAL TOLERANCE OF LEADS, SHALL BE WITHIN 0.25 MM (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.

2. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH.

4. 710-01 OBSOLETE, NEW STD 710-02.

5. CONTROLLING DIMENSION: INCH

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.435	1.465	36.45	37.21					
B	0.540	0.560	13.72	14.22					
C	0.155	0.200	3.94	5.08					
D	0.014	0.022	0.36	0.56					
F	0.040	0.060	1.02	1.52					
G	0.100 BSC		2.54 BSC						
H	0.065	0.085	1.65	2.16					
J	0.008	0.015	0.20	0.38					
K	0.115	0.135	2.92	3.43					
L	0.600 BSC		15.24 BSC						
M	0°	15°	0°	15°					
N	0.020	0.040	0.51	1.02					

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

28 LD PDIP

DOCUMENT NO: 98ASB42390B

REV: D

CASE NUMBER: 710-02

24 MAY 2005

STANDARD: NON-JEDEC

A.6 MC Order Numbers

Table A-7 shows the ordering numbers for the low-voltage devices.

Table A-7. MC68HLC908JL3E/JK3E/JK1E Order Numbers

MC Order Number	Oscillator Type	Flash Memory	Package
MC68HLC98JL3EIFA	Crystal oscillator	4096 Bytes	48-pin LQFP
MC68HLC98JL3EIP MC68HLC98JL3EIDW	Crystal oscillator	4096 Bytes	28-pin package
MC68HLC98JK3EIP MC68HLC98JK3EIDW	Crystal oscillator	4096 Bytes	20-pin package
MC68HLC98JK1EIP MC68HLC98JK1EIDW	Crystal oscillator	1536 Bytes	

Notes:
I = 0 °C to +85 °C
P = Plastic dual in-line package (PDIP)
DW = Small outline integrated circuit package (SOIC)
FA = Low-Profile Quad Flat Pack (LQFP)

C.4 Reserved Registers

The following registers are reserved location on the MC68HC908KL3E/KK3E.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003C	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
$003D	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
$003E	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								

Figure C-4. Reserved Registers

C.5 Reserved Vectors

The following vectors are reserved interrupt vectors on the MC68HC908KL3E/KK3E.

Table C-2. Reserved Vectors

Vector Priority	INT Flag	Address	Vector
—	IF15	$FFDE	Reserved
		$FFDF	Reserved

C.6 Order Numbers

Table C-3. MC68HC908KL3E/KK3E Order Numbers

MC order number	Package	Operating Temperature	Operating V_DD	OSC	Flash Memory
MC68HC908KL3ECP	28-pin PDIP	−40 to +85 °C	3V, 5V	XTAL	4096 Bytes
MC68HC908KL3ECDW	28-pin SOIC				
MC68HC908KK3ECP	20-pin PDIP				
MC68HC908KK3ECDW	20-pin SOIC				