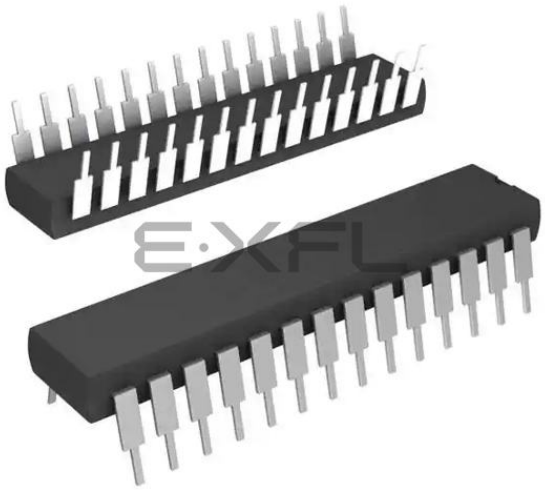

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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcr908jl3ecpe

MC68HC908JL3/JK3E/JK1E
MC68HRC908JL3/JK3E/JK1E
MC68HLC908JL3/JK3E/JK1E
MC68HC908KL3E/KK3E
MC68HC08JL3E/JK3E
MC68HRC08JL3E/JK3E

Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
October 2006	4	Table 4-1. Instruction Set Summary — Updated table to include the WAIT instruction.	42
		5.7.1 Break Status Register (BSR) — Updated for clarity.	63
		5.7.2 Reset Status Register (RSR) — Updated description for clarity.	64
		7.4 Security — Updated to reflect the correct RAM location ($80) to determine if the security code has been entered correctly.	80
		8.9.1 TIM Status and Control Register (TSC) — Added note to definition of TSTOP bit.	89
		10.1 Introduction — Added note regarding 20-pin devices.	103
		15.4.3 Break Status Register — Updated for clarity.	132
		Chapter 17 Mechanical Specifications — Updated package drawings to the latest available.	147
Nov 2004	3	Added appendix B for ROM parts.	159–166
		Added appendix C for ADC-less parts.	167–170
Dec 2002	2	Added appendix A for low-volt devices.	153–224
		Updated Monitor Mode Circuit (Figure 7-1) and Monitor Mode Entry Requirements and Options (Table 7-1) in Monitor ROM section.	76, 77
May 2002	1	First general release.	—

Chapter 6
Oscillator (OSC)

Chapter 7
Monitor ROM (MON)

Chapter 8
Timer Interface Module (TIM)

1.5 Pin Functions

Description of the pin functions are provided in Table 1-2.

Table 1-2. Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
$V_{DDJL3JL3}$	Power supply.	In	5V or 3V
V_{SS}	Power supply ground	Out	0V
$\overline{RST}$	RESET input, active low. With Internal pull-up and Schmitt trigger input.	Input	V_{DD} to V_{TST}
$\overline{IRQ}$	External IRQ pin. With software programmable internal pull-up and schmitt trigger input. This pin is also used for mode entry selection.	Input	V_{DD} to V_{TST}
OSC1	X-tal or RC oscillator input.	In	Analog
OSC2	MC68HC908JL3E/JK3E/JK1E: X-tal oscillator output, this is the inverting OSC1 signal.	Out	Analog
	MC68HRC908JL3E/JK3E/JK1E: Default is RC oscillator clock output, RCCLK. Shared with PTA6/KBI6, with programmable pull-up.	In/Out	V_{DD}
PTA[0:6]	7-bit general purpose I/O port.	In/Out	V_{DD}
	Shared with 7 keyboard interrupts KBI[0:6].	In	V_{DD}
	Each pin has programmable internal pull-up device.	In	V_{DD}
	PTA[0:5] have LED direct sink capability	In	V_{SS}
PTB[0:7]	8-bit general purpose I/O port.	In/Out	V_{DD}
	Shared with 8 ADC inputs, ADC[0:7].	In	Analog
PTD[0:7]	8-bit general purpose I/O port.	In/Out	V_{DD}
	PTD[3:0] shared with 4 ADC inputs, ADC[8:11].	Input	Analog
	PTD[4:5] shared with TIM channels, TCH0 and TCH1.	In/Out	V_{DD}
	PTD[2:3], PTD[6:7] have LED direct sink capability	In	V_{SS}
	PTD[6:7] can be configured as 25mA open-drain output with pull-up.	In/Out	V_{DD}

NOTE

On the MC68H(R)C908JK3E/JK1E, the following pins are not available: PTA0, PTA1, PTA2, PTA3, PTA4, PTA5, PTD0, and PTD1.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE04	Interrupt Status Register 1 (INT1)	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE05	Interrupt Status Register 2 (INT2)	Read:	IF14	0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE06	Interrupt Status Register 3 (INT3)	Read:	0	0	0	0	0	0	0	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE07	Reserved	Read: Write:	R	R	R	R	R	R	R	R
$FE08	Flash Control Register (FLCR)	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE09	Flash Block Protect Register (FLBPR)	Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Reset:	0	0	0	0	0	0	0	0
$FE0A ↓ $FE0B	Reserved	Read: Write:	R	R	R	R	R	R	R	R
$FE0C	Break Address High Register (BRKH)	Read: Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Low Register (BRKL)	Read: Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BRKSCR)	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FFFF	COP Control Register (COPCTL)	Read:	Low byte of reset vector							
		Write:	Writing clears COP counter (any value)							
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 4)

2.12 Flash Block Protect Register

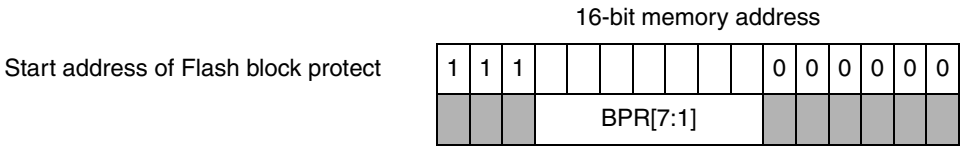
The Flash Block Protect Register is implemented as an 8-bit I/O register. The value in this register determines the starting address of the protected range within the Flash memory.

Address:	$FE09							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

Figure 2-6. Flash Block Protect Register (FLBPR)

BPR[7:0] — Flash Block Protect Register Bit 7 to Bit 0

BPR[7:1] represent bits [12:6] of a 16-bit memory address. Bits [15:13] are 1's and bits [5:0] are 0's.



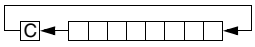
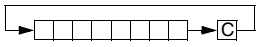
BPR0 is used only for BPR[7:0] = $FF, for no block protection.
The resultant 16-bit address is used for specifying the start address of the Flash memory for block protection. The Flash is protected from this start address to the end of Flash memory, at $FFFF. With this mechanism, the protect start address can be XX00, XX40, XX80, or XXC0 (at page boundaries — 64 bytes) within the Flash memory.

Examples of protect start address:

BPR[7:0]	Start of Address of Protect Range
$00–$60	The entire Flash memory is protected.
$62 or $63 (**0110 001x**)	$EC40 (111**0 1100 01**00 0000)
$64 or $65 (**0110 010x**)	$EC80 (111**0 1100 10**00 0000)
$68 or $69 (**0110 100x**)	$ED00 (111**0 1101 00**00 0000)
and so on...	
$DE or $DF (**1101 111x**)	$FBC0 (111**1 1011 11**00 0000)
$FE (**1111 1110**)	$FFC0 (111**1 1111 11**00 0000)
$FF	The entire Flash memory is not protected.

Note:
The end address of the protected range is always $FFFF.

Table 4-1. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	–	INH	88		2
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X ROL *opr*,SP	Rotate Left through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X ROR *opr*,SP	Rotate Right through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	SP ← $FF	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	–	INH	81		4
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X SBC *opr*,SP SBC *opr*,SP	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X STA *opr*,SP STA *opr*,SP	Store A in M	M ← (A)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
STHX *opr*	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	I ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		1
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X STX *opr*,SP STX *opr*,SP	Store X in M	M ← (X)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

Interrupts are latched, and arbitration is performed in the SIM at the start of interrupt processing. The arbitration result is a constant that the CPU uses to determine which vector to fetch. Once an interrupt is latched by the SIM, no other interrupt can take precedence, regardless of priority, until the latched interrupt is serviced (or the I bit is cleared).

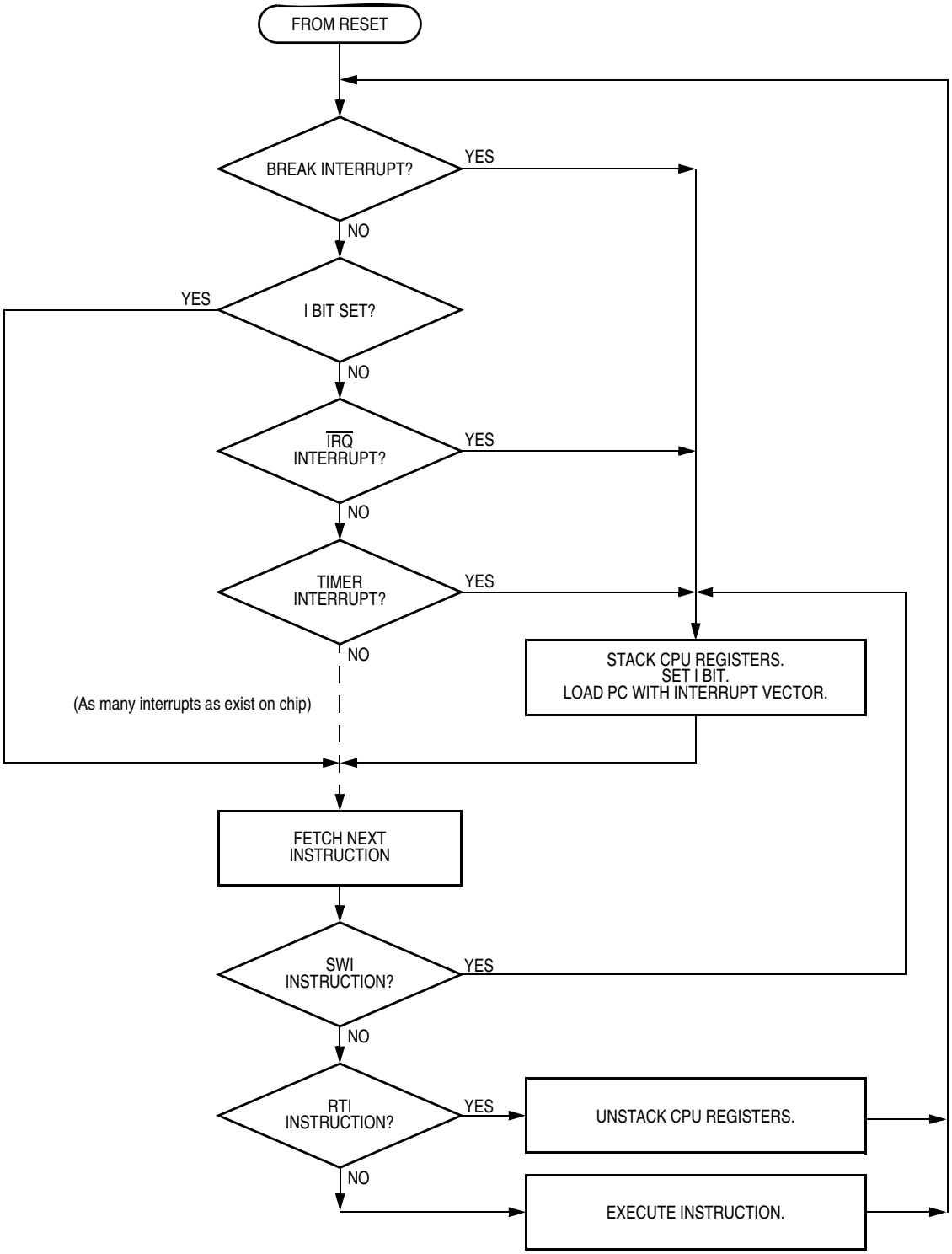


Figure 5-8. Interrupt Processing

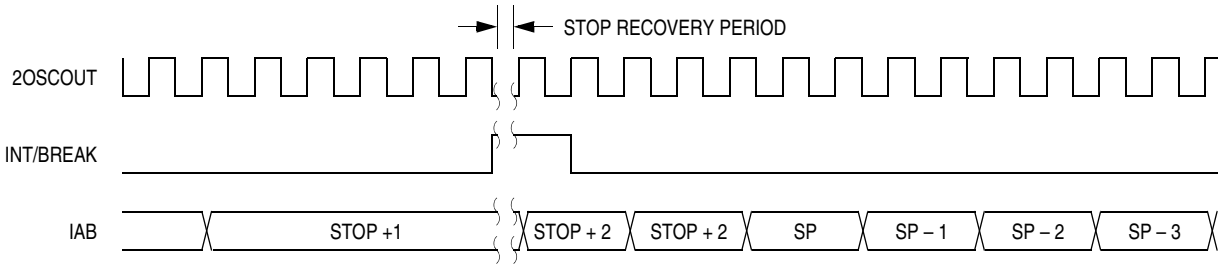


Figure 5-19. Stop Mode Recovery from Interrupt or Break

5.7 SIM Registers

The SIM has three memory mapped registers. Table 5-4 shows the mapping of these registers.

Table 5-4. SIM Registers

Address	Register	Access Mode
$FE00	BSR	User
$FE01	RSR	User
$FE03	BFCR	User

5.7.1 Break Status Register (BSR)

The break status register contains a flag to indicate a break caused by an exit from wait mode.

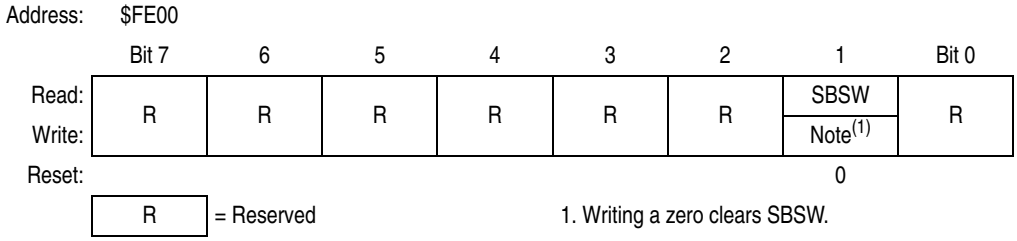


Figure 5-20. Break Status Register (BSR)

SBSW — SIM Break Stop/Wait

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it.

1 = Wait mode was exited by break interrupt

0 = Wait mode was not exited by break interrupt

10.2 Port A

Port A is an 7-bit special function port that shares all seven of its pins with the keyboard interrupt (KBI) module (see Chapter 12 Keyboard Interrupt Module (KBI)). Each port A pin also has software configurable pull-up device if the corresponding port pin is configured as input port. PTA0 to PTA5 has direct LED drive capability.

NOTE

PTA0–PTA5 pins are available on MC68H(R)C908JL3E only.
PTA6 pin is available on MC68HRC908JL3E/JK3E/JK1E only.

10.2.1 Port A Data Register (PTA)

The port A data register (PTA) contains a data latch for each of the seven port A pins.

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Write:								
Reset:	Unaffected by Reset							
Additional Functions:			LED (Sink)	LED (Sink)	LED (Sink)	LED (Sink)	LED (Sink)	LED (Sink)
		30k pull-up	30k pull-up	30k pull-up	30k pull-up	30k pull-up	30k pull-up	30k pull-up
		Keyboard Interrupt	Keyboard Interrupt	Keyboard Interrupt	Keyboard Interrupt	Keyboard Interrupt	Keyboard Interrupt	Keyboard Interrupt

= Unimplemented

Figure 10-2. Port A Data Register (PTA)

PTA[6:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

KBI[6:0] — Port A Keyboard Interrupts

The keyboard interrupt enable bits, KBIE[6:0], in the keyboard interrupt control register (KBIER) enable the port A pins as external interrupt pins, (see Chapter 12 Keyboard Interrupt Module (KBI)).

Chapter 11
External Interrupt (IRQ)

11.1 Introduction

The IRQ (external interrupt) module provides a maskable interrupt input.

11.2 Features

Features of the IRQ module include the following:

- A dedicated external interrupt pin, $\overline{\text{IRQ}}$
- IRQ interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Selectable internal pullup resistor

11.3 Functional Description

A logic zero applied to the external interrupt pin can latch a CPU interrupt request. Figure 11-1 shows the structure of the IRQ module.

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. An interrupt latch remains set until one of the following actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the IRQ latch.
- Software clear — Software can clear the interrupt latch by writing to the acknowledge bit in the interrupt status and control register (INTSCR). Writing a one to the ACK bit clears the IRQ latch.
- Reset — A reset automatically clears the interrupt latch.

The external interrupt pin is falling-edge-triggered and is software-configurable to be either falling-edge or falling-edge and low-level-triggered. The MODE bit in the INTSCR controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

When the interrupt pin is edge-triggered only, the CPU interrupt request remains set until a vector fetch, software clear, or reset occurs.

When the interrupt pin is both falling-edge and low-level-triggered, the CPU interrupt request remains set until both of the following occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic one

16.7 5V Oscillator Characteristics

Table 16-6. Oscillator Component Specifications (5V)

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal frequency, XTALCLK	$f_{OSCXCLK}$	—	10	32	MHz
RC oscillator frequency, RCCLK	f_{RCCLK}	2	10	12	MHz
External clock reference frequency(1)	$f_{OSCXCLK}$	dc	—	32	MHz
Crystal load capacitance(2)	C_L	—	—	—	
Crystal fixed capacitance(2)	C_1	—	$2 \times C_L$	—	
Crystal tuning capacitance(2)	C_2	—	$2 \times C_L$	—	
Feedback bias resistor	R_B	—	10 MΩ	—	
Series resistor(2), (3)	R_S	—	—	—	
RC oscillator external R	R_{EXT}	See Figure 16-1			
RC oscillator external C	C_{EXT}	—	10	—	pF

1. No more than 10% duty cycle deviation from 50%.
2. Consult crystal vendor data sheet.
3. Not required for high frequency crystals.

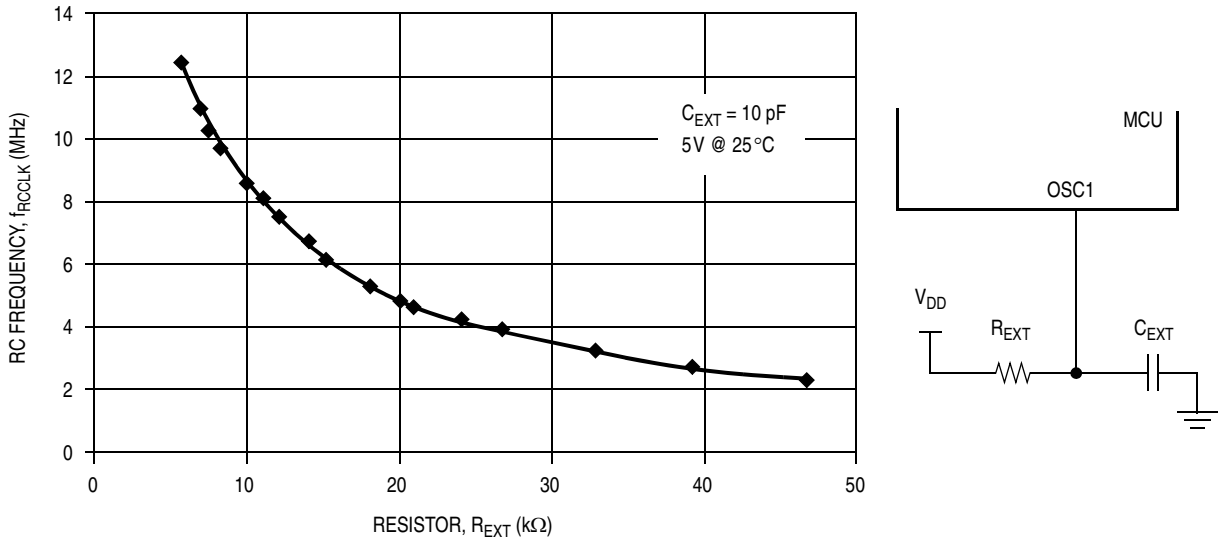


Figure 16-1. RC vs. Frequency (5V @25°C)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	

A.5.2 DC Electrical Characteristics

Table A-2. DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{LOAD} = –1.0mA) PTA0–PTA6, PTB0–PTB7, PTD0–PTD7	V_{OH}	V_{DD}–0.4	—	—	V
Output low voltage (I_{LOAD} = 0.8mA) PTA6, PTB0–PTB7, PTD0, PTD1, PTD4, PTD5	V_{OL}	—	—	0.4	V
Output low voltage (I_{LOAD} = 15mA) PTD6, PTD7	V_{OL}	—	—	0.5	V
Input high voltage PTA0–PTA6, PTB0–PTB7, PTD0–PTD7, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PTA0–PTA6, PTB0–PTB7, PTD0–PTD7, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
V_{DD} supply current (V_{DD} = 2.4V, f_{OP} = 2MHz) Run[3] Wait[4] Stop[5] 0°C to 85°C	I_{DD}	— — —	2 1 1	3.5 1.5 3	mA mA µA
Digital I/O ports Hi-Z leakage current	I_{IL}	—	—	± 10	µA
Input current	I_{IN}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{OUT} C_{IN}	— —	— —	12 8	pF
POR rearm voltage[6]	V_{POR}	0	—	100	mV
POR rise time ramp rate[7]	R_{POR}	0.02	—	—	V/ms
Pullup resistors[8] PTD6, PTD7 $\overline{RST}$, $\overline{IRQ}$, PTA0–PTA6	 R_{PU1} R_{PU2}	 1.8 16	 3.3 26	 4.8 36	 kΩ kΩ

1. V_{DD} = 2.4 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF on OSC2; all ports configured as inputs; OSC2 capacitance linearly affects wait I_{DD}.
5. STOP I_{DD} measured with OSC1 grounded, no port pins sourcing current. LVI is disabled.
6. Maximum is highest voltage that POR is guaranteed.
7. If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{DD} is reached.
8. R_{PU1} and R_{PU2} are measured at V_{DD} = 5.0V

A.6 MC Order Numbers

Table A-7 shows the ordering numbers for the low-voltage devices.

Table A-7. MC68HLC908JL3E/JK3E/JK1E Order Numbers

MC Order Number	Oscillator Type	Flash Memory	Package
MC68HLC98JL3EIFA	Crystal oscillator	4096 Bytes	48-pin LQFP
MC68HLC98JL3EIP MC68HLC98JL3EIDW	Crystal oscillator	4096 Bytes	28-pin package
MC68HLC98JK3EIP MC68HLC98JK3EIDW	Crystal oscillator	4096 Bytes	20-pin package
MC68HLC98JK1EIP MC68HLC98JK1EIDW	Crystal oscillator	1536 Bytes	

Notes:
I = 0 °C to +85 °C
P = Plastic dual in-line package (PDIP)
DW = Small outline integrated circuit package (SOIC)
FA = Low-Profile Quad Flat Pack (LQFP)

Appendix B
MC68H(R)C08JL3E/JK3E

B.1 Introduction

This appendix introduces four devices, that are ROM versions of MC68H(R)C908JL3E/JK3E:

- MC68HC08JL3E
- MC68HC08JK3E
- MC68HRC08JL3E
- MC68HRC08JK3E

The entire data book apply to these ROM devices, with exceptions outlined in this appendix.

Table B-1. Summary of Device Differences

	MC68H(R)C08JL3E/JK3E	MC68H(R)C908JL3E/JK3E
Memory ($EC00–$FBFF)	4,096 bytes ROM	4,096 bytes Flash
User vectors ($FFD0–$FFFF)	48 bytes ROM	48 bytes Flash
Registers at $FE08 and $FE09	Not used; locations are reserved.	Flash related registers. $FE08 — FLCR $FF09 — FLBPR
Monitor ROM ($FC00–$FDFF and $FE10–$FFCF)	$FC00–$FDFF: Not used. $FE10–$FFCF: Used for testing purposes only.	Used for testing and Flash programming/erasing.

B.2 MCU Block Diagram

Figure B-1 shows the block diagram of the MC68H(R)C08JL3E/JK3E.

B.7 Electrical Specifications

Electrical specifications for the MC68H(R)C908JL3E/JK3E apply to the MC68H(R)C08JL3E/JK3E, except for the parameters indicated below.

B.7.1 DC Electrical Characteristics

Table B-2. DC Electrical Characteristics (5V)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
V_{DD} supply current, f_{OP} = 4MHz					
Run[3]					
MC68HC08JL3E/JK3E		—	9	11	mA
MC68HRC08JL3E/JK3E		—	4.3	5	mA
Wait[4]					
MC68HC08JL3E/JK3E		—	5.5	6.5	mA
MC68HRC08JL3E/JK3E		—	0.8	1.5	mA
Stop[5]	I_{DD}				
(–40°C to 85°C)					
MC68HC08JL3E/JK3E		—	1.8	5	µA
MC68HRC08JL3E/JK3E		—	1.8	5	µA
(–40°C to 125°C)					
MC68HC08JL3E/JK3E		—	5	10	µA
MC68HRC08JL3E/JK3E		—	5	10	µA
Pullup resistors[6]					
PTD6, PTD7	R_{PU1}	1.8	4.3	4.8	kΩ
$\overline{RST}$, $\overline{IRQ}$, PTA0–PTA6	R_{PU2}	16	31	36	kΩ

1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{OP} = 4MHz). All inputs 0.2V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using external square wave clock source (f_{OP} = 4MHz). All inputs 0.2V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait I_{DD}.
5. Stop I_{DD} measured with OSC1 grounded; no port pins sourcing current. LVI is disabled.
6. R_{PU1} and R_{PU2} are measured at V_{DD} = 5.0V.

C.4 Reserved Registers

The following registers are reserved location on the MC68HC908KL3E/KK3E.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003C	Reserved	Read: Write: Reset:	R	R	R	R	R	R	R	R
$003D	Reserved	Read: Write: Reset:	R	R	R	R	R	R	R	R
$003E	Reserved	Read: Write: Reset:	R	R	R	R	R	R	R	R

Figure C-4. Reserved Registers

C.5 Reserved Vectors

The following vectors are reserved interrupt vectors on the MC68HC908KL3E/KK3E.

Table C-2. Reserved Vectors

Vector Priority	INT Flag	Address	Vector
—	IF15	$FFDE	Reserved
		$FFDF	Reserved

C.6 Order Numbers

Table C-3. MC68HC908KL3E/KK3E Order Numbers

MC order number	Package	Operating Temperature	Operating V_{DD}	OSC	Flash Memory
MC68HC908KL3ECP	28-pin PDIP	–40 to +85 °C	3V, 5V	XTAL	4096 Bytes
MC68HC908KL3ECDW	28-pin SOIC				
MC68HC908KK3ECP	20-pin PDIP				
MC68HC908KK3ECDW	20-pin SOIC				