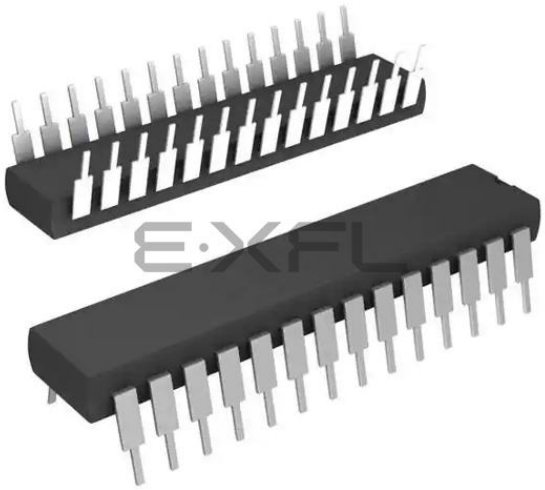


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcr908jl3empe

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
October 2006	4	Table 4-1. Instruction Set Summary — Updated table to include the WAIT instruction.	42
		5.7.1 Break Status Register (BSR) — Updated for clarity.	63
		5.7.2 Reset Status Register (RSR) — Updated description for clarity.	64
		7.4 Security — Updated to reflect the correct RAM location ($80) to determine if the security code has been entered correctly.	80
		8.9.1 TIM Status and Control Register (TSC) — Added note to definition of TSTOP bit.	89
		10.1 Introduction — Added note regarding 20-pin devices.	103
		15.4.3 Break Status Register — Updated for clarity.	132
		Chapter 17 Mechanical Specifications — Updated package drawings to the latest available.	147
Nov 2004	3	Added appendix B for ROM parts.	159–166
		Added appendix C for ADC-less parts.	167–170
Dec 2002	2	Added appendix A for low-volt devices.	153–224
		Updated Monitor Mode Circuit (Figure 7-1) and Monitor Mode Entry Requirements and Options (Table 7-1) in Monitor ROM section.	76, 77
May 2002	1	First general release.	—

Appendix C
MC68HC908KL3E/KK3E

1.2 Features

Features of the MC68H(R)C908JL3E include the following:

- EMC enhanced version of MC68H(R)C908JL3/JK3/JK1
- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Low-power design; fully static with stop and wait modes
- Maximum internal bus frequency:
  - 8-MHz at 5V operating voltage
  - 4-MHz at 3V operating voltage
- Oscillator options:
  - Crystal oscillator for MC68HC908JL3E/JK3E/JK1E
  - RC oscillator for MC68HRC908JL3E/JK3E/JK1E
- User program Flash memory with security[1] feature
  - 4,096 bytes for MC68H(R)C908JL3E/JK3E
  - 1,536 bytes for MC68H(R)C908JK1E
- 128 bytes of on-chip RAM
- 2-channel, 16-bit timer interface module (TIM)
- 12-channel, 8-bit analog-to-digital converter (ADC)
- 23 general purpose I/O ports for MC68H(R)C908JL3E:
  - 7 keyboard interrupt with internal pull-up
    (6 keyboard interrupt for MC68HC908JL3E)
  - 10 LED drivers (sink)
  - 2 × 25mA open-drain I/O with pull-up
- 15 general purpose I/O ports for MC68H(R)C908JK3E/JK1E:
  - 1 keyboard interrupt with internal pull-up
    (MC68HRC908JK3E/JK1E only)
  - 4 LED drivers (sink)
  - 2 × 25mA open-drain I/O with pull-up
  - 10-channel ADC
- System protection features:
  - Optional computer operating properly (COP) reset
  - Optional low-voltage detection with reset and selectable trip points for 3V and 5V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Master reset pin with internal pull-up and power-on reset
- $\overline{\text{IRQ}}$ with schmitt-trigger input and programmable pull-up
- 28-pin PDIP, 28-pin SOIC, and 48-pin LQFP packages for MC68H(R)C908JL3E
- 20-pin PDIP and 20-pin SOIC packages for MC68H(R)C908JK3E/JK1E

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the Flash difficult for unauthorized users.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE04	Interrupt Status Register 1 (INT1)	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE05	Interrupt Status Register 2 (INT2)	Read:	IF14	0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE06	Interrupt Status Register 3 (INT3)	Read:	0	0	0	0	0	0	0	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE07	Reserved	Read: Write:	R	R	R	R	R	R	R	R
$FE08	Flash Control Register (FLCR)	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE09	Flash Block Protect Register (FLBPR)	Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Reset:	0	0	0	0	0	0	0	0
$FE0A ↓ $FE0B	Reserved	Read: Write:	R	R	R	R	R	R	R	R
$FE0C	Break Address High Register (BRKH)	Read: Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Low Register (BRKL)	Read: Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BRKSCR)	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FFFF	COP Control Register (COPCTL)	Read:	Low byte of reset vector							
		Write:	Writing clears COP counter (any value)							
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 4)

2.8 Flash Page Erase Operation

Use the following procedure to erase a page of Flash memory. A page consists of 64 consecutive bytes starting from addresses $XX00, $XX40, $XX80 or $XXC0. The 48-byte user interrupt vectors area also forms a page. Any page within the 4K bytes user memory area ($EC00–$FBFF) can be erased alone. *The 48-byte user interrupt vectors cannot be erased by the page erase operation because of security reasons. Mass erase is required to erase this page.*

1. Set the ERASE bit and clear the MASS bit in the Flash Control Register.
2. Write any data to any Flash address within the page address range desired.
3. Wait for a time, t_{nvs} (10μs).
4. Set the HVEN bit.
5. Wait for a time t_{Erase} (1ms).
6. Clear the ERASE bit.
7. Wait for a time, t_{nvh} (5μs).
8. Clear the HVEN bit.
9. After time, t_{rcv} (1μs), the memory can be accessed in read mode again.

NOTE

Programming and erasing of Flash locations cannot be performed by code being executed from the Flash memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.

2.9 Flash Mass Erase Operation

Use the following procedure to erase the entire Flash memory:

1. Set both the ERASE bit and the MASS bit in the Flash Control Register.
2. Write any data to any Flash location within the Flash memory address range.
3. Wait for a time, t_{nvs} (10μs).
4. Set the HVEN bit.
5. Wait for a time t_{MErase} (4ms).
6. Clear the ERASE bit.
7. Wait for a time, t_{nvh1} (100μs).
8. Clear the HVEN bit.
9. After time, t_{rcv} (1μs), the memory can be accessed in read mode again.

NOTE

Programming and erasing of Flash locations cannot be performed by code being executed from the Flash memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.

4.3.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	V	1	1	H	I	N	Z	C
Reset:	X	1	1	X	1	X	X	X

X = Indeterminate

Figure 4-6. Condition Code Register (CCR)

V — Overflow Flag

The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.

1 = Overflow
0 = No overflow

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C flags to determine the appropriate correction factor.

1 = Carry between bits 3 and 4
0 = No carry between bits 3 and 4

I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled
0 = Interrupts enabled

NOTE

To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.

After the I bit is cleared, the highest-priority interrupt request is serviced first.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

N — Negative Flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

1 = Negative result
0 = Non-negative result

5.6 Low-Power Modes

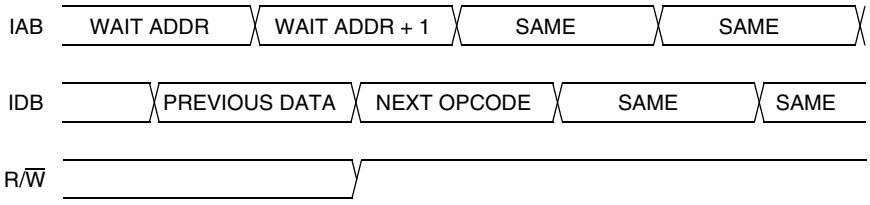
Executing the WAIT or STOP instruction puts the MCU in a low-power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described below. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

5.6.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. Figure 5-15 shows the timing for wait mode entry.

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

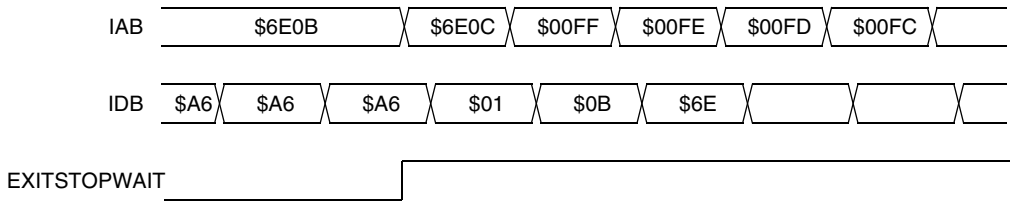
Wait mode can also be exited by a reset or break. A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the break status register (BSR). If the COP disable bit, COPD, in the mask option register is zero, then the computer operating properly module (COP) is enabled and remains active in wait mode.



NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 5-15. Wait Mode Entry Timing

Figure 5-16 and Figure 5-17 show the timing for WAIT recovery.



NOTE: EXITSTOPWAIT = $\overline{\text{RST}}$ pin OR CPU interrupt OR break interrupt

Figure 5-16. Wait Recovery from Interrupt or Break

Chapter 6
Oscillator (OSC)

6.1 Introduction

The oscillator module provides the reference clock for the MCU system and bus. Two types of oscillator modules are available:

- MC68HC908JL3E/JK3E/JK1E — built-in oscillator module (X-tal) that requires an external crystal or ceramic-resonator. This option also allows an external clock that can be driven directly into OSC1.
- MC68HRC908JL3E/JK3E/JK1E — built-in oscillator module (RC) that requires an external RC connection only.

6.2 X-tal Oscillator (MC68HC908JL3E/JK3E/JK1E)

The X-tal oscillator circuit is designed for use with an external crystal or ceramic resonator to provide accurate clock source.

In its typical configuration, the X-tal oscillator is connected in a Pierce oscillator configuration, as shown in Figure 6-1. This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X_1
- Fixed capacitor, C_1
- Tuning capacitor, C_2 (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S (optional)

The series resistor (R_S) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.

6.3 RC Oscillator (MC68HRC908JL3E/JK3E/JK1E)

The RC oscillator circuit is designed for use with external R and C to provide a clock source with tolerance less than 10%.

In its typical configuration, the RC oscillator requires two external components, one R and one C. Component values should have a tolerance of 1% or less, to obtain a clock source with less than 10% tolerance. The oscillator configuration uses two components:

- C_{EXT}
- R_{EXT}

The RC connection is shown in Figure 6-2.

7.3.3 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. (See Figure 7-3 and Figure 7-4.)

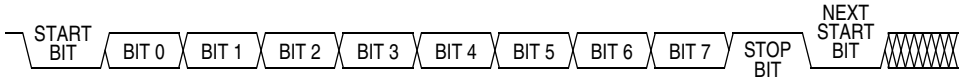


Figure 7-3. Monitor Data Format

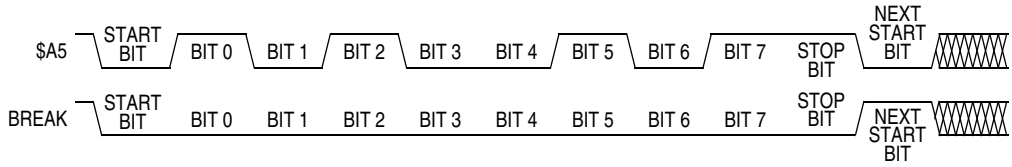


Figure 7-4. Sample Monitor Waveforms

The data transmit and receive rate can be anywhere from 4800 baud to 28.8k-baud. Transmit and receive baud rates must be identical.

7.3.4 Echoing

As shown in Figure 7-5, the monitor ROM immediately echoes each received byte back to the PTB0 pin for error checking.

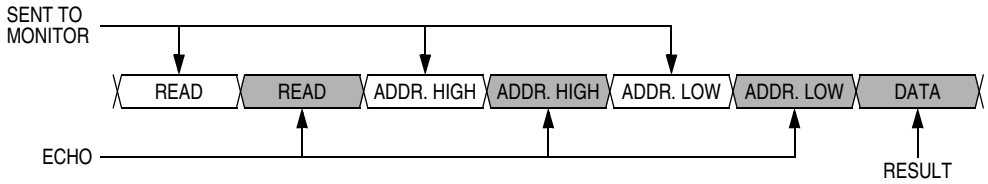


Figure 7-5. Read Transaction

Any result of a command appears after the echo of the last byte of the command.

7.3.5 Break Signal

A start bit followed by nine low bits is a break signal. (See **Figure 7-6**.) When the monitor receives a break signal, it drives the PTB0 pin high for the duration of two bits before echoing the break signal.

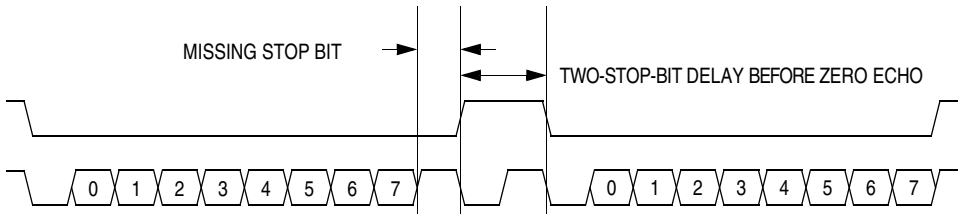


Figure 7-6. Break Transaction

8.9.2 TIM Counter Registers (TCNTH:TCNTL)

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

NOTE

If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.

Address: $0021 TCNTH

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Write:								
Reset:	0	0	0	0	0	0	0	0

Address: $0022 TCNTL

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 8-5. TIM Counter Registers (TCNTH:TCNTL)

8.9.3 TIM Counter Modulo Registers (TMODH:TMODL)

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from $0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

Address: $0023 TMODH

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Reset:	1	1	1	1	1	1	1	1

Address: $0024 TMODL

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reset:	1	1	1	1	1	1	1	1

Figure 8-6. TIM Counter Modulo Registers (TMODH:TMODL)

NOTE

Reset the TIM counter before writing to the TIM counter modulo registers.

TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM counter overflows. When channel x is an input capture channel, TOVx has no effect. Reset clears the TOVx bit.

1 = Channel x pin toggles on TIM counter overflow.
0 = Channel x pin does not toggle on TIM counter overflow.

NOTE

When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at one, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As Figure 8-8 shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.

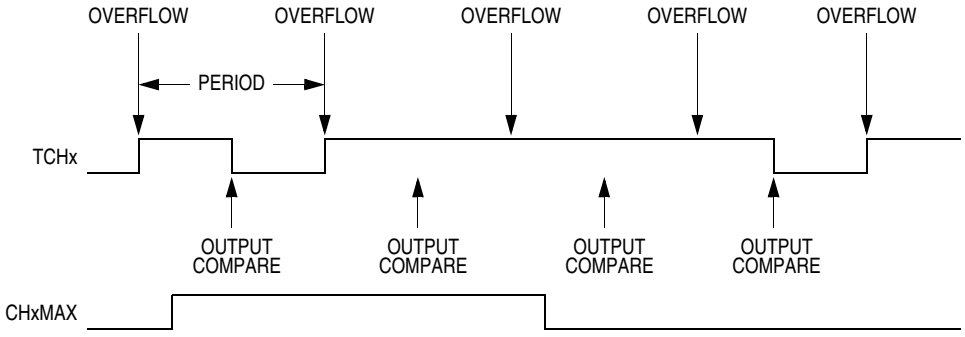


Figure 8-8. CHxMAX Latency

10.2.3 Port A Input Pull-up Enable Register (PTAPUE)

The port A input pull-up enable register (PTAPUE) contains a software configurable pull-up device for each of the seven port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx be configured as input. Each pull-up device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output.

Address: $000D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTA6EN	PTAPUE6	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
Reset:	0	0	0	0	0	0	0	0

Figure 10-5. Port A Input Pull-up Enable Register (PTAPUE)

PTA6EN — Enable PTA6 on OSC2

This read/write bit configures the OSC2 pin function when RC oscillator option is selected. This bit has no effect for X-tal oscillator option.

1 = OSC2 pin configured for PTA6 I/O, and has all the interrupt and pull-up functions
0 = OSC2 pin outputs the RC oscillator clock (RCCLK)

PTAPUE[6:0] — Port A Input Pull-up Enable Bits

These read/write bits are software programmable to enable pull-up devices on port A pins

1 = Corresponding port A pin configured to have internal pull-up if its DDRA bit is set to 0
0 = Pull-up device is disconnected on the corresponding port A pin regardless of the state of its DDRA bit

Table 10-2 summarizes the operation of the port A pins.

Table 10-2. Port A Pin Functions

PTAPUE Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	0	X(1)	Input, V_{DD}(2)	DDRA[6:0]	Pin	PTA[6:0](3)
0	0	X	Input, Hi-Z(4)	DDRA[6:0]	Pin	PTA[6:0](3)
X	1	X	Output	DDRA[6:0]	PTA[6:0]	PTA[6:0]

1. X = Don't care.
2. I/O pin pulled to V_{DD} by internal pull-up.
3. Writing affects data register, but does not affect input.
4. Hi-Z = High Impedance.

16.3 Functional Operating Range

Table 16-2. Operating Range

Characteristic	Symbol	Value		Unit
Operating temperature range	T_A	−40 to +125	−40 to +85	°C
Operating voltage range	V_{DD}	5 ±10%	3 ±10%	V

16.4 Thermal Characteristics

Table 16-3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 20-pin PDIP 20-pin SOIC 28-pin PDIP 28-pin SOIC 48-pin LQFP	θ_{JA}	 70 70 70 70 80	 °C/W °C/W °C/W °C/W °C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273\ °C)$	W
Constant(2)	K	$P_D \times (T_A + 273\ °C) + P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C

1. Power dissipation is a function of temperature.
2. K constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

NOTES:

1. POSITIONAL TOLERANCE OF LEADS, SHALL BE WITHIN 0.25 MM (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.

2. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH.

4. 710-01 OBSOLETE, NEW STD 710-02.

5. CONTROLLING DIMENSION: INCH

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.435	1.465	36.45	37.21					
B	0.540	0.560	13.72	14.22					
C	0.155	0.200	3.94	5.08					
D	0.014	0.022	0.36	0.56					
F	0.040	0.060	1.02	1.52					
G	0.100 BSC		2.54 BSC						
H	0.065	0.085	1.65	2.16					
J	0.008	0.015	0.20	0.38					
K	0.115	0.135	2.92	3.43					
L	0.600 BSC		15.24 BSC						
M	0°	15°	0°	15°					
N	0.020	0.040	0.51	1.02					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:

28 LD PDIP

DOCUMENT NO: 98ASB42390B | REV: D

CASE NUMBER: 710-02 | 24 MAY 2005

STANDARD: NON-JEDEC

Chapter 18
Ordering Information

18.1 Introduction

This section contains ordering numbers for the MC68H(R)C908JL3E, MC68H(R)C908JK3E, and MC68H(R)C908JK1E.

18.2 MC Order Numbers

Table 18-1. MC Order Numbers

MC Order Number	Oscillator Type	Flash Memory	Package
MC68HC908JL3ECFA MC68HC908JL3EMFA	Crystal oscillator	4096 Bytes	48-pin LQFP
MC68HRC98JL3ECFA MC68HRC98JL3EMFA	RC oscillator		
MC68HC908JL3ECP MC68HC908JL3EMP MC68HC908JL3ECDW MC68HC908JL3EMDW	Crystal oscillator	4096 Bytes	28-pin package
MC68HRC98JL3ECP MC68HRC98JL3EMP MC68HRC98JL3ECDW MC68HRC98JL3EMDW	RC oscillator		
MC68HC908JK3ECP MC68HC908JK3EMP MC68HC908JK3ECDW MC68HC908JK3EMDW	Crystal oscillator	4096 Bytes	20-pin package
MC68HRC98JK3ECP MC68HRC98JK3EMP MC68HRC98JK3ECDW MC68HRC98JK3EMDW	RC oscillator		
MC68HC908JK1ECP MC68HC908JK1EMP MC68HC908JK1ECDW MC68HC908JK1EMDW	Crystal oscillator	1536 Bytes	
MC68HRC98JK1ECP MC68HRC98JK1EMP MC68HRC98JK1ECDW MC68HRC98JK1EMDW	RC oscillator		

Temperature: C = –40°C to +85°C M = –40°C to +125°C (available for V_{DD} = 5V only)
Package: P = PDIP DW = SOIC FA = LQFP

A.6 MC Order Numbers

Table A-7 shows the ordering numbers for the low-voltage devices.

Table A-7. MC68HLC908JL3E/JK3E/JK1E Order Numbers

MC Order Number	Oscillator Type	Flash Memory	Package
MC68HLC98JL3EIFA	Crystal oscillator	4096 Bytes	48-pin LQFP
MC68HLC98JL3EIP MC68HLC98JL3EIDW	Crystal oscillator	4096 Bytes	28-pin package
MC68HLC98JK3EIP MC68HLC98JK3EIDW	Crystal oscillator	4096 Bytes	20-pin package
MC68HLC98JK1EIP MC68HLC98JK1EIDW	Crystal oscillator	1536 Bytes	

Notes:
I = 0 °C to +85 °C
P = Plastic dual in-line package (PDIP)
DW = Small outline integrated circuit package (SOIC)
FA = Low-Profile Quad Flat Pack (LQFP)

B.4 Reserved Registers

The two registers at $FE08 and $FE09 are reserved locations on the MC68H(R)C08JL3E/JK3E.

On the MC68H(R)C908JL3E/JK3E, these two locations are the Flash control register and the Flash block protect register respectively.

B.5 Mask Option Registers

This section describes the mask option registers (MOR1 and MOR2). The mask option registers enable or disable the following options:

- Stop mode recovery time (32 × 2OSCOUT cycles or 4096 × 2OSCOUT cycles)
- STOP instruction
- Computer operating properly module (COP)
- COP reset period (COPRS), 8176 × 2OSCOUT or 262,128 × 2OSCOUT
- Enable LVI circuit
- Select LVI trip voltage

B.5.1 Functional Description

The mask options are hard-wired connections, specified at the same time as the ROM code, which allow the user to customize the MCU.

B.5.2 Mask Option Register 1 (MOR1)

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	0	0	LVID	0	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-1. Mask Option Register 1 (MOR1)

COPRS — COP reset period selection bit

1 = COP reset cycle is 8176 × 2OSCOUT
0 = COP reset cycle is 262,128 × 2OSCOUT

LVID — Low Voltage Inhibit Disable Bit

1 = Low Voltage Inhibit disabled
0 = Low Voltage Inhibit enabled

B.7 Electrical Specifications

Electrical specifications for the MC68H(R)C908JL3E/JK3E apply to the MC68H(R)C08JL3E/JK3E, except for the parameters indicated below.

B.7.1 DC Electrical Characteristics

Table B-2. DC Electrical Characteristics (5V)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
V_{DD} supply current, f_{OP} = 4MHz					
Run[3]					
MC68HC08JL3E/JK3E		—	9	11	mA
MC68HRC08JL3E/JK3E		—	4.3	5	mA
Wait[4]					
MC68HC08JL3E/JK3E		—	5.5	6.5	mA
MC68HRC08JL3E/JK3E		—	0.8	1.5	mA
Stop[5]	I_{DD}				
(–40°C to 85°C)					
MC68HC08JL3E/JK3E		—	1.8	5	µA
MC68HRC08JL3E/JK3E		—	1.8	5	µA
(–40°C to 125°C)					
MC68HC08JL3E/JK3E		—	5	10	µA
MC68HRC08JL3E/JK3E		—	5	10	µA
Pullup resistors[6]					
PTD6, PTD7	R_{PU1}	1.8	4.3	4.8	kΩ
$\overline{RST}$, $\overline{IRQ}$, PTA0–PTA6	R_{PU2}	16	31	36	kΩ

1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{OP} = 4MHz). All inputs 0.2V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using external square wave clock source (f_{OP} = 4MHz). All inputs 0.2V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait I_{DD}.
5. Stop I_{DD} measured with OSC1 grounded; no port pins sourcing current. LVI is disabled.
6. R_{PU1} and R_{PU2} are measured at V_{DD} = 5.0V.

Appendix C
MC68HC908KL3E/KK3E

C.1 Introduction

This appendix introduces two devices, that are ADC-less versions of MC68HC908JL3E/JK3E:

- MC68HC908KL3E
- MC68HC908KK3E

The entire data book applies to these devices, with exceptions outlined in this appendix.

Table C-1. Summary of MC68HC908KL3E/KK3E and MC68HC908JL3E Differences

	MC68HC908KL3E/KK3E	MC68HC908JL3E
Analog-to-Digital Converter (ADC)	—	12-channel, 8-bit.
Registers at: **$003C, $003E, and $003E**	Not used; locations are reserved.	ADC registers.
Interrupt Vector at: **$FFDE and $FFDF**	Not used.	ADC interrupt vector.
Available Packages	20-pin PDIP (MC68HC908KK3E) 20-pin SOIC (MC68HC908KK3E) 28-pin PDIP 28-pin SOIC —	20-pin PDIP (MC68HC908JK3E) 20-pin SOIC (MC68HC908JK3E) 28-pin PDIP 28-pin SOIC 48-pin LQFP

C.2 MCU Block Diagram

Figure C-1 shows the block diagram of the MC68HC908KL3E/KK3E.

C.3 Pin Assignments

Figure C-2 and Figure C-3 show the pin assignments for the MC68HC908KL3E/KK3E.