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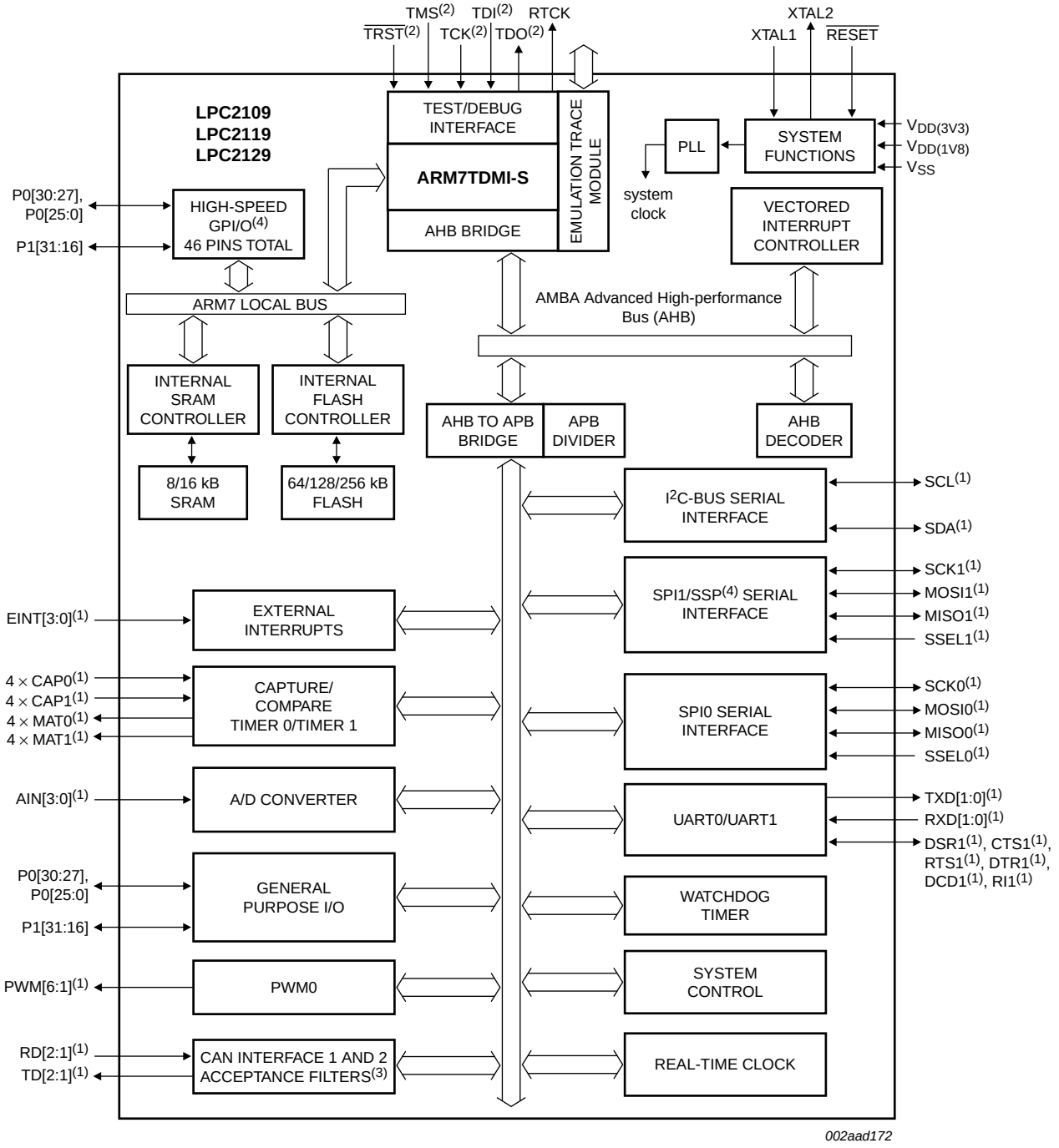
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2119fbd64-01-15

4. Block diagram



(1) Shared with GPIO.

(2) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(3) Only 1 for LPC2109.

(4) SSP interface and high-speed GPIO are available on LPC2109/01, LPC2119/01, and LPC2129/01 only.

Fig 1. Block diagram

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	19	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	21	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/ CAP0[0]	22	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	26	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	27	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	29	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	30	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	31	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4	33	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	34	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	35	O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	37	I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P0[12]/DSR1/ MAT1[0]	38	I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P0[13]/DTR1/ MAT1[1]	39	O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
P0[14]/DCD1/ EINT1	41	I	**DCD1 —** Data Carrier Detect input for UART1.
		I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take control of the part after reset.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
$V_{DDA(1V8)}$	63	I	Analog 1.8 V core power supply; this is the power supply voltage for internal circuitry. This should be nominally the same voltage as $V_{DD(1V8)}$ but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	23, 43, 51	I	3.3 V pad power supply; this is the power supply voltage for the I/O ports.
$V_{DDA(3V3)}$	7	I	Analog 3.3 V pad power supply; this should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error.

[1] SSP interface available on LPC2109/01, LPC2119/01, and LPC2129/01 only.

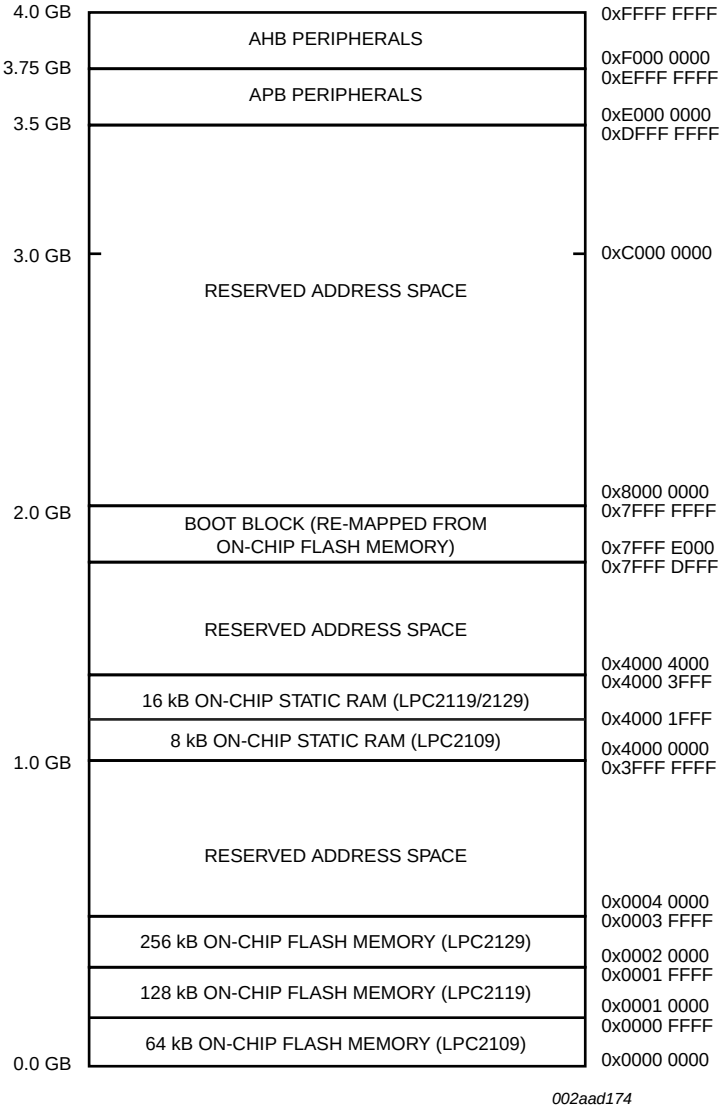


Fig 3. LPC2109/2119/2129 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt reQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

6.8 10-bit ADC

The LPC2109/2119/2129 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.8.2 ADC features available in LPC2109/2119/2129/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.9 CAN controllers and acceptance filter

The LPC2119 and LPC2129 each contain two CAN controllers, while the LPC2109 has one CAN controller. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low-cost multiplex wiring.

6.9.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0 B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit Rx identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

6.10 UARTs

The LPC2109/2119/2129 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.

to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Timer or external event counter operation
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.14.2 Features available in LPC2109/2119/2129/01 only

The LPC2109/2119/2129/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer’s capture inputs can be selected as the timer’s clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAPn input cannot be shorter than 1 / (2PCLK).

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.

- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable reference clock divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2109/2119/2129. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2109/2119/2129: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Code security (Code Read Protection - CRP)

This feature of the LPC2109/2119/2129 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

8. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I$ < 5 V	[9]	0	0	0	μA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

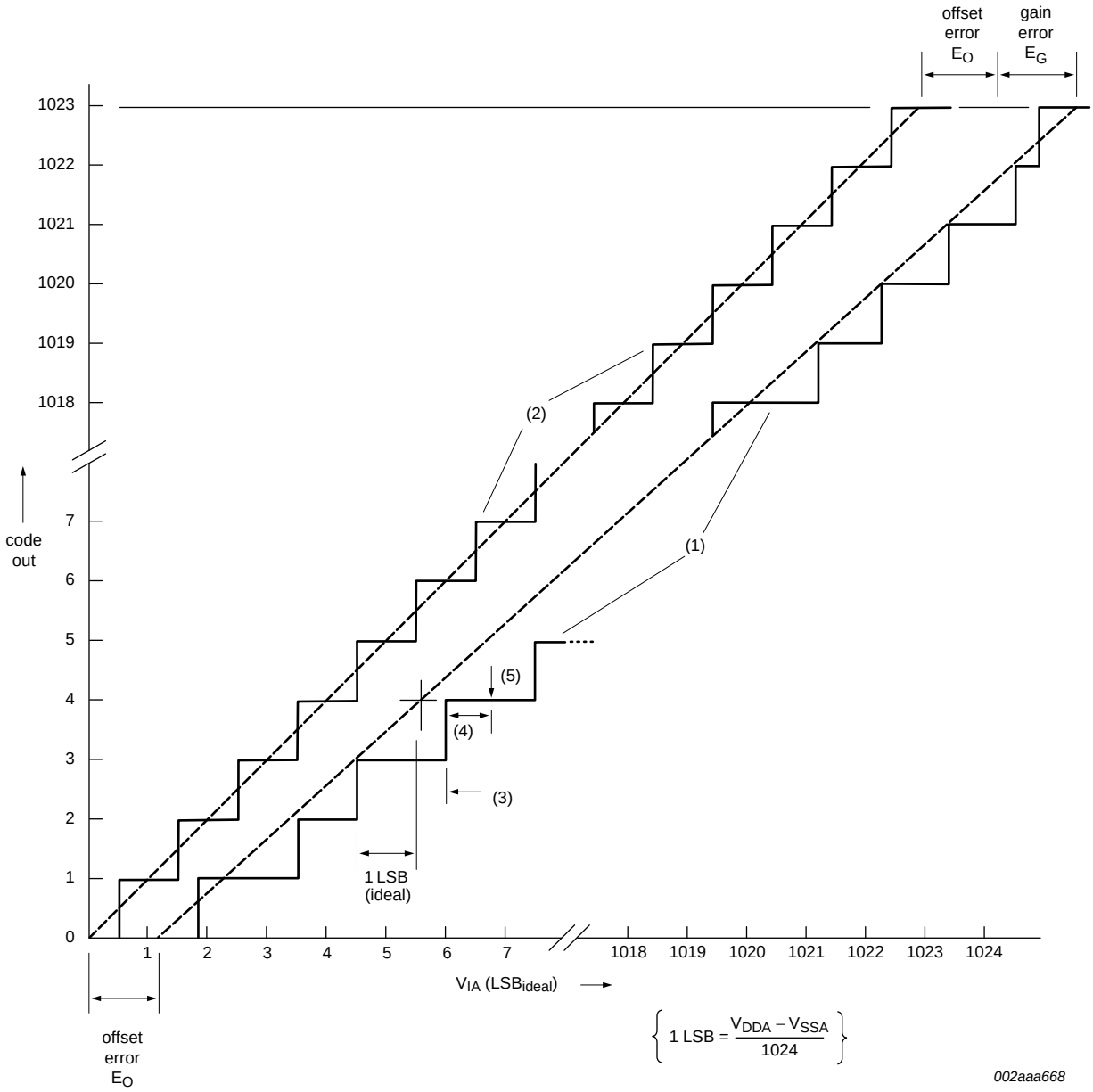
[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

[11] See *LPC2119/2129/2194/2292/2294 User Manual*.

[12] To V_{SS}.



(1) Example of an actual transfer curve.

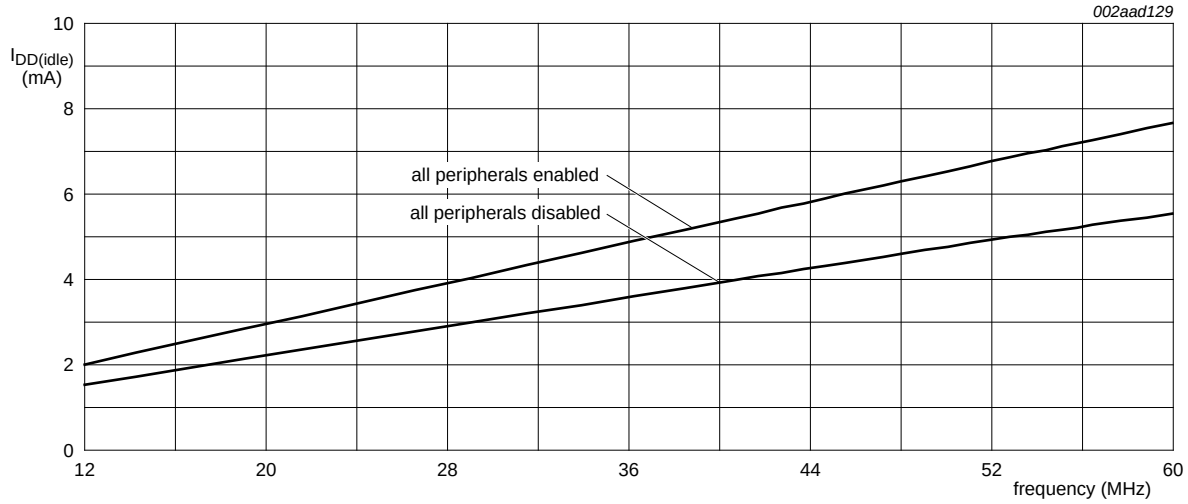
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

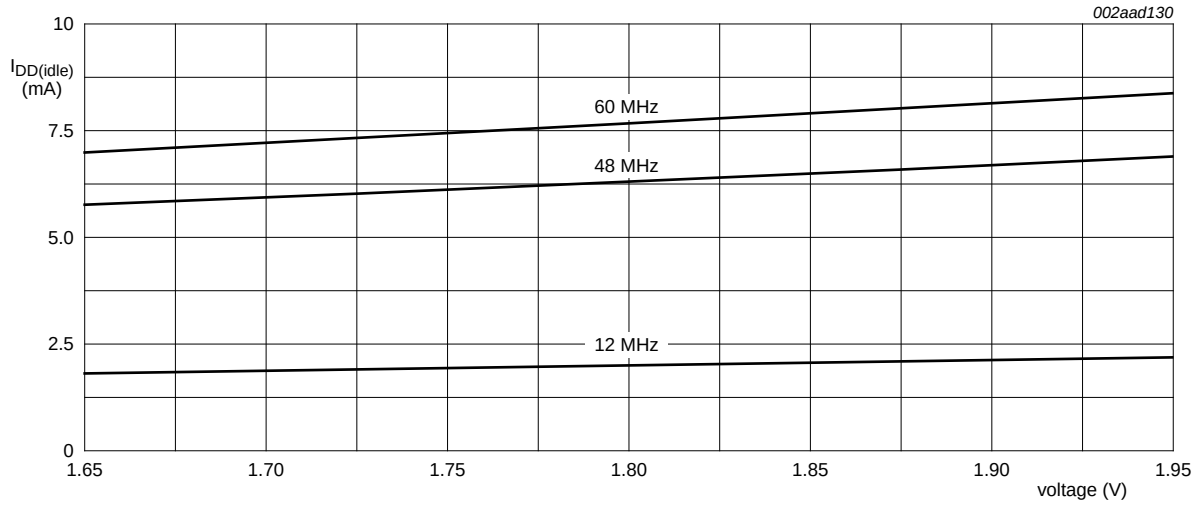
(5) Center of a step of the actual transfer curve.

Fig 4. ADC characteristics



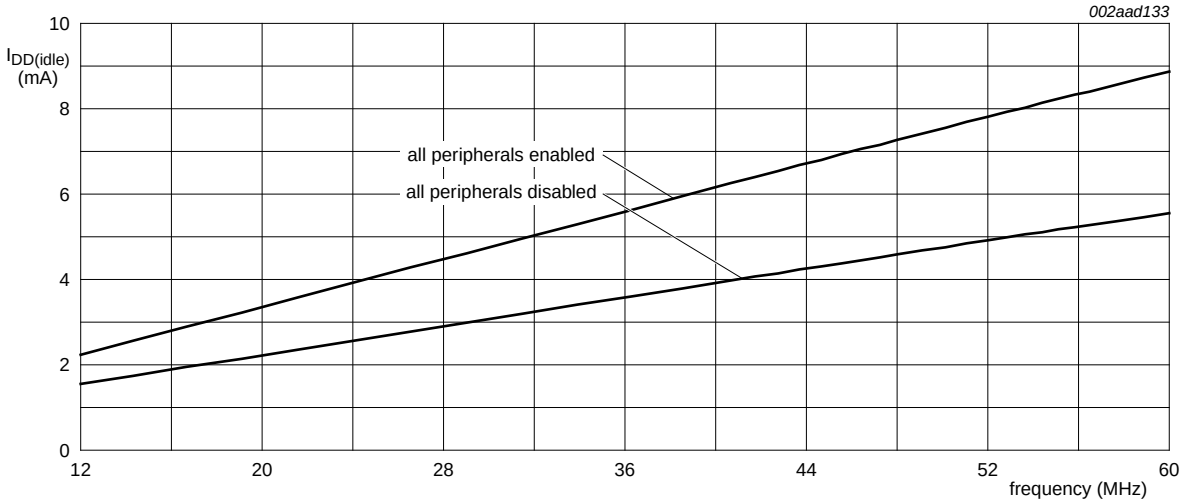
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 7. Typical LPC2109/01 $I_{DD(idle)}$ measured at different frequencies



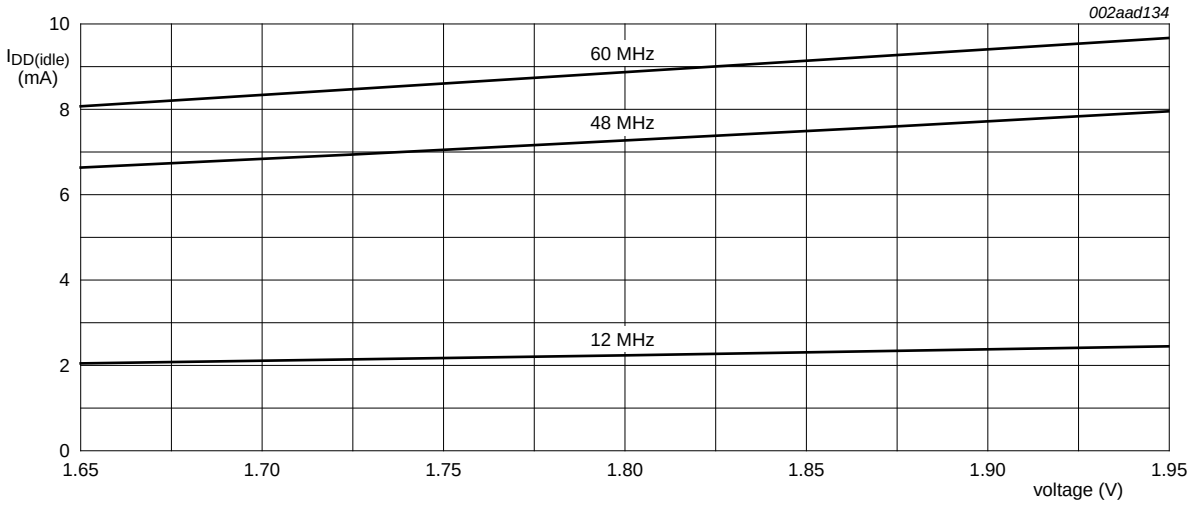
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V; all peripherals enabled.

Fig 8. Typical LPC2109/01 $I_{DD(idle)}$ measured at different voltages



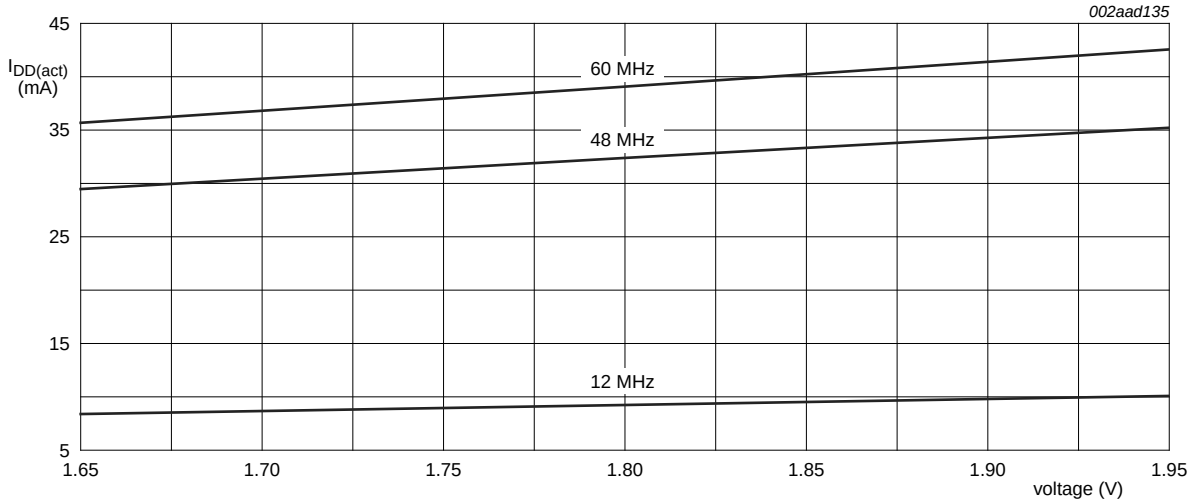
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 11. Typical LPC2119/01 and LPC2129/01 $I_{DD(idle)}$ measured at different frequencies



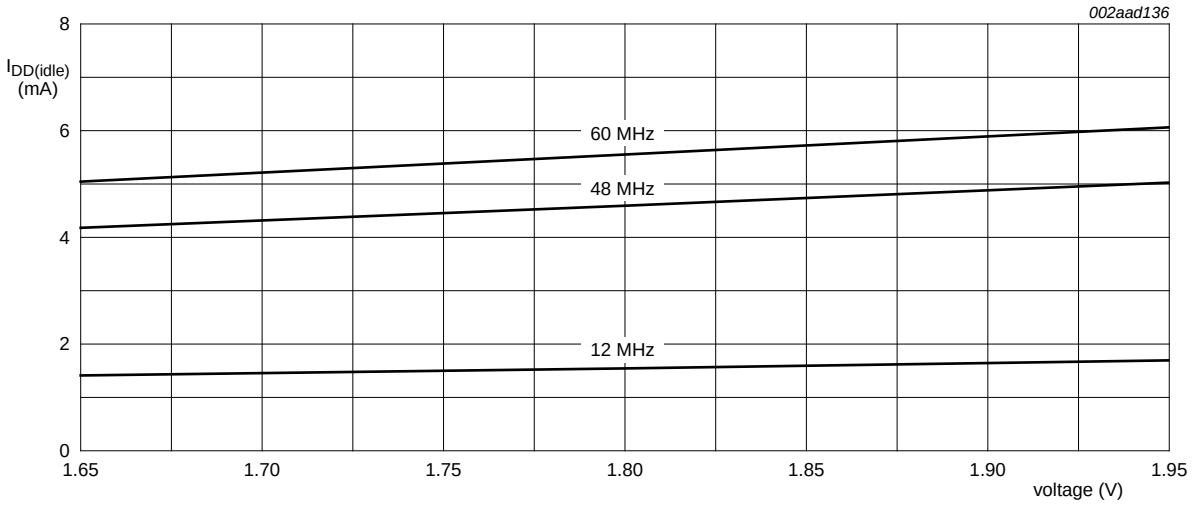
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V; all peripherals enabled.

Fig 12. Typical LPC2119/01 and LPC2129/01 $I_{DD(idle)}$ measured at different voltages



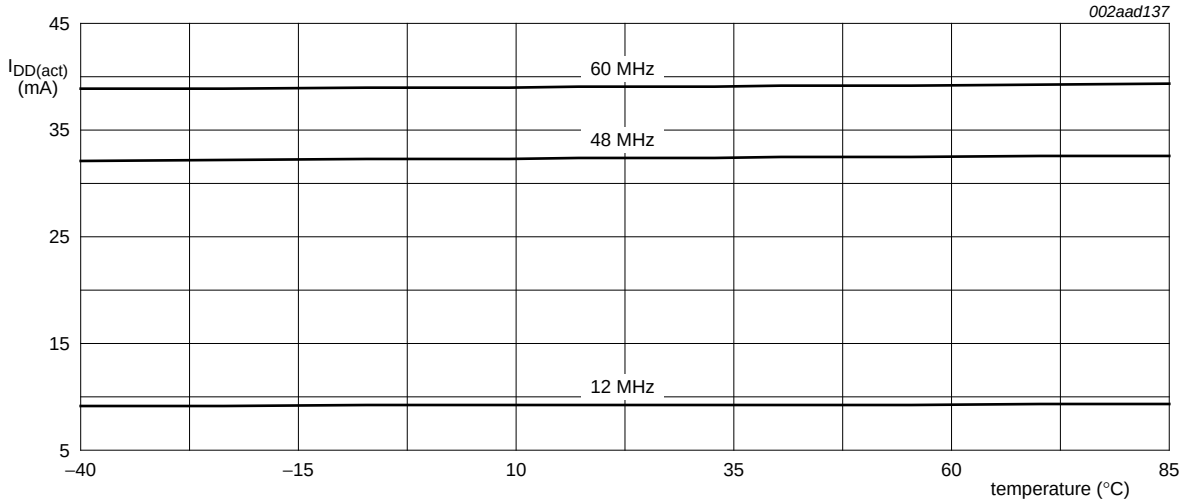
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Temp = 25 °C; core voltage 1.8 V; all peripherals disabled.

Fig 13. Typical LPC2109/01, LPC2119/01, and LPC2129/01 $I_{DD(act)}$ measured at different voltages



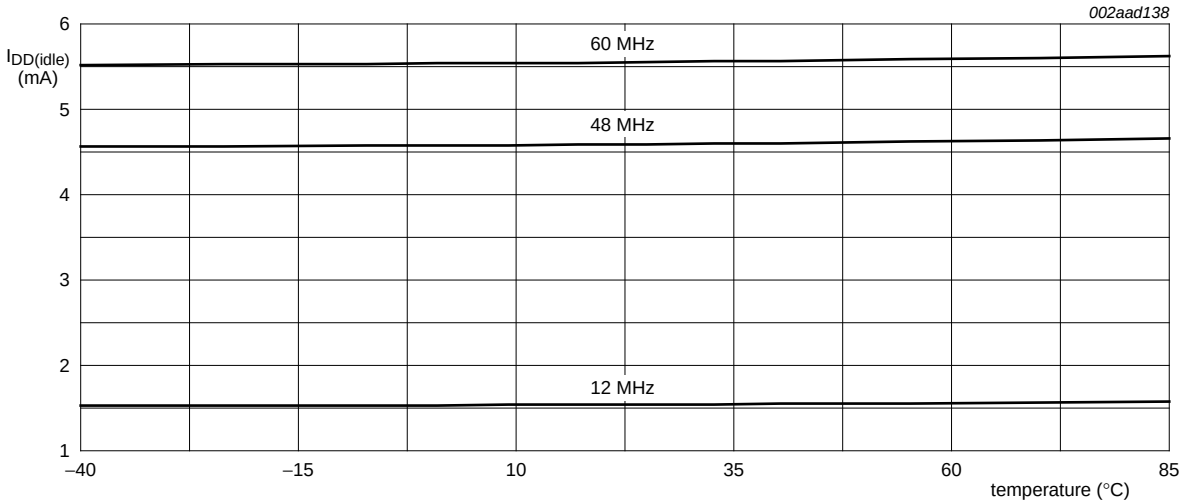
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Temp = 25 °C; core voltage 1.8 V; all peripherals disabled.

Fig 14. Typical LPC2109/01, LPC2119/01, and LPC2129/01 $I_{DD(idle)}$ measured at different voltages



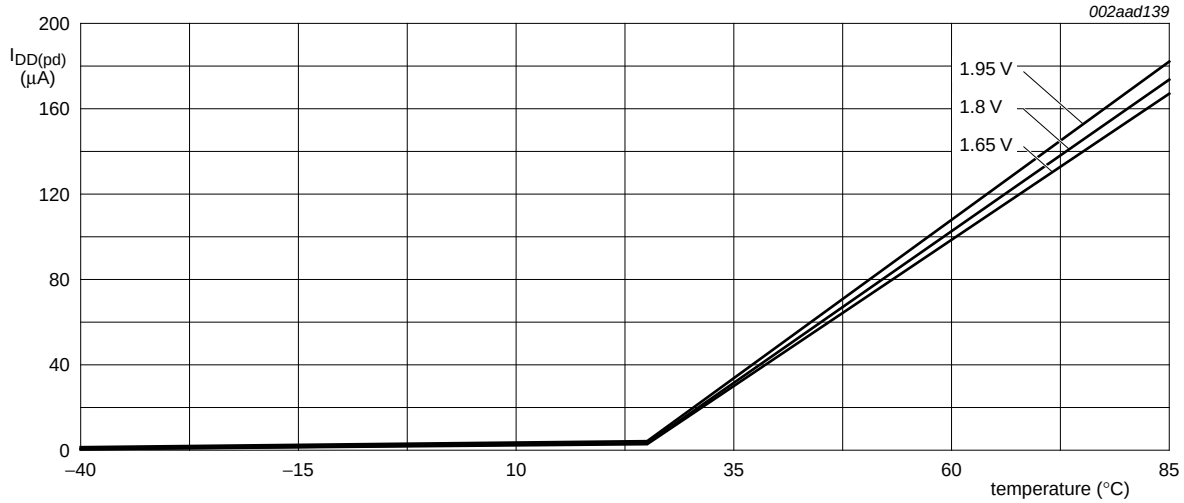
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 15. Typical LPC2109/01, LPC2119/01, and LPC2129/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 16. Typical LPC2109/01, LPC2119/01, and LPC2129/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 17. Typical LPC2109/01, LPC2119/01, and LPC2129/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 8. Typical LPC2109/01 peripheral power consumption in active mode
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in μA; PCLK = $^{CCLK}/_{4}$.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
ADC	33	128	167
CAN1	230	764	914

9. Dynamic characteristics

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

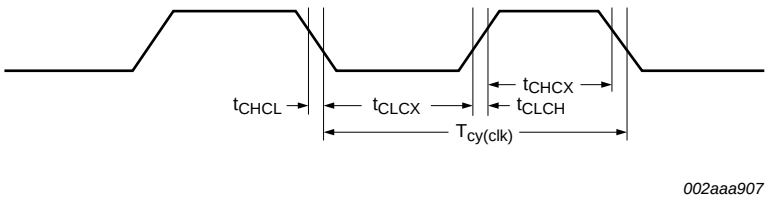


Fig 18. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2109_2119_2129 v.7	20110614	Product data sheet	201004021F	LPC2109_2119_2129 v.6
Modifications:	• Table 6 “Static characteristics”; Changed /01 Power-down mode supply current ($I_{DD(pd)}$) from 180 μA to 500 μA for industrial temperature range. • Table 6 “Static characteristics”; Moved V_{hys} voltage from typical to minimum. • Table 6 “Static characteristics”; Changed I^2C pad hysteresis from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.			
LPC2109_2119_2129 v.6	20071210	Product data sheet	-	LPC2109_2119_2129 v.5
Modifications:	• Type number LPC2109FBD64/01 has been added. • Type number LPC2119FBD64/01 has been added. • Type number LPC2129FBD64/01 has been added. • Details introduced with /01 devices on new peripherals/features (Fast I/O Ports, SSP, CRP) and enhancements to existing ones (UART0/1, Timers, ADC, and SPI) have been added. • Power measurements for LPC2109/2119/2129/01 devices have been added. • Description of JTAG pin TCK has been updated.			
LPC2109_2119_2129 v.5	20070627	Product data sheet	-	LPC2119_2129 v.4
LPC2119_2129 v.4	20060714	Product data sheet	-	LPC2119_2129 v.3
LPC2119_2129 v.3	20041222	Product data	-	LPC2119_2129 v.2
LPC2119_2129 v.2	20040202	Preliminary data	-	LPC2119_2129 v.1
LPC2119_2129 v.1	20031118	Preliminary data	-	-

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14. Contact information

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