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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	46
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2129fbd64-151

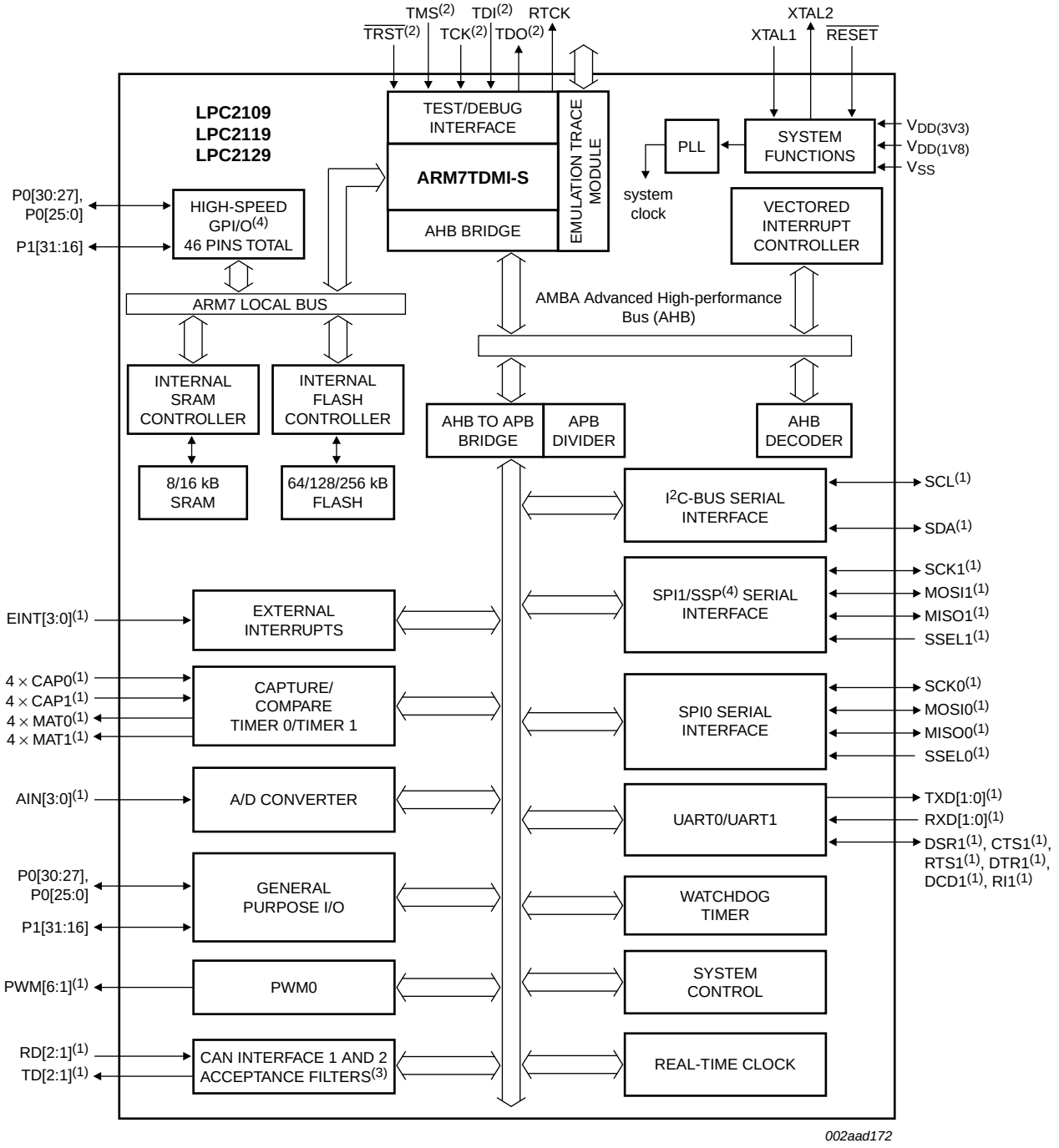
- 64/128/256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high speed 60 MHz operation.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- EmbeddedICE-RT interface enables breakpoints and watch points. Interrupt service routines can continue to execute while the foreground task is debugged with the on-chip RealMonitor software.
- Embedded Trace Macrocell (ETM) enables non-intrusive high speed real-time tracing of instruction execution.
- Two interconnected CAN interfaces (one for LPC2109) with advanced acceptance filters.
- Four-channel 10-bit A/D converter with conversion time as low as 2.44 μs.
- Multiple serial interfaces including two UARTs (16C550), Fast I^2C-bus (400 kbit/s) and two SPIs.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 μs.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC) and watchdog.
- Up to forty-six 5 V tolerant general purpose I/O pins. Up to nine edge or level sensitive external interrupt pins available.
- On-chip crystal oscillator with an operating range of 1 MHz to 30 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2109FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2119FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2129FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4. Block diagram



(1) Shared with GPIO.

(2) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(3) Only 1 for LPC2109.

(4) SSP interface and high-speed GPIO are available on LPC2109/01, LPC2119/01, and LPC2129/01 only.

Fig 1. Block diagram

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
$V_{DDA(1V8)}$	63	I	Analog 1.8 V core power supply; this is the power supply voltage for internal circuitry. This should be nominally the same voltage as $V_{DD(1V8)}$ but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	23, 43, 51	I	3.3 V pad power supply; this is the power supply voltage for the I/O ports.
$V_{DDA(3V3)}$	7	I	Analog 3.3 V pad power supply; this should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error.

[1] SSP interface available on LPC2109/01, LPC2119/01, and LPC2129/01 only.

6. Functional description

Details of the LPC2109/2119/2129 systems and peripheral functions are described in the following sections.

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2109/2119/2129 incorporate a 64/128/256 kB flash memory system, respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 60/120/248 kB of flash memory is available for user code.

The LPC2109/2119/2129 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.60) provides Code Read Protection (CRP) for the LPC2109/2119/2129 on-chip flash memory. When the CRP is enabled, the JTAG debug port and ISP commands accessing either the on-chip RAM or flash memory are disabled.

6.8 10-bit ADC

The LPC2109/2119/2129 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.8.2 ADC features available in LPC2109/2119/2129/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.9 CAN controllers and acceptance filter

The LPC2119 and LPC2129 each contain two CAN controllers, while the LPC2109 has one CAN controller. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low-cost multiplex wiring.

6.9.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0 B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit Rx identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

6.10 UARTs

The LPC2109/2119/2129 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.

- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.10.2 UART features available in LPC2109/2119/2129/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2109/2119/2129/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.11 I^2C-bus serial I/O controller

The I^2C-bus is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus; it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2109/2119/2129 supports a bit rate up to 400 kbit/s (Fast I^2C-bus).

6.11.1 Features

- Standard I^2C-bus compliant interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Timer or external event counter operation
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.14.2 Features available in LPC2109/2119/2129/01 only

The LPC2109/2119/2129/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer’s capture inputs can be selected as the timer’s clock. The rate of such a clock is limited to PCLK / 4. Duration of HIGH/LOW levels on the selected CAPn input cannot be shorter than 1 / (2PCLK).

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.

- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable reference clock divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2109/2119/2129. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Devices without the suffix /00 or /01 have only a security level equivalent to CRP2 available.

6.18.5 External interrupt inputs

The LPC2109/2119/2129 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.18.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip SRAM. This allows code running in different memory spaces to have control of the interrupts.

6.18.7 Power control

The LPC2109/2119/2129 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2109/2119/2129 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

8. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I$ < 5 V	[9]	0	0	0	μA

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Power consumption LPC2109/00, LPC2119, LPC2119/00, LPC2129, LPC2129/00							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	60	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	μA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	μA
Power consumption LPC2109/01, LPC2119/01, LPC2129/01							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	41.5	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	9	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	μA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	μA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	μA
		V_I = 5 V		-	10	22	μA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

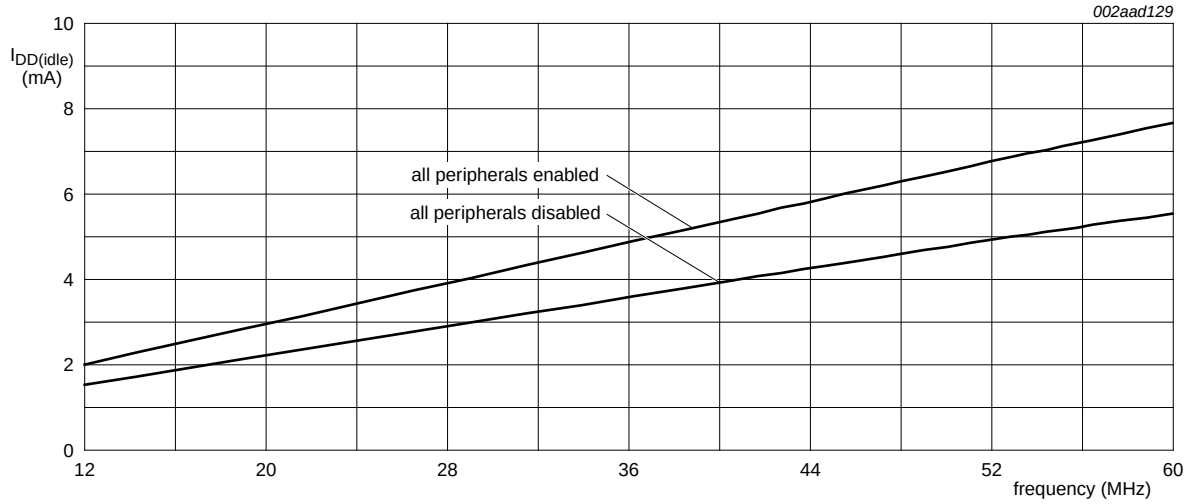
[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

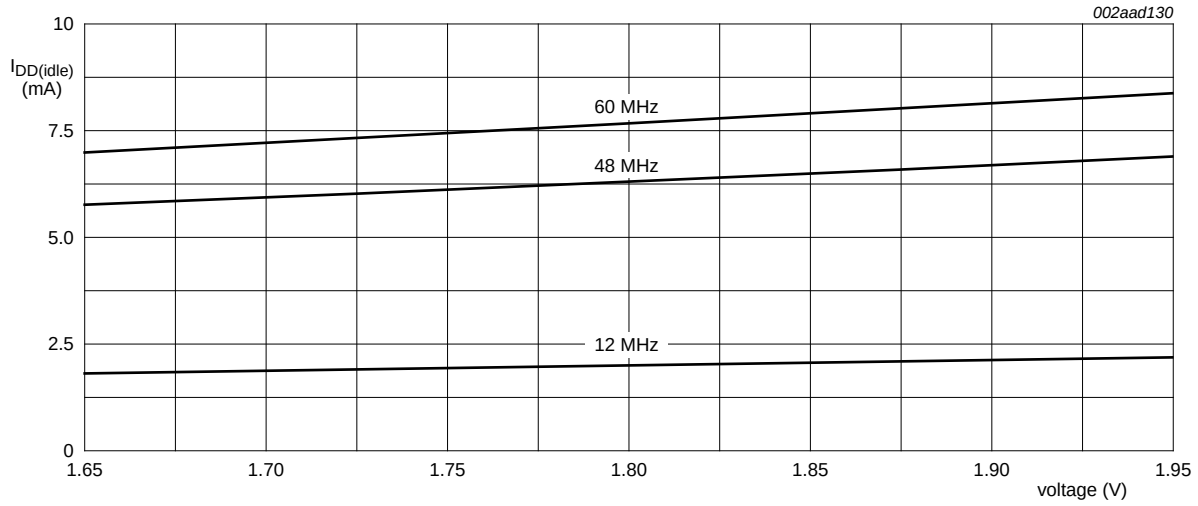
[11] See *LPC2119/2129/2194/2292/2294 User Manual*.

[12] To V_{SS}.



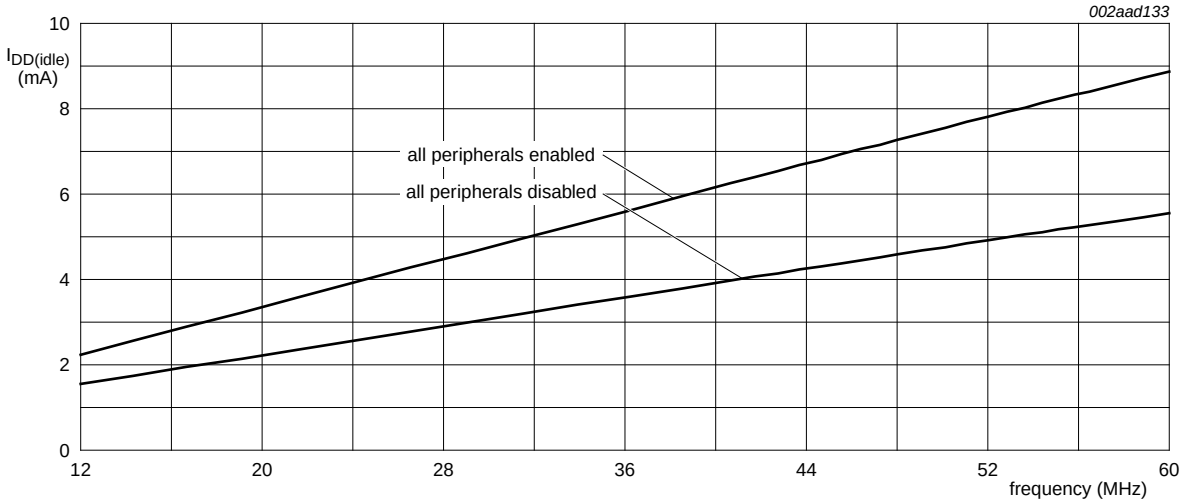
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 7. Typical LPC2109/01 $I_{DD(idle)}$ measured at different frequencies



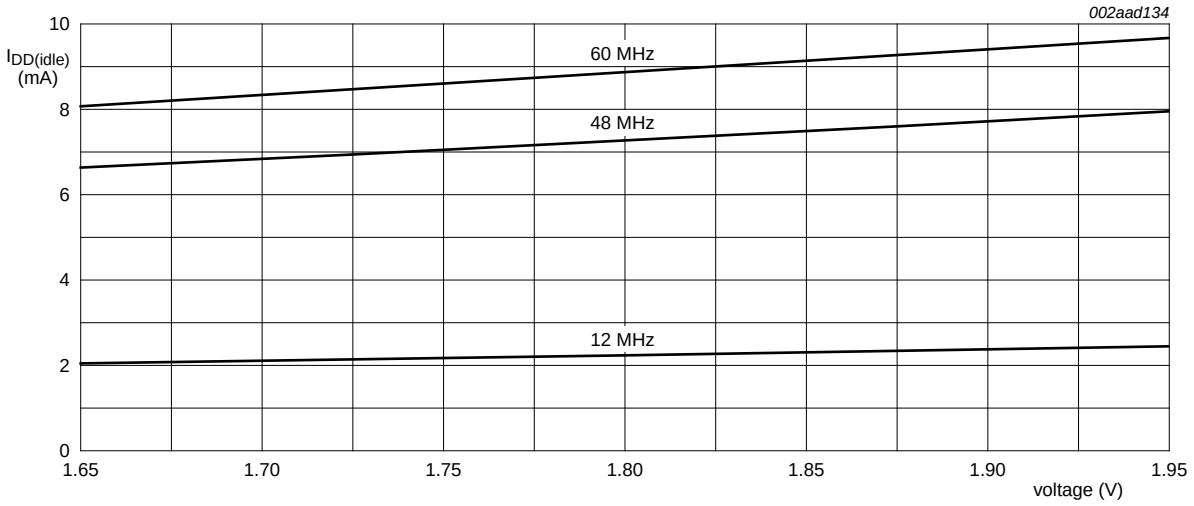
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V; all peripherals enabled.

Fig 8. Typical LPC2109/01 $I_{DD(idle)}$ measured at different voltages



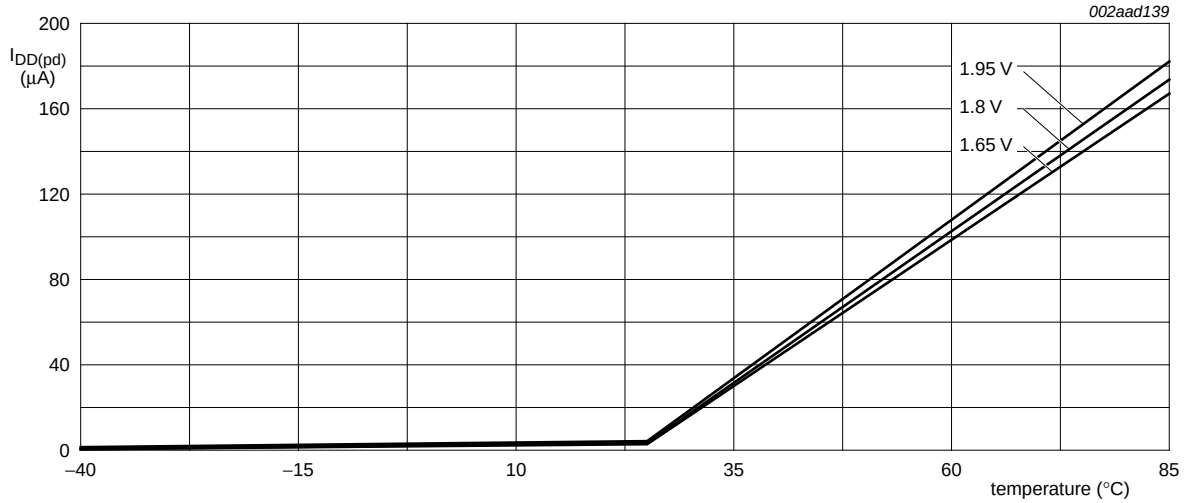
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 11. Typical LPC2119/01 and LPC2129/01 $I_{DD(idle)}$ measured at different frequencies



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V; all peripherals enabled.

Fig 12. Typical LPC2119/01 and LPC2129/01 $I_{DD(idle)}$ measured at different voltages



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 17. Typical LPC2109/01, LPC2119/01, and LPC2129/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 8. Typical LPC2109/01 peripheral power consumption in active mode
Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in μA; PCLK = $^{CCLK}/_{4}$.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421
PWM0	103	341	407
I^2C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
ADC	33	128	167
CAN1	230	764	914

9. Dynamic characteristics

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I/O	Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

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