Lattice Semiconductor Corporation - ISPLSI 5512VA-110LB388 Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	8.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	24000
Number of I/O	288
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-5512va-110lb388

ispLSI 5000V Description (Continued)

five extra product terms are used for shared GLB controls, set, reset, clock, clock enable and output enable.

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, which can be fed back through the Global Routing Pool. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of this feature to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flip flop.

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one line from each macrocell output and one line from each I/O pin.

The input buffer threshold has programmable TTL/3.3V/2.5V compatible levels. The output driver can source 4mA and sink 8mA in 3.3V mode. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows the output drivers to drive either 3.3V or 2.5V output levels while the device logic and the output current drive is always powered from 3.3V. The output drivers also provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device.

The ispLSI 5000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 5000V Family Members

The ispLSI 5000V Family ranges from 256 macrocells to 512 macrocells and operates from a 3.3V power supply. All family members will be available with multiple package options. The ispLSI 5000V Family device matrix showing the various bondout options is shown in the table below.

The interconnect structure (GRP) is very similar to Lattice's existing ispLSI 1000, 2000 and 3000 families, but with an enhanced interconnect structure for optimal pin locking and logic routing. This eliminates the need for registered I/O cells or an Output Routing Pool.

Table 1. ispLSI 5000VA Family

			Package Type			
Device	**GLBs**	**Macrocells**	**208 fpBGA**	**208 PQFP**	**272 BGA**	**388 BGA**
ispLSI 5256VA	8	256	144 I/O	144 I/O	192 I/O	—
ispLSI 5384VA	12	384	144 I/O	144 I/O	192 I/O	288 I/O
ispLSI 5512VA	16	512	—	144 I/O	192 I/O	288 I/O

Figure 2. ispLSI 5512VA Block Diagram (288 I/O Version)

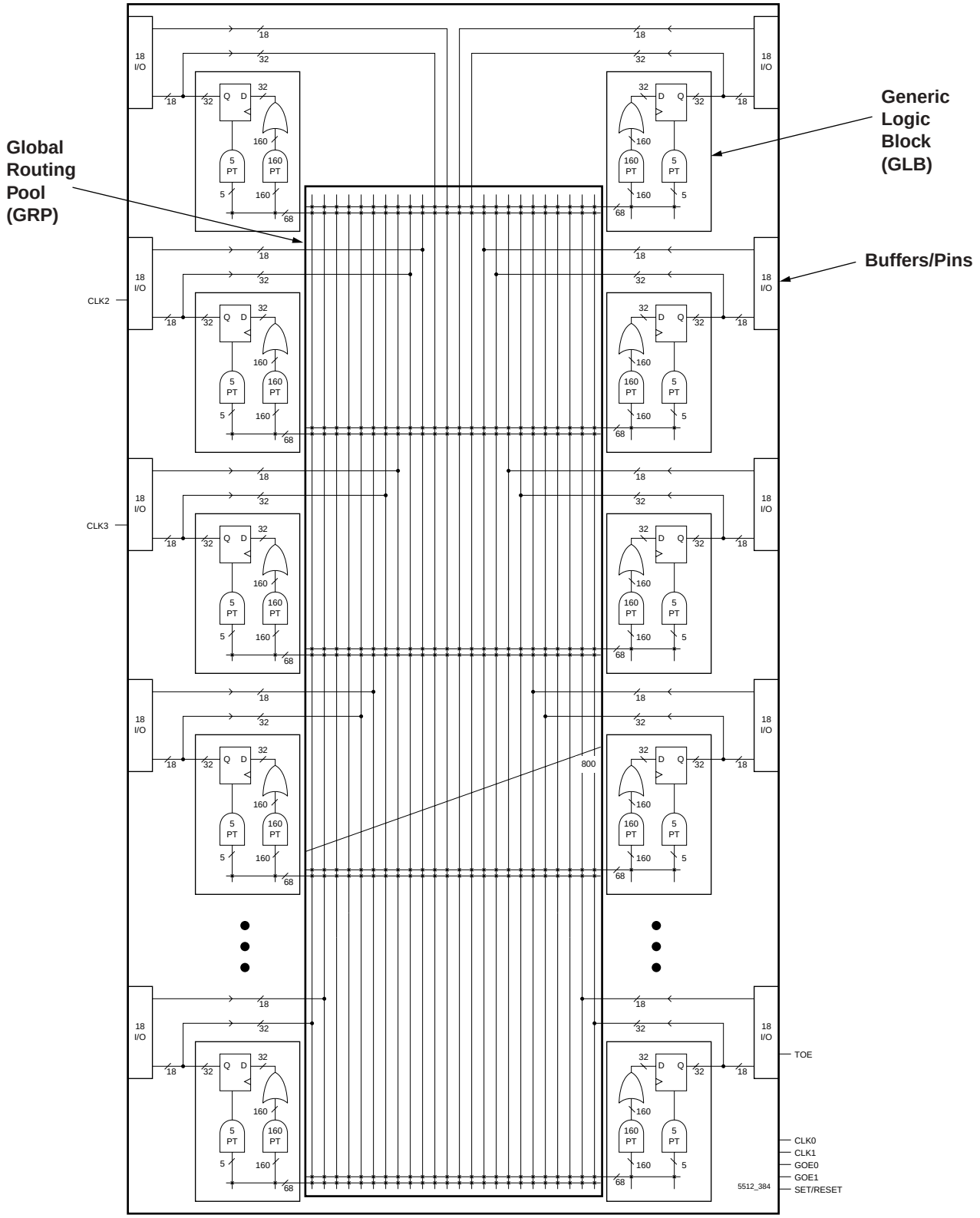
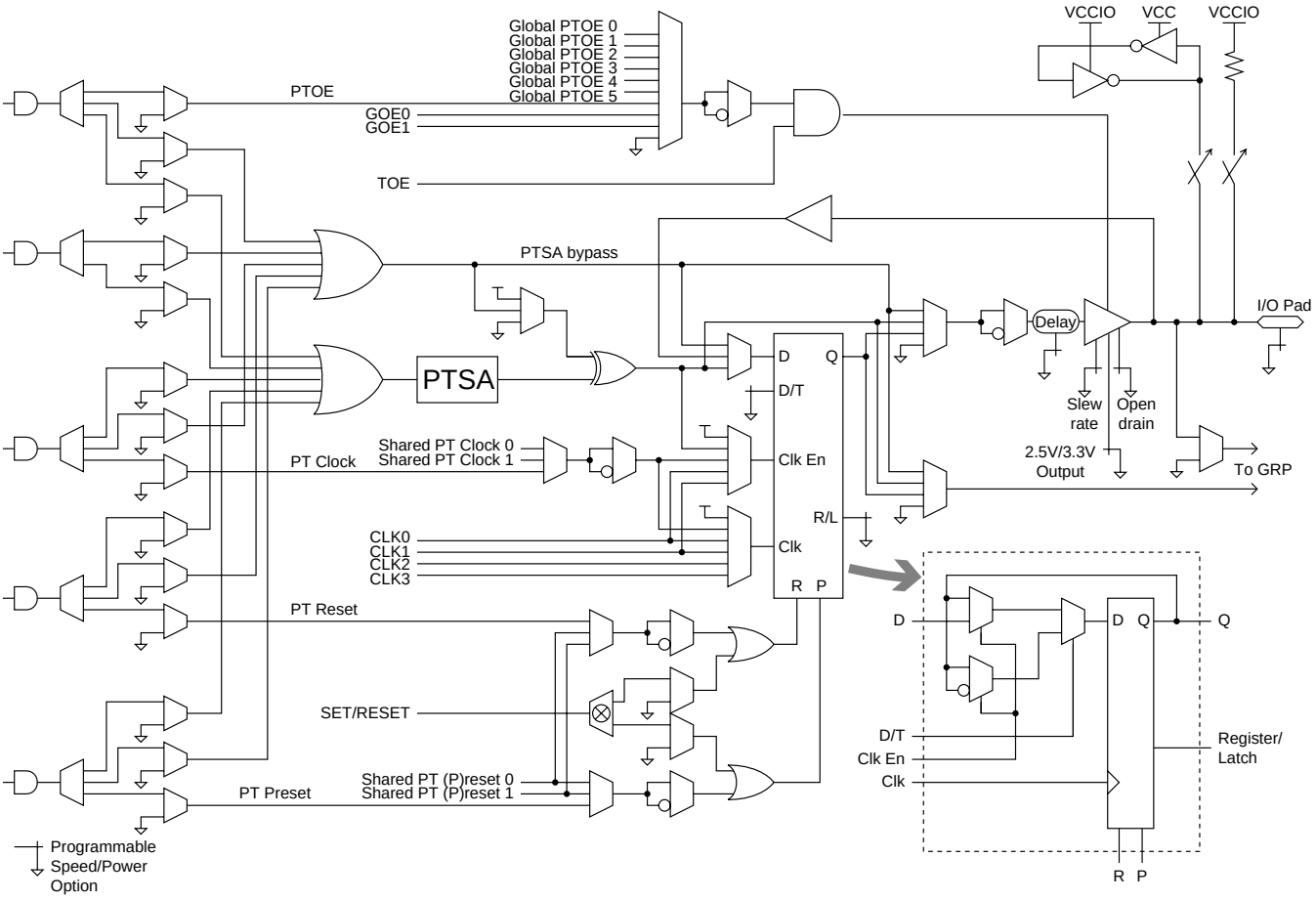


Figure 4. ispLSI 5000V Macrocell



Global Clock Distribution

The ispLSI 5000V Family has four dedicated clock input pins: CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but also is available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

Figure 5. ispLSI 5000V Global Clock Structure

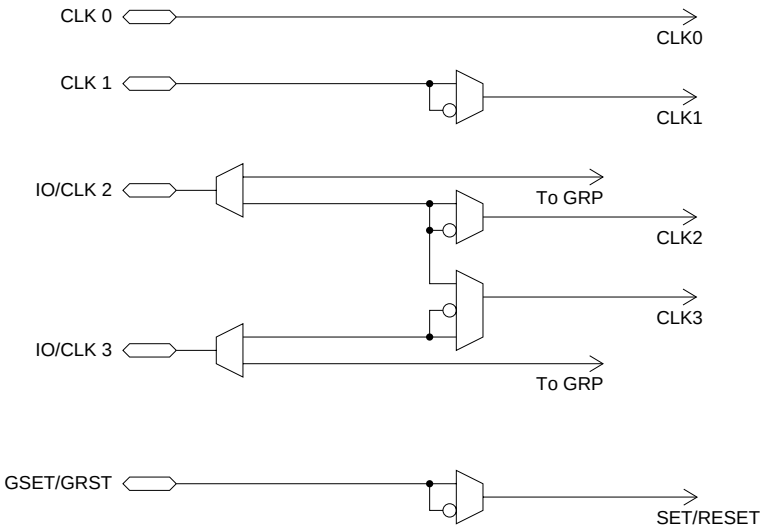


Figure 6. Boundary Scan Register Circuit for I/O Pins

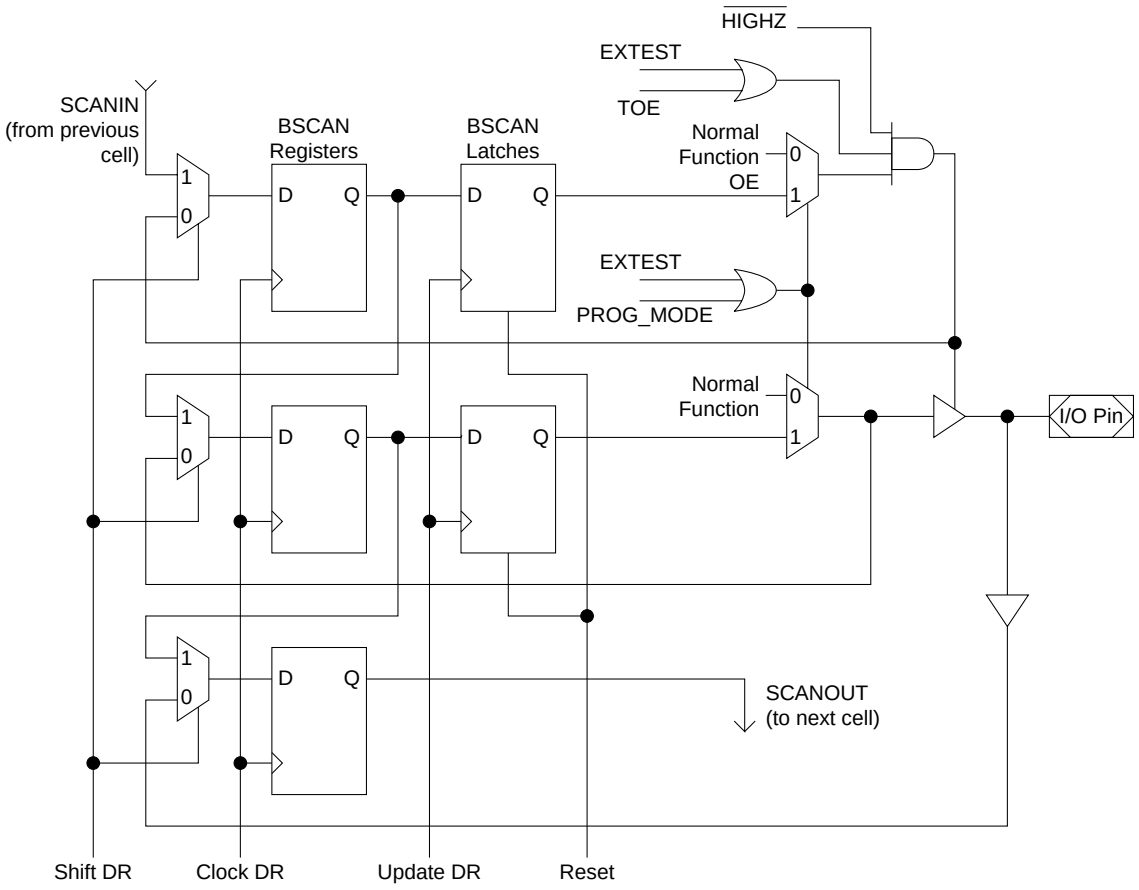
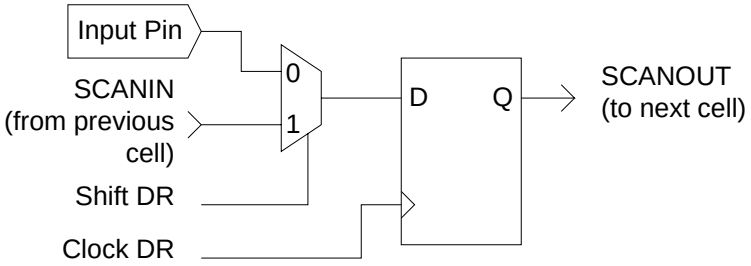


Figure 7. Boundary Scan Register Circuit for Input-Only Pins



Absolute Maximum Ratings [1, 2]

Supply Voltage V_{CC} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Tri-Stated Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	3.00	3.60	V
		Industrial	T_A = -40°C to +85°C	3.00	3.60	V
V_{CCIO}	I/O Reference Voltage			2.3	3.60	V

Table 2 - 0005/5000

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	10	pf	V_{CC} = 3.3V, V_{CK} = 2.0V
C_3	Global Input Capacitance	10	pf	V_{CC} = 3.3V, V_G = 2.0V

Table 2 - 0006/5384

Erase Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3320

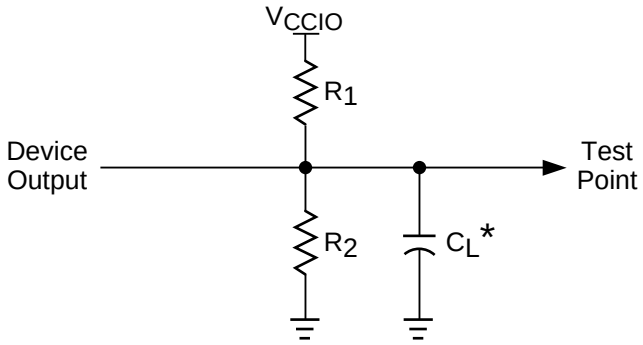
Switching Test Conditions

Input Pulse Levels	GND to $V_{CCIO_{min}}$
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure

Table 2 - 0003/5384

3-state levels are measured 0.5V from steady-state active level.

Figure 9. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213D

Output Load Conditions (See Figure 8)

		3.3V		2.5V		
TEST CONDITION		**R1**	**R2**	**R1**	**R2**	**CL**
A		316Ω	348Ω	511Ω	475Ω	35pF
B	Active High	∞	348Ω	∞	475Ω	35pF
	Active Low	316Ω	∞	511Ω	∞	35pF
C	Active High to Z at V_{OH}-0.5V	∞	348Ω	∞	475Ω	5pF
	Active Low to Z at V_{OL}+0.5V	316Ω	∞	511Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2 - 0004A/5384

DC Electrical Characteristics for 3.3V Range[1]

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage		3.0	–	3.6	V
V_{IL}	Input Low Voltage	$V_{OH} \le V_{OUT}$ or $V_{OUT} \le V_{OL\ (max)}$	-0.3	–	0.8	V
V_{IH}	Input High Voltage	$V_{OH} \le V_{OUT}$ or $V_{OUT} \le V_{OL\ (max)}$	2.0	–	5.25	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V

Table 2-0007/5512VA

1. I/O voltage configuration must be set to VCC.

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST[3] COND.	#	DESCRIPTION [4,5]	-110		-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1[6]	A	1	Data Prop. Delay, 5PT Bypass	—	8.5	—	10	—	15	ns
tpd2[6]	A	2	Data Propagation Delay	—	10	—	13	—	19	ns
fmax	A	3	Clock Frequency with Internal Feedback[1]	110	—	100	—	70	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	91	—	69	—	45	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[2]	143	—	125	—	83	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clk, 5PT bypass	6	—	8	—	12	—	ns
tco1[6]	A	7	GLB Reg. Clock to Output Delay	—	4	—	5.5	—	8	ns
th1	—	8	GLB Reg. Hold Time after Clock, 5PT bypass	0	—	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	7	—	9	—	14	—	ns
th2	—	10	GLB Reg. Hold Time after Clock	0	—	0	—	0	—	ns
tsu3 (CLK0/1)	—	11	GLB Reg. Setup Time before Clock, Input Reg. Path (CLK0/1)	4.5	—	6	—	9	—	ns
tsu3 (CLK2/3)	—	12	GLB Reg. Setup Time before Clock, Input Reg. Path (CLK2/3)	3.5	—	5	—	7	—	ns
th3 (CLK0/1)	—	13	GLB Reg. Hold Time after Clock, Input Reg. Path (CLK0/1)	0	—	0	—	0	—	ns
th3 (CLK2/3)	—	14	GLB Reg. Hold Time after Clock, Input Reg. Path (CLK2/3)	0	—	0	—	0	—	ns
tr1	A	15	Ext. Reset Pin to Output Delay	—	17	—	20	—	30	ns
trw1	—	16	Ext. Reset Pulse Duration	7.5	—	9	—	14	—	ns
tptoe/dis	B/C	17	Local Product Term Output Enable/Disable	—	10	—	12	—	18	ns
tgptoe/dis	B/C	18	Global Product Term Output Enable/Disable	—	20	—	24	—	30	ns
tgoe/dis	B/C	19	Global OE Input to Output Enable/Disable	—	6.5	—	8	—	12	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	3.5	—	4	—	6	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	3.5	—	4	—	6	—	ns

1. Standard 32-bit counter using GRP feedback.
2. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
3. Reference Switching Test Conditions section.
4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, and CLK0.
5. Timing parameters measured using normal active output driver.
6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

Timing Ext.5512VA/4.0.eps

Internal Timing Parameters[1]

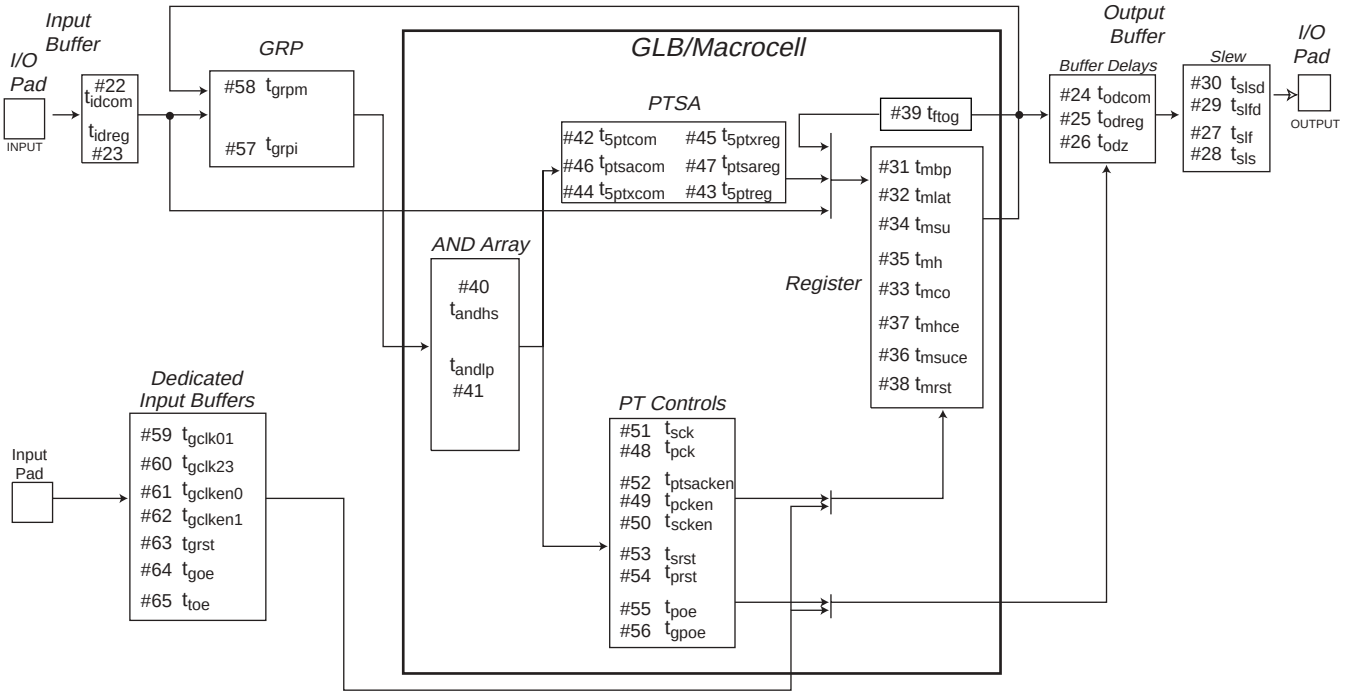
Over Recommended Operating Conditions

PARAM	#[2]	DESCRIPTION	-110		-100		-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
GRP									
tgrpi	57	GRP Delay from I/O Pad	–	1.5	–	2	–	3	ns
tgrpm	58	GRP Delay from Macrocell	–	1.2	–	1.2	–	1.2	ns
Global Control Delays									
tgclk01	59	Global Clock 0 or 1 Delay	–	1.2	–	1.7	–	2.4	ns
tgclk23	60	Global Clock 2 or 3 Delay	–	2.2	–	2.7	–	4.4	ns
tgclken0	61	Global CLKEN 0 Delay	–	1.7	–	2.4	–	3.4	ns
tgclken1	62	Global CLKEN 1 Delay	–	2.7	–	3.4	–	5.4	ns
tgrst	63	Global Set/Reset Delay	–	14.2	–	15.8	–	23.4	ns
tgoe	64	Global OE Delay	–	4.8	–	6.3	–	9.4	ns
ttoe	65	Test OE Delay	–	4.7	–	6.2	–	9.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
Refer to Timing Model in this data sheet for further details.

Timing Rev 4.0

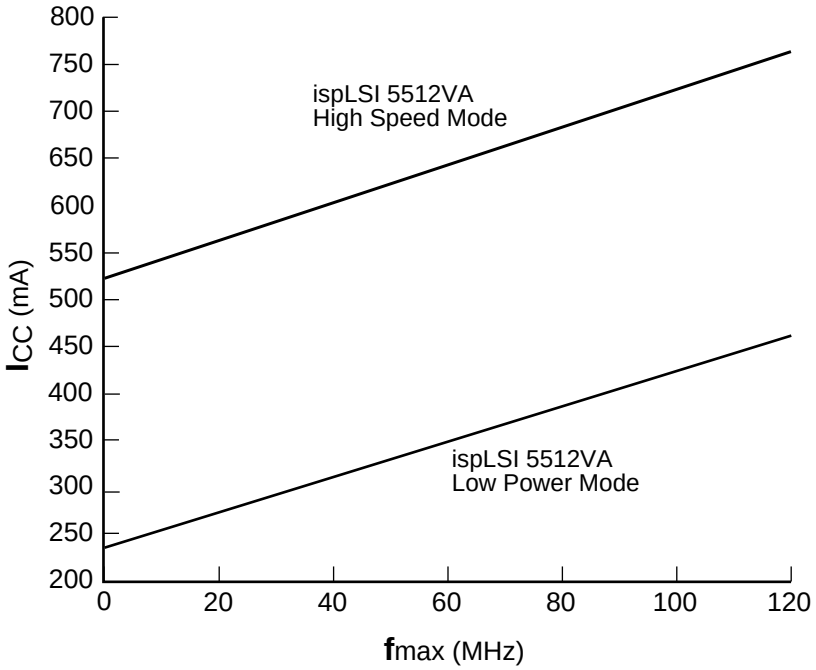
ispLSI 5512VA Timing Model



Power Consumption

Power consumption in the ispLSI 5512VA device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts on the complete group of four. The fast "high-speed" setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower "low-power" setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 32 16-bit Counters
Typical Current at 3.3V, 25° C

I_{CC} can be estimated for the ispLSI 5512VA using the following equation:

High Speed Mode: ICC = 70 + (# of PTs * 0.4592) + (# of nets * Max. freq * 0.00391)
Low Power Mode: ICC = 70 + (# of PTs * 0.160) + (# of nets * Max. freq * 0.00391)
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 3.3V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/5512va

Signal Descriptions

Signal Name	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the JTAG state machine.
TCK	Input - This pin is the Test Clock input pin used to clock through the JTAG state machine.
TDI	Input - This pin is the JTAG Test Data In pin used to load data.
TDO	Output - This pin is the JTAG Test Data Out pin used to shift data out.
TOE / I/O0	Input/Output - This pin functions as either the Test Output Enable pin or an I/O pin based upon customer's design. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
GSET/GRST	Dedicated Set/Reset Input - This pin is available to all registers in the device and can independently be configured as preset, reset or no effect on each register. The global polarity (active high or low input) for this pin is also selectable.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
GND	Ground
NC[1]	No connect.
VCC	Vcc
CLK0, CLK1	Dedicated clock inputs for all registers. Both clocks are muxed before being used as the clock input to all registers in the device.
CLK2 / I/O, CLK3 / I/O	Input/Output - These pins function as either dedicated clock inputs for all registers or an I/O pin based upon customer's design. Both clocks are muxed before being used as the clock input to all registers in the device.
VCCIO	Input - This pin is used if an optional 2.5V output is to be used. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the Vcc supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.

1. NC pins are not to be connected to any active signals, VCC or GND.

388-Ball BGA Signal Locations

Signal	Ball
GOE0, GOE1	AF14, AD13
TOE / I/O0	T1
GSET/GRST	L25
TCK	T2
TDI	R3
TDO	N24
TMS	R1
CLK0, CLK1	A13, C14
CLK2 / I/O179	A23
CLK3 / I/O197	B17
VCCIO	M26
GND	A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D19, D23, H4, J23, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N4, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, P23, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V4, W23, AC4, AC8, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26
VCC	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21
NC[1]	C9, D2, E24, L1, AC25, AF19

1. NCs are not to be connected to any active signals, VCC or GND.

388-Ball BGA I/O Locations (Sorted by I/O)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	T1	48	AC9	96	AE23	144	M24	192	D18	240	B4
1	R4	49	AF8	97	AC22	145	L26	193	A19	241	D5
2	U2	50	AD8	98	AF23	146	M23	194	C19	242	A4
3	T3	51	AE9	99	AD22	147	K25	195	B18	243	C5
4	U1	52	AF9	100	AE24	148	L24	196	A18	244	B3
5	U4	53	AE10	101	AD23	149	K26	197*	B17	245	C4
6	V2	54	AD9	102	AF24	150	K23	198	C18	246	A3
7	U3	55	AF10	103	AE26	151	J25	199	A17	247	B1
8	V1	56	AC10	104	AD25	152	K24	200	D17	248	C2
9	W2	57	AE11	105	AD26	153	J26	201	B16	249	C1
10	W1	58	AD10	106	AC24	154	H25	202	C17	250	D3
11	V3	59	AF11	107	AC26	155	H26	203	A16	251	D1
12	Y2	60	AE12	108	AB25	156	J24	204	B15	252	E2
13	W4	61	AF12	109	AB23	157	G25	205	A15	253	E4
14	Y1	62	AD11	110	AB24	158	H23	206	C16	254	E3
15	W3	63	AE13	111	AB26	159	G26	207	B14	255	E1
16	AA2	64	AC12	112	AA25	160	H24	208	D15	256	F2
17	Y4	65	AF13	113	Y23	161	F25	209	A14	257	G4
18	AA1	66	AD12	114	AA24	162	G23	210	C15	258	F3
19	Y3	67	AE14	115	AA26	163	F26	211	B13	259	F1
20	AB2	68	AC14	116	Y25	164	G24	212	D13	260	G2
21	AB1	69	AE15	117	Y26	165	E25	213	B12	261	G1
22	AA3	70	AD14	118	Y24	166	E26	214	C13	262	G3
23	AC2	71	AF15	119	W25	167	F24	215	A12	263	H2
24	AB4	72	AE16	120	V23	168	D25	216	B11	264	J4
25	AC1	73	AD15	121	W26	169	E23	217	C12	265	H1
26	AB3	74	AF16	122	W24	170	D26	218	A11	266	H3
27	AD2	75	AC15	123	V25	171	C25	219	D12	267	J2
28	AC3	76	AE17	124	V26	172	D24	220	B10	268	J1
29	AD1	77	AD16	125	U25	173	C26	221	C11	269	K2
30	AF2	78	AF17	126	V24	174	A25	222	A10	270	J3
31	AE3	79	AC17	127	U26	175	B24	223	D10	271	K1
32	AF3	80	AE18	128	U23	176	A24	224	B9	272	K4
33	AE4	81	AD17	129	T25	177	B23	225	C10	273	L2
34	AD4	82	AF18	130	U24	178	C23	226	A9	274	K3
35	AF4	83	AE19	131	T26	179*	A23	227	B8	275	M2
36	AE5	84	AD18	132	R25	180	B22	228	A8	276	M1
37	AC5	85	AE20	133	R26	181	D22	229	B7	277	L3
38	AD5	86	AC19	134	T24	182	C22	230	D8	278	N2
39	AF5	87	AF20	135	P25	183	A22	231	A7	279	M4
40	AE6	88	AD19	136	R23	184	B21	232	C8	280	N1
41	AC7	89	AE21	137	P26	185	D20	233	B6	281	M3
42	AD6	90	AC20	138	R24	186	C21	234	D7	282	P2
43	AF6	91	AF21	139	N25	187	A21	235	A6	283	P4
44	AE7	92	AD20	140	N23	188	B20	236	C7	284	P1
45	AF7	93	AE22	141	N26	189	A20	237	B5	285	N3
46	AD7	94	AF22	142	P24	190	C20	238	A5	286	R2
47	AE8	95	AD21	143	M25	191	B19	239	C6	287	P3

* I/O 179 is multiplexed with CLK2, I/O 197 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

Signal Locations (272-Ball BGA)

Signal	Ball
GOE0, GOE1	V11, U11
TOE / I/O 0	M2
GSET/GRST	J18
TCK	L4
TDI	M1
TDO	J20
TMS	L3
CLK0, CLK1	C10, D10
CLK2 / I/O 119	A18
CLK3 / I/O 131	B13
VCCIO	J19
GND	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17
VCC	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15
NC[1]	A17, B3, B18, B19, B20, C3, C5, C18, C19, D3, D19, E2, P19, R3, T4, T17, T20, U1, U2, U3, W1, W2, W4, W17, W19, W20, Y2, Y12, Y20

1. NCs are not to be connected to any active signals, VCC or GND.

272-Ball BGA I/O Locations (Sorted by I/O)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	M2	32	W7	64	U16	96	J17	128	B14	160	A3
1	M3	33	Y7	65	V17	97	H20	129	A14	161	D5
2	M4	34	V8	66	W18	98	H19	130	C13	162	C4
3	N1	35	W8	67	Y19	99	H18	131*	B13	163	B2
4	N2	36	Y8	68	V18	100	G20	132	A13	164	A2
5	N3	37	U9	69	V19	101	G19	133	D12	165	B1
6	P1	38	V9	70	U19	102	F20	134	C12	166	C2
7	P2	39	W9	71	U18	103	G18	135	B12	167	D2
8	R1	40	Y9	72	V20	104	F19	136	A12	168	E4
9	P3	41	W10	73	U20	105	E20	137	B11	169	C1
10	R2	42	V10	74	T18	106	G17	138	C11	170	D1
11	T1	43	Y10	75	T19	107	F18	139	A11	171	E3
12	P4	44	Y11	76	R18	108	E19	140	A10	172	E1
13	T2	45	W11	77	P17	109	D20	141	B10	173	F3
14	T3	46	W12	78	R19	110	E18	142	A9	174	G4
15	V1	47	V12	79	R20	111	C20	143	B9	175	F2
16	V2	48	U12	80	P18	112	E17	144	C9	176	F1
17	V3	49	Y13	81	P20	113	D18	145	D9	177	G3
18	Y1	50	W13	82	N18	114	A20	146	A8	178	G2
19	W3	51	V13	83	N19	115	A19	147	B8	179	G1
20	V4	52	Y14	84	N20	116	B17	148	C8	180	H3
21	U5	53	W14	85	M17	117	C17	149	A7	181	H2
22	Y3	54	Y15	86	M18	118	D16	150	B7	182	H1
23	Y4	55	V14	87	M19	119*	A18	151	A6	183	J4
24	V5	56	W15	88	M20	120	C16	152	C7	184	J3
25	W5	57	Y16	89	L19	121	B16	153	B6	185	J2
26	Y5	58	U14	90	L18	122	A16	154	A5	186	J1
27	V6	59	V15	91	L20	123	C15	155	D7	187	K2
28	U7	60	W16	92	K20	124	D14	156	C6	188	K3
29	W6	61	Y17	93	K19	125	B15	157	B5	189	K1
30	Y6	62	V16	94	K18	126	A15	158	A4	190	L1
31	V7	63	Y18	95	K17	127	C14	159	B4	191	L2

* I/O 119 is multiplexed with CLK2, I/O 131 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

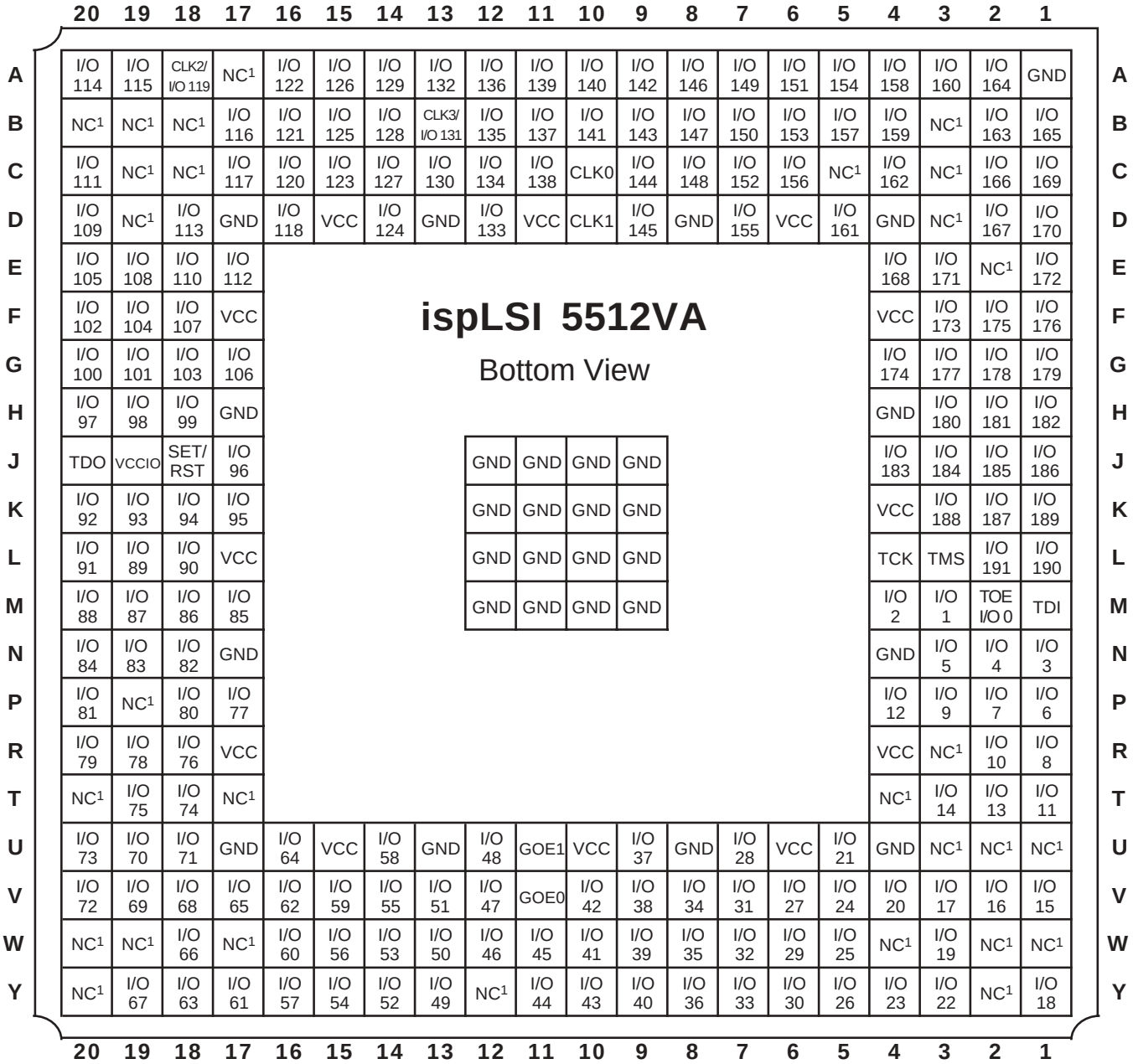
272-Ball BGA I/O Locations (Sorted by Ball)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
164	A2	121	B16	108	E19	93	K19	11	T1	72	V20
160	A3	116	B17	105	E20	92	K20	13	T2	19	W3
158	A4	169	C1	176	F1	190	L1	14	T3	25	W5
154	A5	166	C2	175	F2	191	L2	74	T18	29	W6
151	A6	162	C4	173	F3	90	L18	75	T19	32	W7
149	A7	156	C6	107	F18	89	L19	21	U5	35	W8
146	A8	152	C7	104	F19	91	L20	28	U7	39	W9
142	A9	148	C8	102	F20	0*	M2	37	U9	41	W10
140	A10	144	C9	179	G1	1	M3	48	U12	45	W11
139	A11	138	C11	178	G2	2	M4	58	U14	46	W12
136	A12	134	C12	177	G3	85	M17	64	U16	50	W13
132	A13	130	C13	174	G4	86	M18	71	U18	53	W14
129	A14	127	C14	106	G17	87	M19	70	U19	56	W15
126	A15	123	C15	103	G18	88	M20	73	U20	60	W16
122	A16	120	C16	101	G19	3	N1	15	V1	66	W18
119*	A18	117	C17	100	G20	4	N2	16	V2	18	Y1
115	A19	111	C20	182	H1	5	N3	17	V3	22	Y3
114	A20	170	D1	181	H2	82	N18	20	V4	23	Y4
165	B1	167	D2	180	H3	83	N19	24	V5	26	Y5
163	B2	161	D5	99	H18	84	N20	27	V6	30	Y6
159	B4	155	D7	98	H19	6	P1	31	V7	33	Y7
157	B5	145	D9	97	H20	7	P2	34	V8	36	Y8
153	B6	133	D12	186	J1	9	P3	38	V9	40	Y9
150	B7	124	D14	185	J2	12	P4	42	V10	43	Y10
147	B8	118	D16	184	J3	77	P17	47	V12	44	Y11
143	B9	113	D18	183	J4	80	P18	51	V13	49	Y13
141	B10	109	D20	96	J17	81	P20	55	V14	52	Y14
137	B11	172	E1	189	K1	8	R1	59	V15	54	Y15
135	B12	171	E3	187	K2	10	R2	62	V16	57	Y16
131*	B13	168	E4	188	K3	76	R18	65	V17	61	Y17
128	B14	112	E17	95	K17	78	R19	68	V18	63	Y18
125	B15	110	E18	94	K18	79	R20	69	V19	67	Y19

* I/O 119 is multiplexed with CLK2, I/O 131 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

Signal Configuration

ispLSI 5512VA 272-ball BGA



	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O 114	I/O 115	CLK2/ I/O 119	NC[1]	I/O 122	I/O 126	I/O 129	I/O 132	I/O 136	I/O 139	I/O 140	I/O 142	I/O 146	I/O 149	I/O 151	I/O 154	I/O 158	I/O 160	I/O 164	GND	A
B	NC[1]	NC[1]	NC[1]	I/O 116	I/O 121	I/O 125	I/O 128	CLK3/ I/O 131	I/O 135	I/O 137	I/O 141	I/O 143	I/O 147	I/O 150	I/O 153	I/O 157	I/O 159	NC[1]	I/O 163	I/O 165	B
C	I/O 111	NC[1]	NC[1]	I/O 117	I/O 120	I/O 123	I/O 127	I/O 130	I/O 134	I/O 138	CLK0	I/O 144	I/O 148	I/O 152	I/O 156	NC[1]	I/O 162	NC[1]	I/O 166	I/O 169	C
D	I/O 109	NC[1]	I/O 113	GND	I/O 118	VCC	I/O 124	GND	I/O 133	VCC	CLK1	I/O 145	GND	I/O 155	VCC	I/O 161	GND	NC[1]	I/O 167	I/O 170	D
E	I/O 105	I/O 108	I/O 110	I/O 112													I/O 168	I/O 171	NC[1]	I/O 172	E
F	I/O 102	I/O 104	I/O 107	VCC													VCC	I/O 173	I/O 175	I/O 176	F
G	I/O 100	I/O 101	I/O 103	I/O 106													I/O 174	I/O 177	I/O 178	I/O 179	G
H	I/O 97	I/O 98	I/O 99	GND													GND	I/O 180	I/O 181	I/O 182	H
J	TDO	VCCIO	SET/ RST	I/O 96					GND	GND	GND	GND					I/O 183	I/O 184	I/O 185	I/O 186	J
K	I/O 92	I/O 93	I/O 94	I/O 95					GND	GND	GND	GND					VCC	I/O 188	I/O 187	I/O 189	K
L	I/O 91	I/O 89	I/O 90	VCC					GND	GND	GND	GND					TCK	TMS	I/O 191	I/O 190	L
M	I/O 88	I/O 87	I/O 86	I/O 85					GND	GND	GND	GND					I/O 2	I/O 1	TOE I/O 0	TDI	M
N	I/O 84	I/O 83	I/O 82	GND													GND	I/O 5	I/O 4	I/O 3	N
P	I/O 81	NC[1]	I/O 80	I/O 77													I/O 12	I/O 9	I/O 7	I/O 6	P
R	I/O 79	I/O 78	I/O 76	VCC													VCC	NC[1]	I/O 10	I/O 8	R
T	NC[1]	I/O 75	I/O 74	NC[1]													NC[1]	I/O 14	I/O 13	I/O 11	T
U	I/O 73	I/O 70	I/O 71	GND	I/O 64	VCC	I/O 58	GND	I/O 48	GOE1	VCC	I/O 37	GND	I/O 28	VCC	I/O 21	GND	NC[1]	NC[1]	NC[1]	U
V	I/O 72	I/O 69	I/O 68	I/O 65	I/O 62	I/O 59	I/O 55	I/O 51	I/O 47	GOE0	I/O 42	I/O 38	I/O 34	I/O 31	I/O 27	I/O 24	I/O 20	I/O 17	I/O 16	I/O 15	V
W	NC[1]	NC[1]	I/O 66	NC[1]	I/O 60	I/O 56	I/O 53	I/O 50	I/O 46	I/O 45	I/O 41	I/O 39	I/O 35	I/O 32	I/O 29	I/O 25	NC[1]	I/O 19	NC[1]	NC[1]	W
Y	NC[1]	I/O 67	I/O 63	I/O 61	I/O 57	I/O 54	I/O 52	I/O 49	NC[1]	I/O 44	I/O 43	I/O 40	I/O 36	I/O 33	I/O 30	I/O 26	I/O 23	I/O 22	NC[1]	I/O 18	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

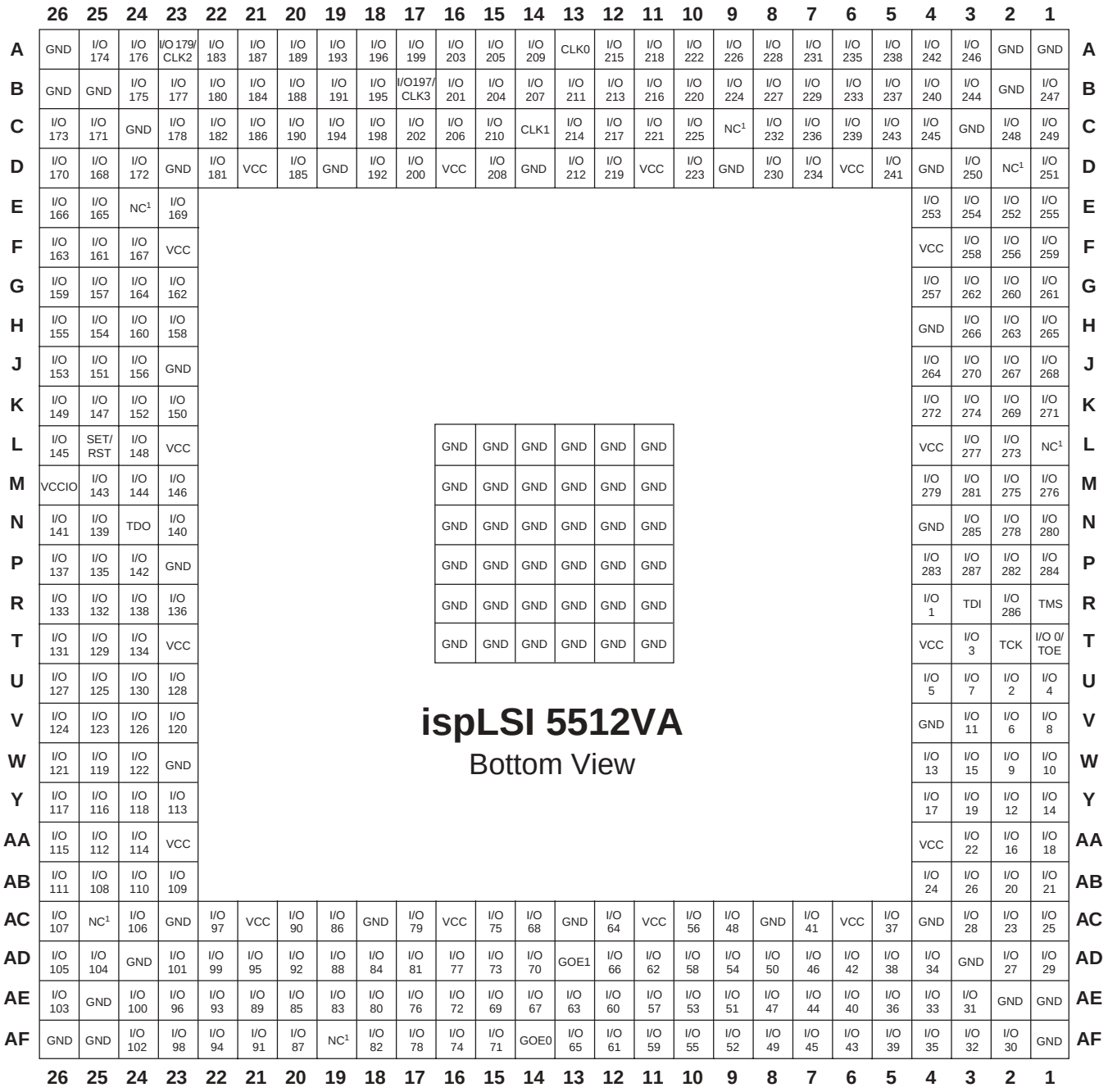
1. NCs are not to be connected to any active signals, Vcc or GND.

272 BGA/5512VA

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispLSI 5512VA 388-ball BGA



	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O 174	I/O 176	I/O 179/ CLK2	I/O 183	I/O 187	I/O 189	I/O 193	I/O 196	I/O 199	I/O 203	I/O 205	I/O 209	CLK0	I/O 215	I/O 218	I/O 222	I/O 226	I/O 228	I/O 231	I/O 235	I/O 238	I/O 242	I/O 246	GND	GND	A
B	GND	GND	I/O 175	I/O 177	I/O 180	I/O 184	I/O 188	I/O 191	I/O 195	I/O197/ CLK3	I/O 201	I/O 204	I/O 207	I/O 211	I/O 213	I/O 216	I/O 220	I/O 224	I/O 227	I/O 229	I/O 233	I/O 237	I/O 240	I/O 244	GND	I/O 247	B
C	I/O 173	I/O 171	GND	I/O 178	I/O 182	I/O 186	I/O 190	I/O 194	I/O 198	I/O 202	I/O 206	I/O 210	CLK1	I/O 214	I/O 217	I/O 221	I/O 225	NC[1]	I/O 232	I/O 236	I/O 239	I/O 243	I/O 245	GND	I/O 248	I/O 249	C
D	I/O 170	I/O 168	I/O 172	GND	I/O 181	VCC	I/O 185	GND	I/O 192	I/O 200	VCC	I/O 208	GND	I/O 212	I/O 219	VCC	I/O 223	GND	I/O 230	I/O 234	VCC	I/O 241	GND	I/O 250	NC[1]	I/O 251	D
E	I/O 166	I/O 165	NC[1]	I/O 169																			I/O 253	I/O 254	I/O 252	I/O 255	E
F	I/O 163	I/O 161	I/O 167	VCC																			VCC	I/O 258	I/O 256	I/O 259	F
G	I/O 159	I/O 157	I/O 164	I/O 162																			I/O 257	I/O 262	I/O 260	I/O 261	G
H	I/O 155	I/O 154	I/O 160	I/O 158																			GND	I/O 266	I/O 263	I/O 265	H
J	I/O 153	I/O 151	I/O 156	GND																			I/O 264	I/O 270	I/O 267	I/O 268	J
K	I/O 149	I/O 147	I/O 152	I/O 150																			I/O 272	I/O 274	I/O 269	I/O 271	K
L	I/O 145	SET/ RST	I/O 148	VCC																			VCC	I/O 277	I/O 273	NC[1]	L
M	VCCIO	I/O 143	I/O 144	I/O 146																			I/O 279	I/O 281	I/O 275	I/O 276	M
N	I/O 141	I/O 139	TDO	I/O 140																			GND	I/O 285	I/O 278	I/O 280	N
P	I/O 137	I/O 135	I/O 142	GND																			I/O 283	I/O 287	I/O 282	I/O 284	P
R	I/O 133	I/O 132	I/O 138	I/O 136																			I/O 1	TDI	I/O 286	TMS	R
T	I/O 131	I/O 129	I/O 134	VCC																			VCC	I/O 3	TCK	I/O 0/ TOE	T
U	I/O 127	I/O 125	I/O 130	I/O 128																			I/O 5	I/O 7	I/O 2	I/O 4	U
V	I/O 124	I/O 123	I/O 126	I/O 120																			GND	I/O 11	I/O 6	I/O 8	V
W	I/O 121	I/O 119	I/O 122	GND																			I/O 13	I/O 15	I/O 9	I/O 10	W
Y	I/O 117	I/O 116	I/O 118	I/O 113																			I/O 17	I/O 19	I/O 12	I/O 14	Y
AA	I/O 115	I/O 112	I/O 114	VCC																			VCC	I/O 22	I/O 16	I/O 18	AA
AB	I/O 111	I/O 108	I/O 110	I/O 109																			I/O 24	I/O 26	I/O 20	I/O 21	AB
AC	I/O 107	NC[1]	I/O 106	GND	I/O 97	VCC	I/O 90	I/O 86	GND	I/O 79	VCC	I/O 75	I/O 68	GND	I/O 64	VCC	I/O 56	I/O 48	GND	I/O 41	VCC	I/O 37	GND	I/O 28	I/O 23	I/O 25	AC
AD	I/O 105	I/O 104	GND	I/O 101	I/O 99	I/O 95	I/O 92	I/O 88	I/O 84	I/O 81	I/O 77	I/O 73	I/O 70	GOE1	I/O 66	I/O 62	I/O 58	I/O 54	I/O 50	I/O 46	I/O 42	I/O 38	I/O 34	GND	I/O 27	I/O 29	AD
AE	I/O 103	GND	I/O 100	I/O 96	I/O 93	I/O 89	I/O 85	I/O 83	I/O 80	I/O 76	I/O 72	I/O 69	I/O 67	I/O 63	I/O 60	I/O 57	I/O 53	I/O 51	I/O 47	I/O 44	I/O 40	I/O 36	I/O 33	I/O 31	GND	GND	AE
AF	GND	GND	I/O 102	I/O 98	I/O 94	I/O 91	I/O 87	NC[1]	I/O 82	I/O 78	I/O 74	I/O 71	GOE0	I/O 65	I/O 61	I/O 59	I/O 55	I/O 52	I/O 49	I/O 45	I/O 43	I/O 39	I/O 35	I/O 32	I/O 30	GND	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

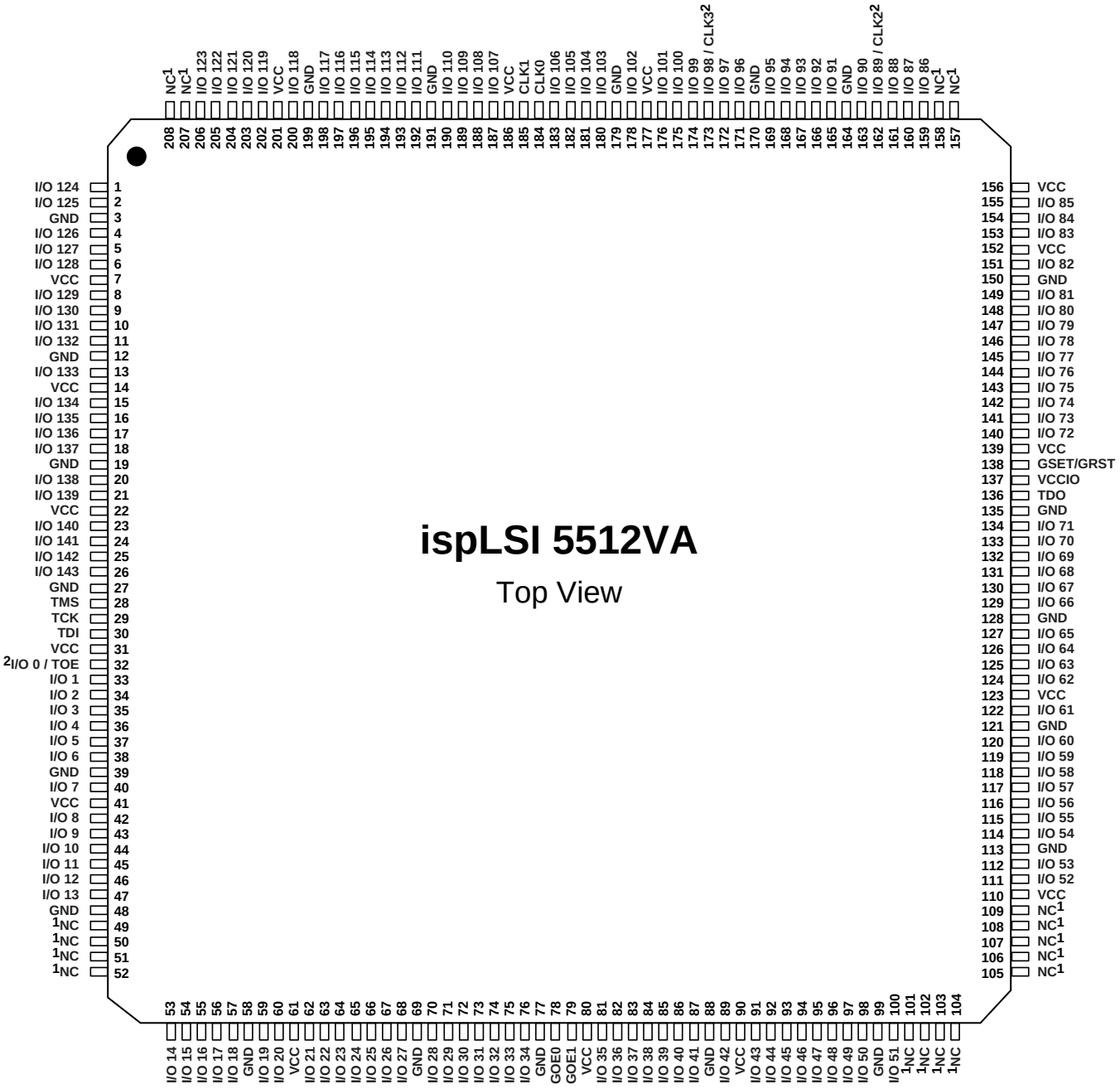
388 BGA/5512VA

1. NC pins are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Pin Configuration

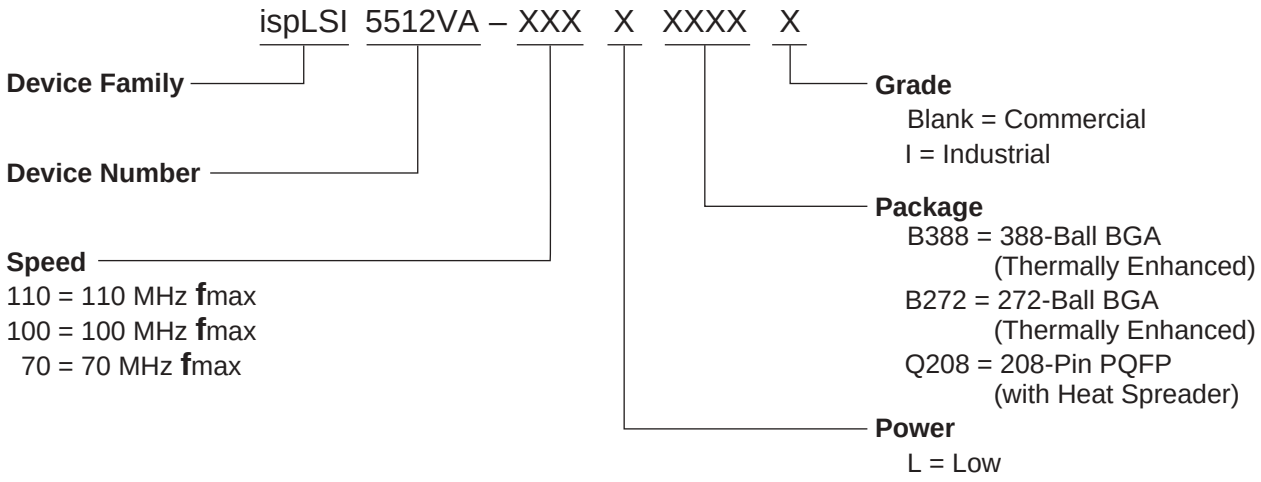
ispLSI 5512VA 208-pin PQFP (with Heat Spreader)



208-PQFP/5512VA

1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Part Number Description



0212/5512va

Ordering Information

COMMERCIAL

Family	fmax	tpd	Ordering Number	Package
ispLSI	110	8.5	ispLSI5512VA-110LB272	272-Ball BGA
	110	8.5	ispLSI 5512VA-110LB388	388-Ball BGA
	110	8.5	ispLSI 5512VA-110LQ208	208-Pin PQFP
	100	10	ispLSI 5512VA-100LB272	272-Ball BGA
	100	10	ispLSI 5512VA-100LB388	388-Ball BGA
	100	10	ispLSI 5512VA-100LQ208	208-Pin PQFP
	70	15	ispLSI 5512VA-70LB272	272-Ball BGA
	70	15	ispLSI 5512VA-70LB388	388-Ball BGA
	70	15	ispLSI 5512VA-70LQ208	208-Pin PQFP

INDUSTRIAL

Family	fmax	tpd	Ordering Number	Package
ispLSI	70	15	ispLSI 5512VA-70LB388I	388-Ball BGA