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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60Lite RISC
Core Size	32-Bit Single-Core
Speed	33MHz
Connectivity	UART/USART
Peripherals	DMA, WDT
Number of I/O	49
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f267apmc-ge1

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• Internal peripheral functions

	MB91V265A	MB91F267A	MB91F267NA	MB91267A	MB91267NA
	Evaluation product	**Flash memory product**		**MASK ROM product**	
Package	PGA-401 (Lead pitch 2.54 mm interstitial)	LQFP-64 (Lead pitch 0.65 mm)			
ROM/Flash size	External SRAM	128 Kbytes			
RAM size	24 Kbytes	4 Kbytes			
C-CAN	1 channel	No	1 channel	No	1 channel

- A/D converter (sequential comparison type)
  Resolution : 8/10 bits : 4 channels × 1 unit, 7 channels × 1 unit
  Conversion time : 1.2 μs (Minimum conversion time system clock at 33 MHz)
  1.35 μs (Minimum conversion time system clock at 20 MHz)
- External interrupt input : 8 channels
- Bit search module (for REALOS)
  Function for searching the MSB (upper bit) in each word for the first 1-to-0 inverted bit position
- C-CAN 32MSB : 1 channel (loaded in MB91267NA/F267NA)
- UART (Full-duplex double buffer) : 2 channels
  Selectable parity On/Off
  Asynchronous (start-stop synchronized) or clock-synchronous communications selectable
  Internal timer for dedicated baud rate (U-TIMER) on each channel
  External clock can be used as transfer clock
  Error detection function for parity, frame, and overrun errors
- 8/16-bit PPG timer : 8 channels (at 8-bit) / 4 channels (at 16-bit)
- Timing generator
- 16-bit reload timer : 3 channels (with cascade mode, without output of reload timer 0)
- 16-bit free-run timer : 3 channels
- 16-bit PWC timer : 1 channel
- Input capture : 4 channels (interface with free-run timer)
- Output compare : 6 channels (interface with free-run timer)
- Waveform generator
  Various waveforms which are generated by using output compare, 16-bit PPG timer 0, and 16-bit dead timer
- SUM of products macro
  RAM : instruction RAM (I-RAM) 256 × 16-bit
  coefficient RAM (X-RAM) 64 × 16-bit
  variable RAM (Y-RAM) 64 × 16-bit
  Execution of 1 cycle MAC (16-bit × 16-bit + 40 bits)
  Operation results are extracted rounded from 40 to 16 bits
- DMAC (DMA Controller) : 5 channels
  Operation of transfer and activation by internal peripheral interrupts and software
- Watchdog timer
- Low-power consumption mode
  Sleep/stop function
- Package : LQFP-64
- Technology : CMOS 0.35 μm
- Power supply : 1-power supply (Vcc = 4.0 V to 5.5 V)

Pin no.	Pin name	I/O Circuit type*1	Description
32	INT6	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	PPG5		Output terminal of PPG timer 5. This function becomes valid when output of PPG timer 5 is set to enabled.
	RX0		RX0 input terminal of C-CAN0 (MB91267NA/F267NA) . Since this input is used as required while the RX0 input is enabled, port output must remain off unless intentionally used.
	P16		General purpose input/output port. This function becomes valid when output of PPG timer 5 and RX0 input*2 of C-CAN0 are set to disabled.
33	PPG6	D	Output terminal of PPG timer 6. This function becomes valid when output of PPG timer 6 is set to enabled.
	TX0		TX0 output terminal of C-CAN0 (MB91267NA/F267NA) . This function becomes valid when TX0 output of C-CAN0 is set to enabled.
	P17		General purpose input/output port. This function becomes valid when output of PPG timer 6 and TX0 output*2 of C-CAN0 are set to disabled.
34	ADTG1	D	External trigger input terminal of A/D converter 1. Since this input is used as required while it selects as A/D activation trigger cause, the port output must remain off unless intentionally used.
	IC2		Trigger input terminal of input capture 2. The port can serve as an input when set for input with the setting of the input capture trigger input. When the port is used for input capture input, this input is used as required. The port output must therefore remain off unless intentionally used.
	P20		General purpose input/output port. This function becomes valid when the setting of the external trigger input of A/D converter 1 or the setting of the input capture trigger input is set to disabled.
35	ADTG2	D	External trigger input terminal of A/D converter 2. Since this input is used as required while it selects as A/D activation trigger cause, the port output must remain off unless intentionally used.
	IC3		Trigger input terminal of input capture 3. The port can serve as an input when set for input with the setting of the input capture trigger input. When the port is used for input capture input, this input is used as required. The port output must therefore remain off unless intentionally used.
	P21		General purpose input/output port. This function becomes valid when the setting of the external trigger input of A/D converter 2 or the setting of the input capture trigger input is set to disabled.
36	PWI0	D	Pulse width counter input of PWC timer 0 This function becomes valid when pulse width counter input of PWC timer 0 is set to enabled.
	P22		General purpose input/output port. This function becomes valid when pulse width counter input of PWC timer 0 is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
50	INT7	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	PPG7		Output terminal of PPG timer 7. This function becomes valid when output of PPG timer 7 is set to enabled.
	P36		General purpose input/output port. This function becomes valid when output of PPG timer 7 is set to disabled.
51	$\overline{\text{INIT}}$	I	External reset input terminal.
52	RTO5	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P35		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
53	RTO4	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P34		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
54	RTO3	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P33		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
55	RTO2	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P32		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
56	RTO1	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P31		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
57	RTO0	J	Waveform generator output terminal of multi-function timer. This terminal outputs waveform set at the waveform generator. This function becomes valid when waveform generator output of multi-function timer is set to enabled.
	P30		General purpose input/output port. This function becomes valid when output of waveform generator is set to disabled.
58	INT0	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P40		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.

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Pin no.	Pin name	I/O Circuit type*1	Description
59	INT1	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P41		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.
60	INT2	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P42		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.
61	INT3	E	External interrupt input terminal. Since this input is used as required while the corresponding external interrupt is enabled, the port output must remain off unless intentionally used.
	P43		General purpose input/output port. This function becomes valid when external interrupt input is set to disabled.

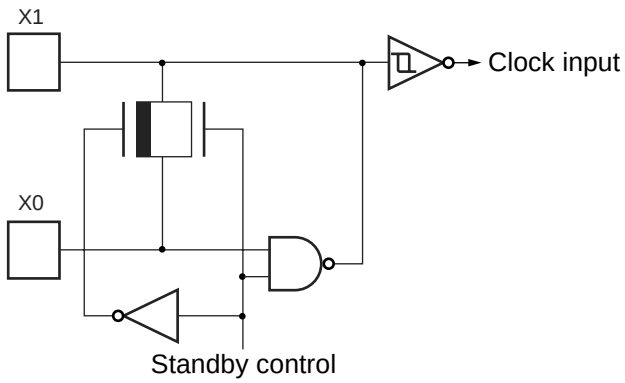
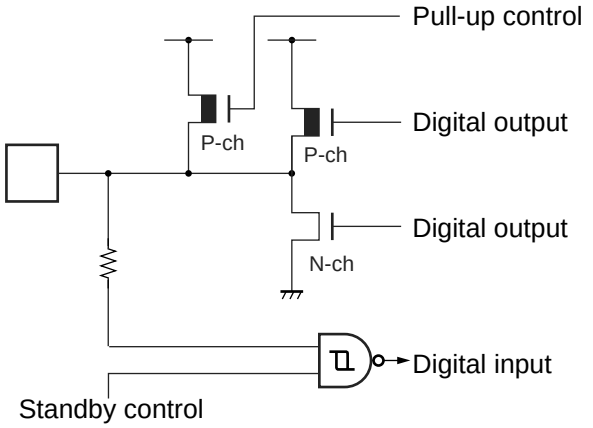
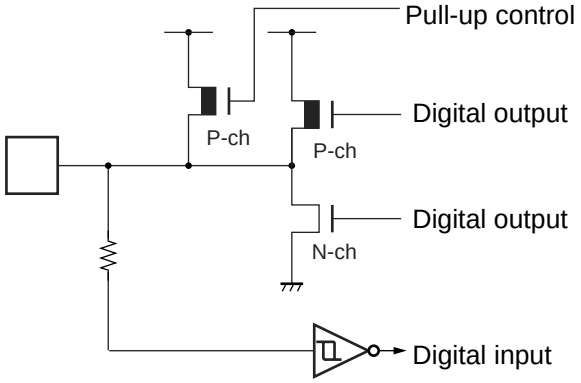
*1 : For the I/O circuit type, refer to " ■ I/O CIRCUIT TYPE "

*2 : C-CAN is set in MB91267NA/F267NA.

• Power supply and GND pins

Pin no.	Pin name	Description
16, 48	Vss	GND pins. Apply equal potential to all of the pins.
17	Vcc	Power supply pin. Apply equal potential to all of the pins.
64	AVcc	Analog power supply pin for A/D converter.
63	AVRH2	Analog reference power supply pin for A/D converter 2.
62	AVRH1	Analog reference power supply pin for A/D converter 1.
1	AVss	Analog GND pin for A/D converter.
15	C	Condenser connection pin for internal regulator.
2	ACC	Condenser connection pin for analog.

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		Oscillation feedback resistance for high speed (main clock oscillation) : approx. 1 MΩ
D		• CMOS level output • CMOS level hysteresis input • With standby control • With Pull-up control • I_{OL} = 4 mA
E		• CMOS level output • CMOS level hysteresis input • Without standby control • With Pull-up control • I_{OL} = 4 mA

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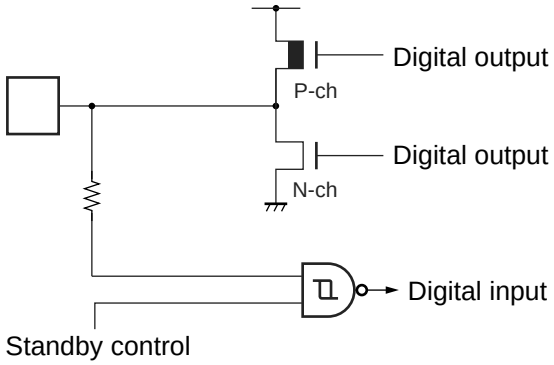
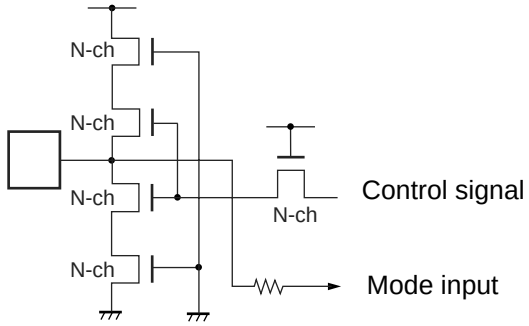
Type	Circuit type	Remarks
J		• CMOS level output • CMOS level hysteresis input • With standby control • I_{OL} = 12 mA
K		Flash memory product only • CMOS level input • High voltage control for test of flash

Order of power turning ON/OFF

Use the following procedure for turning the power on or off.

Note that, even if the A/D converter is not used, keep the following pins connected with the level as described below.

AV_{CC} = V_{CC} level

AV_{SS} = V_{SS} level

- When Powering ON : $V_{CC} \rightarrow AV_{CC} \rightarrow AVRH$
- When Powering OFF : $AVRH \rightarrow AV_{CC} \rightarrow V_{CC}$

About Oscillation Input at Power On

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

- The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) acceptance of a user interrupt, (b) single-stepped, or (c) breaks in response to a data event or emulator menu :

  1) The D0 and D1 flags are updated in advance.

  2) An EIT handling routine (user interrupt or emulator) is executed.

  3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed, and the D0 and D1 flags are updated to the same values as in 1).

- The following operations are performed when the ORCCR/STILM/MOVRi and PS instructions are executed to allow the interrupt.

  1) The PS register is updated in advance.

  2) An EIT handling routine (user interrupt) is executed.

  3) Upon returning from the EIT, the above instructions are executed, and the PS register is updated to the same value as in 1).

Watchdog Timer

The watchdog timer built in this model monitors a program that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on operating programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.

For those conditions to which this exception applies, refer to “ ■ NOTE ON DEBUGGER”.

■ NOTE ON DEBUGGER

- Step execution of RETI command

  If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution.

  This will prevent the main routine and low-interrupt-level programs from being executed.

  Do not execute step of RETI instruction for escape.

  Disable the corresponding interrupt and execute debugger when the corresponding interrupt handling routine no longer needs debugging.

- Operand break

  Do not apply a data event break to access to the area containing the address of a system stack pointer.

- Execution in an unused area of flash memory

  Accidentally executing an instruction in an unused area of flash memory (with data placed at 0xFFFF) prevents breaks from being accepted.

  To prevent this, the code event address mask function of the debugger should be used to cause a break when accessing an instruction in an unused area.

- Power-on debugging

  All of the following three conditions must be satisfied when the power supply is turned off by power-on debugging.

  (1) The time for the user power to fall from 0.9 V_{CC} to 0.5 V_{CC} is 25 µs or longer.
  Note : In a dual-power system, V_{CC} indicates the external I/O power supply voltage.

  (2) CPU operating frequency must be higher than 1 MHz.

  (3) During execution of user program

- Interrupt handler for NMI request (tool)

  Add the following program to the interrupt handler to prevent the device from malfunctioning in case the factor flag to be set only in response to a break request from the ICE is set, for example, by an adverse effect of noise to the DSU pin while the ICE is not connected. Enable to use the ICE while adding this program.

Additional location

Next interrupt handler

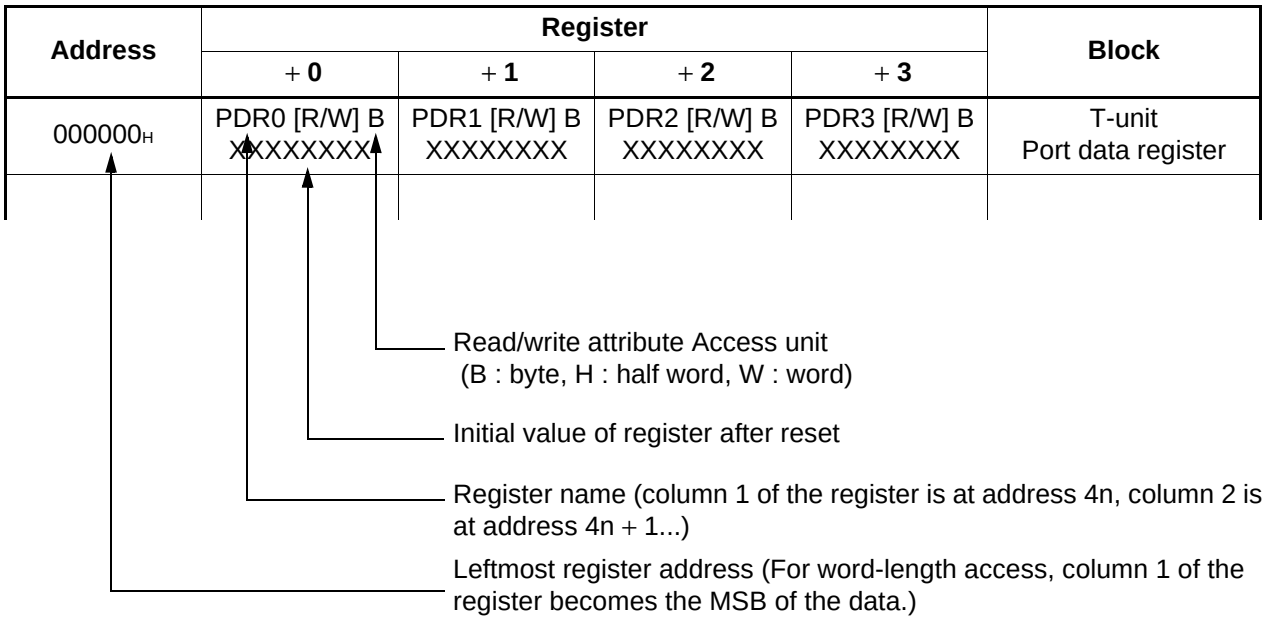
Interrupt source	: NMI request (tool)
Interrupt number	: #13 (decimal) , 0D (hexadecimal)
Offset	: $3C8_H$
Address TBR is default	: $000FFFC8_H$

Additional program

```
STM     (R0, R1)
LDI     #B00H, R0;    : B00H is the address of DSU break factor register.
LDI     #0, R1
STB     R1, @R0       : Clear the break factor register.
LDM     (R0, R1)
RETI
```

■ I/O MAP

[How to read the table]



Note : Initial values of register bits are represented as follows :

" 1 " : Initial Value " 1 "
" 0 " : Initial Value " 0 "
" X " : Initial Value " undefined"
" - " : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] B, H, W XXXXXXXX	PDR1 [R/W] B, H, W XXXXXXXX	PDR2 [R/W] B, H, W XXXXXXXX	PDR3 [R/W] B, H, W XXXXXXXX	Port data register
000004H	PDR4 [R/W] B, H, W -XXXXXXX	PDR5 [R/W] B, H, W XXXXXXXX	—		
000008H, 00000CH	—				
000010H	PDRG [R/W] B, H, W ------X-	—			
000014H to 00003CH	—				Reserved
000040H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt (INT0 to INT7)
000044H	DICR [R/W] B, H, W -------0	HRCL [R/W, R] B, H, W 0--11111	—		Delay interrupt/ Hold request
000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 0
00004CH	—		TMCSR0 [R/W, R] B, H, W ---00000 00000000		
000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 1
000054H	—		TMCSR1 [R/W, R] B, H, W ---00000 00000000		
000058H	TMRLR2 [W] H, W XXXXXXXX XXXXXXXX		TMR2 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 2
00005CH	—		TMCSR2 [R/W, R] B, H, W ---00000 00000000		
000060H	SSR0 [R/W, R] B, H, W 00001000	SIDR0 [R]/SODR0[W] B, H, W XXXXXXXX	SCR0 [R/W] B, H, W 00000100	SMR0 [R/W, W] B, H, W 00--0-0-	UART0
000064H	UTIM0 [R] H / UTIMR0 [W] H 00000000 00000000		DRCL0 [W] B --------	UTIMC0 [R/W] B 0--00001	U-TIMER 0
000068H	SSR1 [R/W, R] B, H, W 00001000	SIDR1 [R]/SODR1[W] B, H, W XXXXXXXX	SCR1 [R/W] B, H, W 00000100	SMR1 [R/W] B, H, W 00--0-0-	UART1
00006CH	UTIM1 [R] H / UTIMR1 [W] H 00000000 00000000		DRCL1 [W] B --------	UTIMC1 [R/W] B 0--00001	U-TIMER 1
000070H to 00007CH	—				Reserved
000080H	ADCH1 [R/W] B, H, W XXXX0XX0	ADMD1 [R/W] B, H, W 00001111	ADCD11 [R] B, H, W XXXXXXXX	ADCD10 [R] B, H, W XXXXXXXX	A/D converter 1/ AICR1
000084H	ADCS1 [R/W, W] B, H, W 00000X00	—	AICR1 [R/W] B, H, W ----0000	—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00015CH	CPCLRBH2, CPCLRBL2 [W] / CPCLRH2, CPCLRL2 [R] H, W 11111111 11111111		TCDTH2, TCDTL2 [R/W] H, W 00000000 00000000		16-bit free-run timer 2
000160H	TCCSH2 [R/W] B, H, W 00000000	TCCSL2 [R/W] B, H, W 01000000	—		
000164H	—				Reserved
000168H	—	FSR2 [R/W] B, H, W 00000000	FSR1 [R/W] B, H, W ----0000	FSR0 [R/W] B, H, W 00000000	FRT selector
00016CH to 0001A4H	—				Reserved
0001A8H	CANPRE [R, R/W] B, H, W 00000000	—			C-CAN*1 prescaler
0001ACH to 0001FCH	—				Reserved
000200H	DMACA0 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] B, H, W*2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] B, H, W *2 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	—				Reserved
000240H	DMACR [R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 000398H	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00039C$_H$	—				16-bit MAC
0003A0$_H$	DSP-PC [R/W] XXXXXXXX	DSP-CSR [R/W, R, W] 00000000	DSP-LY [R/W] XXXXXXXX XXXXXXXX		
0003A4$_H$	DSP-OT0 [R] XXXXXXXX XXXXXXXX		DSP-OT1 [R] XXXXXXXX XXXXXXXX		
0003A8$_H$	DSP-OT2 [R] XXXXXXXX XXXXXXXX		DSP-OT3 [R] XXXXXXXX XXXXXXXX		
0003AC$_H$	—				
0003B0$_H$	DSP-OT4 [R] XXXXXXXX XXXXXXXX		DSP-OT5 [R] XXXXXXXX XXXXXXXX		
0003B4$_H$	DSP-OT6[R] XXXXXXXX XXXXXXXX		DSP-OT7 [R] XXXXXXXX XXXXXXXX		
0003B8$_H$	—				
0003BC$_H$ to 0003EC$_H$	—				Reserved
0003F0$_H$	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4$_H$	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8$_H$	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC$_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400$_H$	DDR0 [R/W] B, H, W 00000000	DDR1 [R/W] B, H, W 00000000	DDR2 [R/W] B, H, W 00000000	DDR3 [R/W] B, H, W 00000000	Data direction register
000404$_H$	DDR4 [R/W] B, H, W -0000000	DDR5 [R/W] B, H, W 00000000	—		
000408$_H$, 00040C$_H$	—				
000410$_H$	DDRG [R/W] B, H, W ------0-	—			
000414$_H$ to 00041C$_H$	—				Reserved
000420$_H$	PFR0 [R/W] B, H, W 00------	PFR1 [R/W] B, H, W 0-0-00-0	—		Port function register
000424$_H$ to 00042C$_H$	—				
000430$_H$	—			PTFR0 [R/W] B, H, W 00000000	

(Continued)

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
020054H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		C-CAN*1
020060H	Reserved (IF2 data mirror, little endian byte ordering)				
020080H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		
020084H	Reserved (>32..128 Message buffer)				
020090H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
020094H	Reserved (>32..128 Message buffer)				
0200A0H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
0200A4H	Reserved (>32..128 Message buffer)				
0200B0H	MESVAL20 [R] 00000000 00000000		MESVAL10 [R] 00000000 00000000		
0200B4H	Reserved (>32..128 Message buffer)				

*1 : C-CAN is loaded in MB91267NA/F267NA.

*2 : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed in bytes.

Notes :
- The initial value of FLWC (7004_H) is "00010011_B" on EVA tool. Writing "00000011_B" on the evaluation model has no effect on its operation.
- Do not execute Read Modify Write instructions on registers having a write-only bit.
- Data is undefined in reserved or (-) area.

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
UART1(Reception completed)	33	21	ICR17	378H	000FFF78H
UART1 (RX completed)	34	22	ICR18	374H	000FFF74H
C-CAN0*	35	23	ICR19	370H	000FFF70H
System reserved	36	24	ICR20	36CH	000FFF6CH
16-bit MAC	37	25	ICR21	368H	000FFF68H
PPG0/PPG1	38	26	ICR22	364H	000FFF64H
PPG2/PPG3	39	27	ICR23	360H	000FFF60H
PPG4/PPG5/PPG6/PPG7	40	28	ICR24	35CH	000FFF5CH
System reserved	41	29	ICR25	358H	000FFF58H
Waveform0/1/2 (underflow)	42	2A	ICR26	354H	000FFF54H
Free-run timer 1 (compare clear)	43	2B	ICR27	350H	000FFF50H
Free-run timer 1 (zero detection)	44	2C	ICR28	34CH	000FFF4CH
Free-run timer 2 (compare clear)	45	2D	ICR29	348H	000FFF48H
Free-run timer 2 (zero detection)	46	2E	ICR30	344H	000FFF44H
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H
Free-run timer 0 (compare clear)	48	30	ICR32	33CH	000FFF3CH
Free-run timer 0 (zero detection)	49	31	ICR33	338H	000FFF38H
System reserved	50	32	ICR34	334H	000FFF34H
A/D converter 1	51	33	ICR35	330H	000FFF30H
A/D converter 2	52	34	ICR36	32CH	000FFF2CH
PWC0 (measurement completed)	53	35	ICR37	328H	000FFF28H
System reserved	54	36	ICR38	324H	000FFF24H
PWC0 (overflow)	55	37	ICR39	320H	000FFF20H
System reserved	56	38	ICR40	31CH	000FFF1CH
ICU0 (capture)	57	39	ICR41	318H	000FFF18H
ICU1 (capture)	58	3A	ICR42	314H	000FFF14H
ICU2/3 (capture)	59	3B	ICR43	310H	000FFF10H
OCU0/1 (match)	60	3C	ICR44	30CH	000FFF0CH
OCU2/3 (match)	61	3D	ICR45	308H	000FFF08H
OCU4/5 (match)	62	3E	ICR46	304H	000FFF04H
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H

(Continued)

(3) UART Timing

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

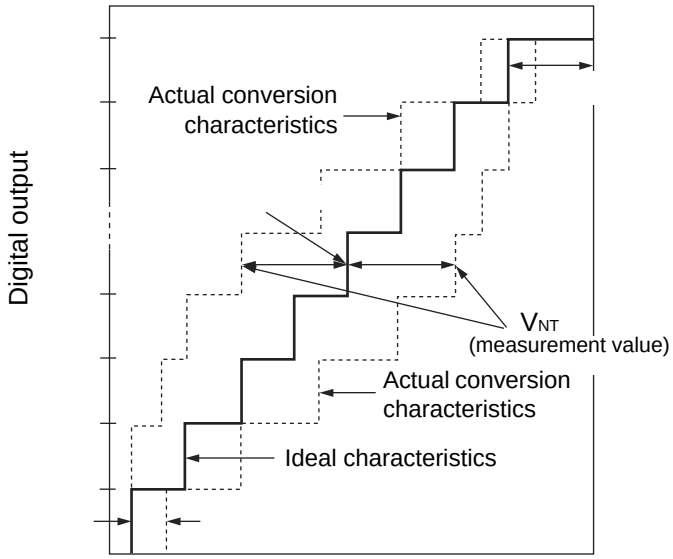
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode	8 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1, SOT0, SOT1		– 80	+ 80	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1, SIN0, SIN1		100	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1, SIN0, SIN1		60	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode	4 t_{CYCP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		4 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1, SOT0, SOT1		—	150	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1, SIN0, SIN1		60	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1, SIN0, SIN1		60	—	ns

Notes : • The above ratings are the values for clock synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.

Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Zero transition point (00 0000 0000 ⟷ 00 0000 0001) and full-scale transition point. Difference between the line connected (11 1111 1110 ⟷ 11 1111 1111) and actual conversion characteristics.
- Differential linearity error : Deviation of input voltage, that is required for changing output code by 1 LSB, from an ideal value.
- Total error : This error indicates the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error..

Total error



$$1\text{LSB'}_{\text{(Ideal value)}} = \frac{AVRH - AV_{SS}}{1024}\ [V] \qquad \text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from $(N + 1)_H$ to N_H.
V_{OT}' (Ideal value) = AV_{SS} + 0.5LSB' [V]
V_{FST}' (Ideal value) = AVRH – 1.5 LSB' [V]

(Continued)

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Deleted the MB91266A (MASK ROM Product) Added the MB91267A and MB91267NA (MASK ROM Product)

MEMO

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