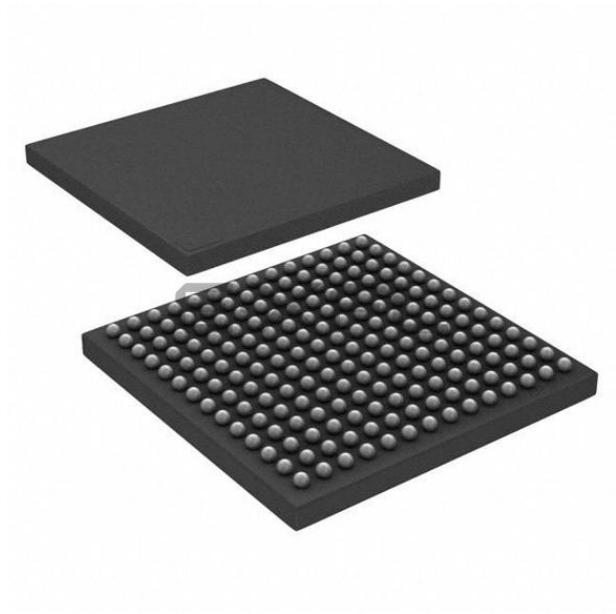

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d22b-cn

26.6.22 RTC TimeStamp Source Register

Name: RTC_TSSRx

Address: 0xF8048168 [0], 0xF8048174 [1]

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
DET7	DET6	DET5	DET4	DET3	DET2	DET1	DET0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	JTAG	TST	–	–

The following configuration values are valid for all listed bit names of this register:

0: No alarm generated since the last clear.

1: An alarm has been generated by the corresponding monitor since the last clear.

TST: Test Pin Monitor

JTAG: JTAG Pins Monitor

DETx: PIOBU Intrusion Detector

34.7.25 Secure PIO Interrupt Status Register

Name: S_PIO_ISRx [x=0..3]

Address: 0xFC03902C [0], 0xFC03906C [1], 0xFC0390AC [2], 0xFC0390EC [3]

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0–P31: Input Change Interrupt Status

0: No Input Change has been detected on the I/O line of the I/O group x since S_PIO_ISRx was last read or since reset.

1: At least one Input Change has been detected on the I/O line of the I/O group since S_PIO_ISRx was last read or since reset.

34.7.26 Secure PIO Set I/O Non-Secure Register

Name: S_PIO_SIONRx [x=0..3]

Address: 0xFC039030 [0], 0xFC039070 [1], 0xFC0390B0 [2], 0xFC0390F0 [3]

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0–P31: Set I/O Non-Secure

0: No effect.

1: Set the I/O line of the I/O group x in Non-Secure mode.

37.7 Product Dependencies

37.7.1 I/O Lines

The pins used for interfacing the Static Memory Controller are multiplexed with the PIO lines. The programmer must first program the PIO controller to assign the Static Memory Controller pins to their peripheral function. If I/O lines of the SMC are not used by the application, they can be used for other purposes by the PIO controller.

37.7.2 Power Management

The SMC is clocked through the Power Management Controller (PMC), thus the programmer must first configure the PMC to enable the SMC clock.

37.7.3 Interrupt Sources

The SMC has an interrupt line connected to the interrupt controller. Handling the SMC interrupt requires programming the interrupt controller before configuring the SMC.

Table 37-3: Peripheral IDs

Instance	ID
HSMC	17

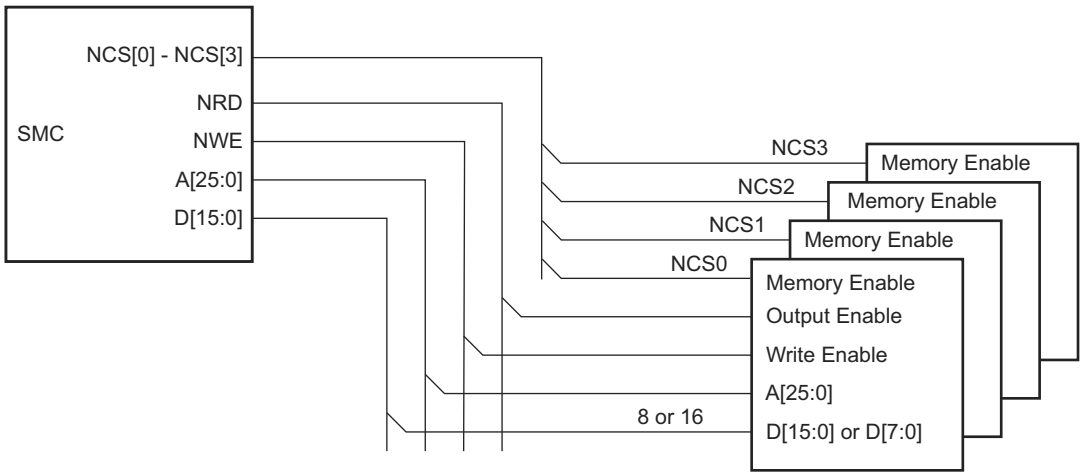
37.8 External Memory Mapping

The SMC provides up to 26 address lines, A[25:0]. This allows each chip select line to address up to 64 Mbytes of memory.

If the physical memory device connected on one chip select is smaller than 64 Mbytes, it wraps around and appears to be repeated within this space. The SMC correctly handles any valid access to the memory device within the page (see Figure 37-3).

A[25:0] is only significant for 8-bit memory; A[25:1] is used for 16-bit memory.

Figure 37-3: Memory Connections for External Devices



37.20.4 NFC Interrupt Enable Register

Name: HSMC_IER

Address: 0xF801400C

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	RB_EDGE0
23	22	21	20	19	18	17	16
NFCASE	AWB	UNDEF	DTOE	–	–	CMDDONE	XFRDONE
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	RB_FALL	RB_RISE	–	–	–	–

RB_RISE: Ready Busy Rising Edge Detection Interrupt Enable

0: No effect

1: Interrupt source enabled

RB_FALL: Ready Busy Falling Edge Detection Interrupt Enable

0: No effect

1: Interrupt source enabled

XFRDONE: Transfer Done Interrupt Enable

0: No effect

1: Interrupt source enabled

CMDDONE: Command Done Interrupt Enable

0: No effect

1: Interrupt source enabled

DTOE: Data Timeout Error Interrupt Enable

0: No effect

1: Interrupt source enabled

UNDEF: Undefined Area Access Interrupt Enable

0: No effect

1: Interrupt source enabled

AWB: Accessing While Busy Interrupt Enable

0: No effect

1: Interrupt source enabled

39.7.20 Base Layer Interrupt Disable Register

Name: LCDC_BASEIDR

Address: 0xF0000050

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	OVR	DONE	ADD	DSCR	DMA	–	–

DMA: End of DMA Transfer Interrupt Disable

0: No effect

1: Interrupt source is disabled

DSCR: Descriptor Loaded Interrupt Disable

0: No effect

1: Interrupt source is disabled

ADD: Head Descriptor Loaded Interrupt Disable

0: No effect

1: Interrupt source is disabled

DONE: End of List Interrupt Disable

0: No effect

1: Interrupt source is disabled

OVR: Overflow Interrupt Disable

0: No effect

1: Interrupt source is disabled

39.7.25 Base DMA Control Register

Name: LCDC_BASECTRL

Address: 0xF0000064

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	DONEIEN	ADDIEN	DSCRIEN	DMAIEN	LFETCH	DFETCH

DFETCH: Transfer Descriptor Fetch Enable

0: Transfer Descriptor fetch is disabled

1: Transfer Descriptor fetch is enabled

LFETCH: Lookup Table Fetch Enable

0: Lookup Table DMA fetch is disabled

1: Lookup Table DMA fetch is enabled

DMAIEN: End of DMA Transfer Interrupt Enable

0: DMA transfer completed interrupt is enabled

1: DMA transfer completed interrupt is disabled

DSCRIEN: Descriptor Loaded Interrupt Enable

0: Transfer descriptor loaded interrupt is enabled

1: Transfer descriptor loaded interrupt is disabled

ADDIEN: Add Head Descriptor to Queue Interrupt Enable

0: Transfer descriptor added to queue interrupt is enabled

1: Transfer descriptor added to queue interrupt is enabled

DONEIEN: End of List Interrupt Enable

0: End of list interrupt is disabled

1: End of list interrupt is enabled

39.7.77 High-End Overlay Channel Disable Register

Name: LCDC_HEOCHDR

Address: 0xF0000344

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	CHRST

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	CHDIS

CHDIS: Channel Disable

0: No effect

1: Disables the layer at the end of the current frame. The frame is completed.

CHRST: Channel Reset

0: No effect

1: Resets the layer immediately. The frame is aborted.

If bit zero of the receive buffer descriptor is already set when the receive buffer manager reads the location of the receive AHB buffer, then the buffer has been already used and cannot be used again until software has processed the frame and cleared bit zero. In this case, the “buffer not available” bit in the Receive Status register is set and an interrupt triggered. The Receive Resource Error statistics register is also incremented.

When the DMA is configured in the packet buffer full store and forward mode, the user can optionally select whether received frames should be automatically discarded when no AHB buffer resource is available. This feature is selected via bit 24 of the DMA Configuration register (by default, the received frames are not automatically discarded). If this feature is off, then received packets will remain to be stored in the SRAM-based packet buffer until AHB buffer resource next becomes available. This may lead to an eventual packet buffer overflow if packets continue to be received when bit zero (used bit) of the receive buffer descriptor remains set. Note that after a used bit has been read, the receive buffer manager will re-read the location of the receive buffer descriptor every time a new packet is received. When the DMA is not configured in the packet buffer full store and forward mode and a used bit is read, the frame currently being received will be automatically discarded.

When the DMA is configured in the packet buffer full store and forward mode, a receive overrun condition occurs when the receive SRAM-based packet buffer is full, or because HRESP was not OK. In all other modes, a receive overrun condition occurs when either the AHB bus was not granted quickly enough, or because HRESP was not OK, or because a new frame has been detected by the receive block, but the status update or write back for the previous frame has not yet finished. For a receive overrun condition, the receive overrun interrupt is asserted and the buffer currently being written is recovered. The next frame that is received whose address is recognized reuses the buffer.

In any packet buffer mode, a write to bit 18 of GMAC_NCR will force a packet from the external SRAM-based receive packet buffer to be flushed. This feature is only acted upon when the RX DMA is not currently writing packet data out to AHB, i.e., it is in an IDLE state. If the RX DMA is active, a write to this bit is ignored.

40.6.3.4 Transmit AHB Buffers

Frames to transmit are stored in one or more transmit AHB buffers. Transmit frames can be between 1 and 16384 bytes long, so it is possible to transmit frames longer than the maximum length specified in the IEEE 802.3 standard. It should be noted that zero length AHB buffers are allowed and that the maximum number of buffers permitted for each transmit frame is 128.

The start location for each transmit AHB buffer is stored in memory in a list of transmit buffer descriptors at a location pointed to by the transmit buffer queue pointer. The base address for this queue pointer is set in software using the Transmit Buffer Queue Base Address register. Each list entry consists of two words. The first is the byte address of the transmit buffer and the second containing the transmit control and status. For the packet buffer DMA, the start location for each AHB buffer is a byte address, the bottom bits of the address being used to offset the start of the data from the data-word boundary (i.e., bits 2,1 and 0 are used to offset the address for 64-bit datapaths).

Frames can be transmitted with or without automatic CRC generation. If CRC is automatically generated, pad will also be automatically generated to take frames to a minimum length of 64 bytes. When CRC is not automatically generated (as defined in word 1 of the transmit buffer descriptor), the frame is assumed to be at least 64 bytes long and pad is not generated.

An entry in the transmit buffer descriptor list is described in Table 40-5.

To transmit frames, the buffer descriptors must be initialized by writing an appropriate byte address to bits [31:0] in the first word of each descriptor list entry.

The second word of the transmit buffer descriptor is initialized with control information that indicates the length of the frame, whether or not the MAC is to append CRC and whether the buffer is the last buffer in the frame.

After transmission the status bits are written back to the second word of the first buffer along with the used bit. Bit 31 is the used bit which must be zero when the control word is read if transmission is to take place. It is written to one once the frame has been transmitted. Bits[29:20] indicate various transmit error conditions. Bit 30 is the wrap bit which can be set for any buffer within a frame. If no wrap bit is encountered the queue pointer continues to increment.

The Transmit Buffer Queue Base Address register can only be updated while transmission is disabled or halted; otherwise any attempted write will be ignored. When transmission is halted the transmit buffer queue pointer will maintain its value. Therefore when transmission is restarted the next descriptor read from the queue will be from immediately after the last successfully transmitted frame. while transmit is disabled (bit 3 of the Network Control register set low), the transmit buffer queue pointer resets to point to the address indicated by the Transmit Buffer Queue Base Address register. Note that disabling receive does not have the same effect on the receive buffer queue pointer.

Once the transmit queue is initialized, transmit is activated by writing to the transmit start bit (bit 9) of the Network Control register. Transmit is halted when a buffer descriptor with its used bit set is read, a transmit error occurs, or by writing to the transmit halt bit of the Network Control register. Transmission is suspended if a pause frame is received while the pause enable bit is set in the Network Configuration register. Rewriting the start bit while transmission is active is allowed. This is implemented with TXGO variable which is readable in the Transmit Status register at bit location 3. The TXGO variable is reset when:

- Transmit is disabled.

41.7.14 UDPHS Endpoint Control Register (Isochronous Endpoint)

Name: UDPHS_EPTCTLx [x=0..15] (ISOENDPT)

Address: 0xFC02C10C [0], 0xFC02C12C [1], 0xFC02C14C [2], 0xFC02C16C [3], 0xFC02C18C [4], 0xFC02C1AC [5], 0xFC02C1CC [6], 0xFC02C1EC [7], 0xFC02C20C [8], 0xFC02C22C [9], 0xFC02C24C [10], 0xFC02C26C [11], 0xFC02C28C [12], 0xFC02C2AC [13], 0xFC02C2CC [14], 0xFC02C2EC [15]

Access: Read-only

31	30	29	28	27	26	25	24
SHRT_PCKT	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	BUSY_BANK	–	–
15	14	13	12	11	10	9	8
–	ERR_FLUSH	ERR_CRC_NTR	ERR_FL_ISO	TXRDY_TRER	TX_COMPLT	RXRDY_TXKL	ERR_OVFLW
7	6	5	4	3	2	1	0
MDATA_RX	DATAX_RX	–	–	INTDIS_DMA	–	AUTO_VALID	EPT_ENABL

This register view is relevant only if EPT_TYPE = 0x1 in “UDPHS Endpoint Configuration Register” .

EPT_ENABL: Endpoint Enable (cleared upon USB reset)

0: The endpoint is disabled according to the device configuration. Endpoint 0 should always be enabled after a hardware or UDPHS bus reset and participate in the device configuration.

1: The endpoint is enabled according to the device configuration.

AUTO_VALID: Packet Auto-Valid Enabled (cleared upon USB reset)

Set this bit to automatically validate the current packet and switch to the next bank for both IN and OUT endpoints.

For IN Transfer:

If this bit is set, the UDPHS_EPTSTAx register TXRDY_TRER bit is set automatically when the current bank is full and at the end of DMA buffer if the UDPHS_DMACONTROLx register END_B_EN bit is set.

The user may still set the UDPHS_EPTSTAx register TXRDY_TRER bit if the current bank is not full, unless the user needs to send a Zero Length Packet by software.

For OUT Transfer:

If this bit is set, the UDPHS_EPTSTAx register RXRDY_TXKL bit is automatically reset for the current bank when the last packet byte has been read from the bank FIFO or at the end of DMA buffer if the UDPHS_DMACONTROLx register END_B_EN bit is set. For example, to truncate a padded data packet when the actual data transfer size is reached.

The user may still clear the UDPHS_EPTSTAx register RXRDY_TXKL bit, for example, after completing a DMA buffer by software if UDPHS_DMACONTROLx register END_B_EN bit was disabled or in order to cancel the read of the remaining data bank(s).

INTDIS_DMA: Interrupt Disables DMA (cleared upon USB reset)

If set, when an enabled endpoint-originated interrupt is triggered, the DMA request is disabled regardless of the UDPHS_IEN register EPT_x bit for this endpoint. Then, the firmware will have to clear or disable the interrupt source or clear this bit if transfer completion is needed.

If the exception raised is associated with the new system bank packet, then the previous DMA packet transfer is normally completed, but the new DMA packet transfer is not started (not requested).

If the exception raised is not associated to a new system bank packet (ex: ERR_FL_ISO), then the request cancellation may happen at any time and may immediately stop the current DMA transfer.

This may be used, for example, to identify or prevent an erroneous packet to be transferred into a buffer or to complete a DMA buffer by software after reception of a short packet, or to perform buffer truncation on ERR_FL_ISO interrupt for adaptive rate.

DATAX_RX: DATAx Interrupt Enabled (Only for High Bandwidth Isochronous OUT endpoints) (cleared upon USB reset)

0: No effect.

FRAME: CLASSD Incoming Data Sampling Frequency

Value	Name	Description
0	FRAME_8K	8 kHz
1	FRAME_16K	16 kHz
2	FRAME_32K	32 kHz
3	FRAME_48K	48 kHz
4	FRAME_96K	96 kHz
5	FRAME_22K	22.05 kHz
6	FRAME_44K	44.1 kHz
7	FRAME_88K	88.2 kHz

EQCFG: Equalization Selection

Value	Name	Description
0	FLAT	Flat Response
1	BBOOST12	Bass boost +12 dB
2	BBOOST6	Bass boost +6 dB
3	BCUT12	Bass cut -12 dB
4	BCUT6	Bass cut -6 dB
5	MBOOST3	Medium boost +3 dB
6	MBOOST8	Medium boost +8 dB
7	MCUT3	Medium cut -3 dB
8	MCUT8	Medium cut -8 dB
9	TBOOST12	Treble boost +12 dB
10	TBOOST6	Treble boost +6 dB
11	TCUT12	Treble cut -12 dB
12	TCUT6	Treble cut -6 dB

Note: EQCFG field values 13–15 = Flat Response

MONO: Mono Signal

0 (DISABLED): The signal is sent stereo to the left and right channels.

1 (ENABLED): The same signal is sent on both left and right channels. The sent signal is defined by the MONOMODE field value.

MONOMODE: Mono Mode Selection

This field defines which signal is sent on both channels when the MONO bit is set.

Value	Name	Description
0	MONOMIX	(left + right) / 2 is sent on both channels
1	MONOSAT	(left + right) is sent to both channels. If the sum is too high, the result is saturated.
2	MONOLEFT	THR[15:0] is sent on both left and right channels
3	MONORIGHT	THR[31:16] is sent on both left and right channels

46.7.15 TWIHS Receive Holding Register

Name: TWIHS_RHR

Address: 0xF8028030 (0), 0xFC028030 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
RXDATA							

RXDATA: Master or Slave Receive Holding Data

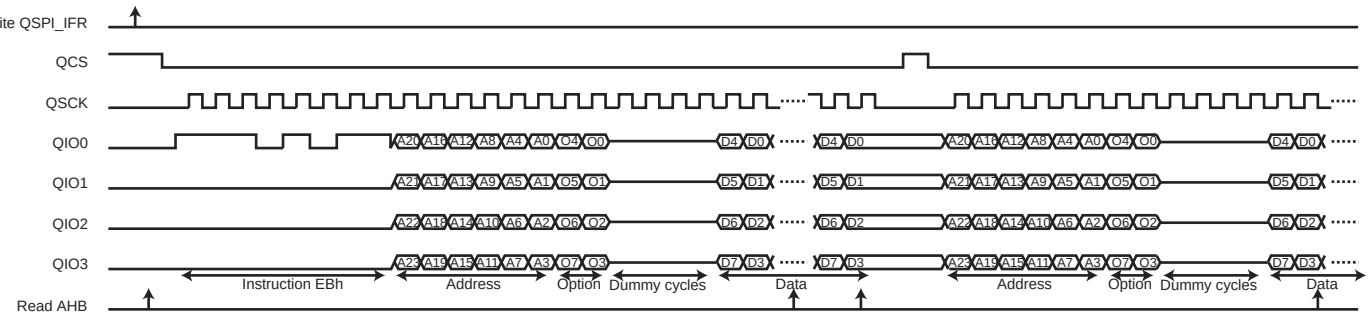
Example 7:

Instruction in Single-bit SPI, with address and option in Quad SPI, with data read in Quad SPI, with four dummy cycles, with fetch and continuous read.

Command: FAST READ QUAD I/O (EBh) - 8-BIT OPTION (0x30h)

- Write 0x0030_00EB in QSPI_ICR.
- Write 0x0004_33F4 in QSPI_IFR.
- Read QSPI_IFR (dummy read) to synchronize system bus accesses.
- Read data in the QSPI system bus memory space (0x9000_00000-0x9800_00000/0XD000_0000--0XD800_0000). Fetch is enabled, the address of the system bus read accesses is always used.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 50-17: Instruction Transmission Waveform 7



54.6.12.2 WAVSEL = 10

When TC_CMRx.WAVSEL = 10, the value of TC_CV is incremented from 0 to the value of RC, then automatically reset on a RC Compare. Once the value of TC_CV has been reset, it is then incremented and so on. See Figure 54-10.

It is important to note that TC_CV can be reset at any time by an external event or a software trigger if both are programmed correctly. See Figure 54-11.

In addition, RC Compare can stop the counter clock (TC_CMRx.CPCSTOP = 1) and/or disable the counter clock (TC_CMRx.CPCDIS = 1).

Figure 54-10: WAVSEL = 10 without Trigger

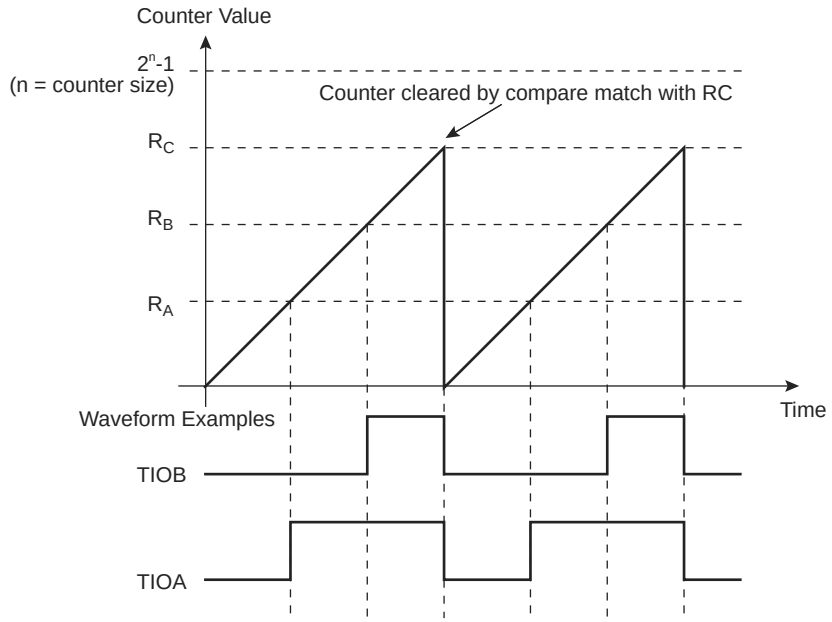
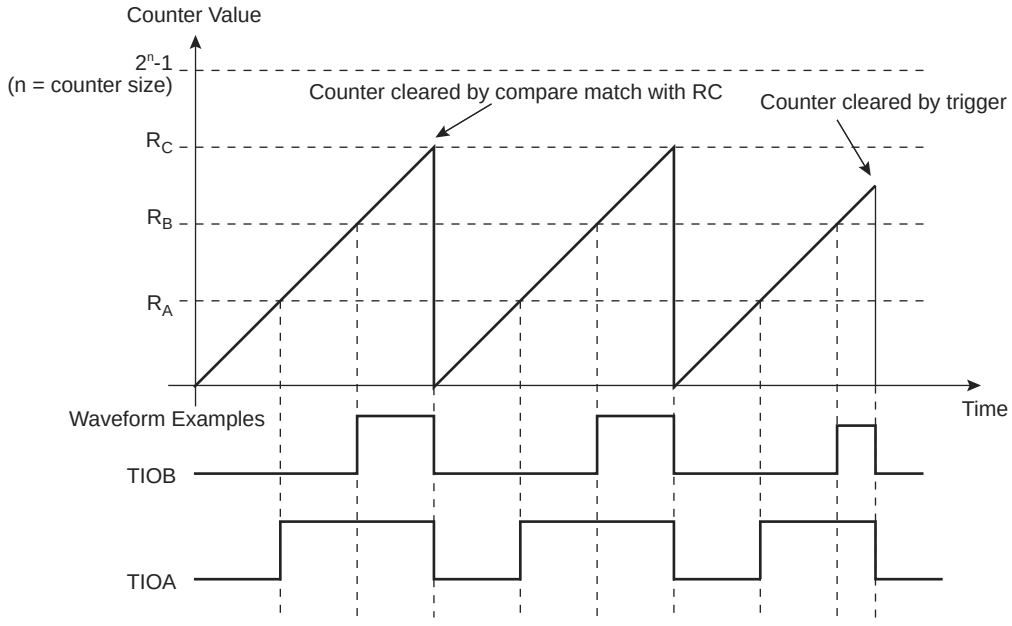


Figure 54-11: WAVSEL = 10 with Trigger



54.6.12.3 WAVSEL = 01

When TC_CMRx.WAVSEL = 01, the value of TC_CV is incremented from 0 to 2^{32}-1 . Once 2^{32}-1 is reached, the value of TC_CV is decremented to 0, then reincremented to 2^{32}-1 and so on. See Figure 54-12.

55.6.2.5 High Pass Filter

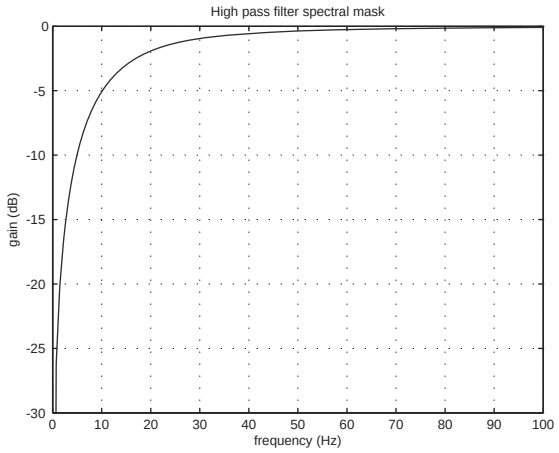
The PDMIC includes an optional first-order IIR filter performing a high pass transfer function after the low pass filter and before the decimation. The coefficients are computed for a decimated sampling rate of 48 kHz to obtain a -3dB cutoff frequency at 15 Hz.

If the decimated sampling rate is modified, the frequency response of this filter is scaled proportionally to the new frequency.

This filter can be bypassed by setting the HPFBYP bit in PDMIC_DSPR0 (see Section 55.7.8 “PDMIC DSP Configuration Register 0”).

Figure 55-9 is drawn for an output sampling frequency of 48 kHz.

Figure 55-9: High Pass Filter Spectral Mask in the 0 to 100 Hz Band



55.6.2.6 Gain and Offset Compensation

An offset, a gain, a scaling factor and a shift can be applied to a converted PDM microphone value using the following operation:

$$data = \frac{(data_0 + offset \times 2^8) \times dgain}{2^{scale + shift + 8}}$$

where:

- $data_0$ is a signed integer defined on 24 bits. It is the output of the filtering channel.
- *offset* is a signed integer defined on 16 bits (see PDMIC DSP Configuration Register 1). It is multiplied by 2^8 to have the same weight as $data_0$.
- *dgain* is an unsigned integer defined on 15 bits (see PDMIC DSP Configuration Register 1). Only the 32 MSBs of the multiplication operation are used for scaling and shifting operations. dgain defaults to 0 after reset, which forces CDR to 0. It must be programmed to a non-zero value to read non-zero data into the PDMIC_CDR register.
- *scale* is an unsigned integer defined on 4 bits (see PDMIC DSP Configuration Register 0). It shifts the multiplication operation result by *scale* bits to the right. Maximum allowed value is 15.
- *shift* is an unsigned integer defined on 4 bits (see PDMIC DSP Configuration Register 0). It shifts the multiplication operation result by *shift* bits to the right. Maximum allowed value is 15.

If the data transfer is configured in 32-bit mode (see PDMIC DSP Configuration Register 0), the 2^{shift} division is not performed and the 32-bit result of the remaining operation is sent.

If the data transfer is configured in 16-bit mode, the 2^{shift} division is performed. The result is then saturated to be within $\pm(2^{15}-1)$ and the 16 LSBs of this saturation operation are sent to the controller as the result of the PDM microphone conversion.

Default parameters are defined to output a 16-bit result whatever the data transfer configuration may be.

60.5.17 AES Extended Mode Register

Name: AES_EMR

Address: 0xF002C0B0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
NHEAD							

15	14	13	12	11	10	9	8
PADLEN							

7	6	5	4	3	2	1	0
–	–	PLIPD	PLIPEN	–	–	APM	APEN

APEN: Auto Padding Enable

0: Auto Padding feature is disabled.

1: Auto Padding feature is enabled.

APM: Auto Padding Mode

0: Auto Padding performed according to IPSEC standard.

1: Auto Padding performed according to SSL standard.

PLIPEN: Protocol Layer Improved Performance Enable

0: Protocol layer improved performance is disabled.

1: Protocol layer improved performance is enabled.

PLIPD: Protocol Layer Improved Performance Decipher

0: Protocol layer improved performance is in ciphering mode.

1: Protocol layer improved performance is in deciphering mode.

PADLEN: Auto Padding Length

0–255: Padding length in bytes

NHEAD: IPSEC Next Header

0–255: IPSEC Next Header field

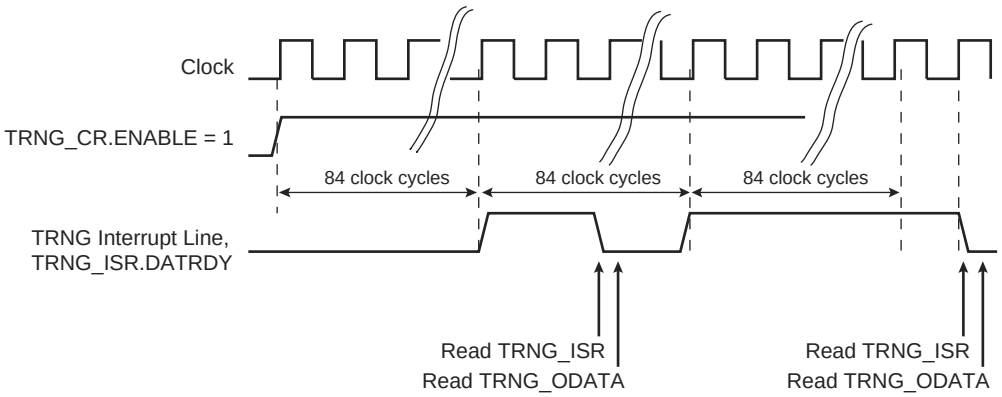
63.5 Functional Description

As soon as the TRNG is enabled in the Control register (TRNG_CR), the generator provides one 32-bit random value every 84 clock cycles.

The TRNG interrupt line can be enabled in the Interrupt Enable register (TRNG_IER), and disabled in the Interrupt Disable register (TRNG_IDR). This interrupt is set when a new random value is available and the interrupt is cleared when the Status register (TRNG_ISR) is read. The flag TRNG_ISR.DATRDY is set when the random data is ready to be read out on the 32-bit Output Data register (TRNG_ODATA).

The normal operating mode checks that the TRNG_ISR.DATRDY flag equals '1' before reading TRNG_ODATA when a 32-bit random value is required by the software application.

Figure 63-2: TRNG Data Generation Sequence



66.14 SMC Timings

66.14.1 Timing Conditions

SMC timings are given in max corners.

Timings assuming a capacitance load on data, control and address pads are given in Table 66-43.

Table 66-43: Capacitance Load

Supply	Corner	
	Max	Min
3.3V	50 pF	5 pF
1.8V	30 pF	5 pF

In the tables that follow, t_{CPMCK} is the MCK period.

Table 66-72: QSPI0 IOSET2 Timings (Continued)

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
$QSPI_{10}$	QIOx Input hold time after SCK falls	0.8	–	0.7	–	ns
$QSPI_{11}$	SCK falling to QIOx valid	0	1.5	0	1.9	ns

Table 66-73: QSPI0 IOSET3 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
Mode 0						
$QSPI_0$	QIOx Input setup time before SCK falls	1.8	–	1.7	–	ns
$QSPI_1$	QIOx Input hold time after SCK falls	0.8	–	0.7	–	ns
$QSPI_2$	SCK falling to QIOx valid	0	1.8	0	2.1	ns
Mode 1						
$QSPI_3$	QIOx Input setup time before SCK rises	12.3	–	10.1	–	ns
$QSPI_4$	QIOx Input hold time after SCK rises	0.5	–	0.3	–	ns
$QSPI_5$	SCK rising to QIOx valid	0	2.2	0	2	ns
Mode 2						
$QSPI_6$	QIOx Input setup time before SCK rises	2	–	1.7	–	ns
$QSPI_7$	QIOx Input hold time after SCK rises	0.5	–	0.3	–	ns
$QSPI_8$	SCK rising to QIOx valid	0	2.5	0	2.2	ns
Mode 3						
$QSPI_9$	QIOx Input setup time before SCK falls	11.7	–	10.2	–	ns
$QSPI_{10}$	QIOx Input hold time after SCK falls	0.8	–	0.7	–	ns
$QSPI_{11}$	SCK falling to QIOx valid	0	1.5	1.2	2	ns

Table 66-74: QSPI1 IOSET1 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
Mode 0						
$QSPI_0$	QIOx Input setup time before SCK falls	1.1	–	0.9	–	ns
$QSPI_1$	QIOx Input hold time after SCK falls	1	–	0.7	–	ns
$QSPI_2$	SCK falling to QIOx valid	0	3.2	0	2.4	ns
Mode 1						
$QSPI_3$	QIOx Input setup time before SCK rises	12	–	9.7	–	ns
$QSPI_4$	QIOx Input hold time after SCK rises	0.8	–	0.5	–	ns
$QSPI_5$	SCK rising to QIOx valid	0	2.7	0	2.1	ns
Mode 2						

Table 66-82: SSC0 IOSET1 Timings (Continued)

Symbol	Power supply / Parameter	Conditions	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
SSC_7	TK edge to TF/TD (TK input, TF input)(1)	–	3.7	13	3.2	11.3	
		STTDLY = 0 START = 4, 5 or 7	3.7 + $(3 \times t_{CPMCK})$	13 + $(3 \times t_{CPMCK})$	3.2 + $(3 \times t_{CPMCK})$	11.3 + $(3 \times t_{CPMCK})$	
Receiver							
SSC_8	RF/RD setup time before RK edge (RK input)	–	0	–	0	–	ns
SSC_9	RF/RD hold time after RK edge (RK input)	–	t_{CPMCK}	–	t_{CPMCK}	–	ns
SSC_{10}	RK edge to RF (RK input) (1)	–	3.5	12	2.9	10.4	ns
SSC_{11}	RF/RD setup time before RK edge (RK output)	–	13.6 - t_{CPMCK}	–	12 - t_{CPMCK}	–	ns
SSC_{12}	RF/RD hold time after RK edge (RK output)	–	t_{CPMCK}	–	t_{CPMCK}	–	ns
SSC_{13}	RK edge to RF (RK output) (1)	–	0	3	0	3.3	ns

Note 1: For output signals (TF, TD, RF), minimum and maximum access times are defined. The minimum access time is the time between the TK (or RK) edge and the signal change. The maximum access time is the time between the TK edge and the signal stabilization. Figure 66-38 illustrates the minimum and maximum accesses for SSC_0. The same applies for SSC_1, SSC_4, SSC_7, SSC_{10} and SSC_{13}.