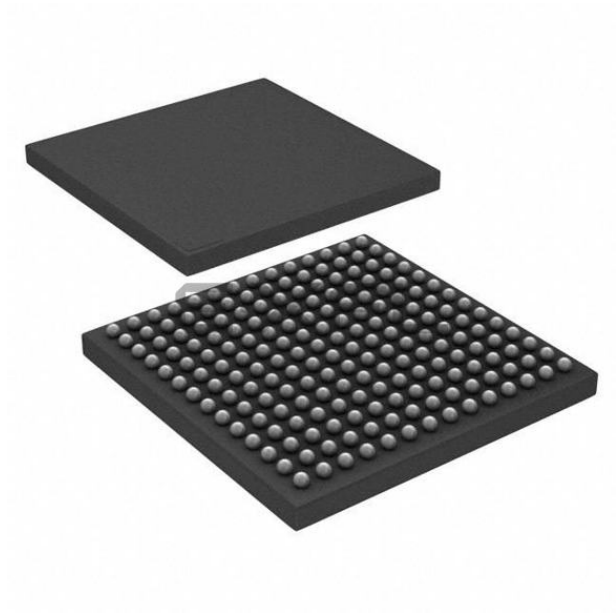

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d22c-cnr

Table 11-1: Peripheral Identifiers (Continued)

Instance ID	Instance Name	Internal Interrupt	PMC Clock Control	Instance Description	Clock Type	Security[2]	In Matrix
26	UART2	X	X	Universal Asynchronous Receiver Transmitter 2	PCLOCK_LS	PS	H32MX
27	UART3	X	X	Universal Asynchronous Receiver Transmitter 3	PCLOCK_LS	PS	H32MX
28	UART4	X	X	Universal Asynchronous Receiver Transmitter 4	PCLOCK_LS	PS	H32MX
29	TWIHS0	X	X	Two-Wire Interface 0	PCLOCK_LS	PS	H32MX
30	TWIHS1	X	X	Two-Wire Interface 1	PCLOCK_LS	PS	H32MX
31	SDMMC0	X	X	Secure Digital MultiMedia Card Controller 0	HCLOCK_HS	PS	H64MX
32	SDMMC1	X	X	Secure Digital MultiMedia Card Controller 1	HCLOCK_HS	PS	H64MX
33	SPI0	X	X	Serial Peripheral Interface 0	PCLOCK_LS	PS	H32MX
34	SPI1	X	X	Serial Peripheral Interface 1	PCLOCK_LS	PS	H32MX
35	TC0	X	X	Timer Counter 0 (ch. 0, 1, 2)	PCLOCK_LS	PS	H32MX
36	TC1	X	X	Timer Counter 1 (ch. 3, 4, 5)	PCLOCK_LS	PS	H32MX
37	–	–	–	–	–	–	–
38	PWM	X	X	Pulse Width Modulation Controller 0 (ch. 0, 1, 2, 3)	PCLOCK_LS	PS	H32MX
39	–	–	–	–	–	–	–
40	ADC	X	X	Touchscreen ADC Controller	PCLOCK_LS	PS	H32MX
41	UHPHS	X	X	USB Host High-Speed	HCLOCK_LS	PS	H32MX
42	UDPHS	X	X	USB Device High-Speed	HCLOCK_LS	PS	H32MX
43	SSC0	X	X	Synchronous Serial Controller 0	PCLOCK_LS	PS	H32MX
44	SSC1	X	X	Synchronous Serial Controller 1	PCLOCK_LS	PS	H32MX
45	LCDC	X	X	LCD Controller	HCLOCK_HS	PS	H64MX
46	ISC	X	X	Image Sensor Controller	HCLOCK_HS	PS	H64MX
47	TRNG	X	X	True Random Number Generator	PCLOCK_LS	PS	H32MX
48	PDMIC	X	X	Pulse Density Modulation Interface Controller	PCLOCK_LS	PS	H32MX
49	AIC	IRQ	–	IRQ Interrupt ID	SYS_CLK_LS	NS	H32MX
50	SFC	X	X	Secure Fuse Controller	PCLOCK_LS	PS	H32MX
51	SECURAM	X	X	Secured RAM	PCLOCK_LS	AS	H32MX
52	QSPI0	X	X	Quad SPI Interface 0	HCLOCK_HS	PS	H64MX
53	QSPI1	X	X	Quad SPI Interface 1	HCLOCK_HS	PS	H64MX
54	I2SC0	X	X	Inter-IC Sound Controller 0	PCLOCK_LS	PS	H32MX
55	I2SC1	X	X	Inter-IC Sound Controller 1	PCLOCK_LS	PS	H32MX
56	MCAN0	INT0	X	MCAN 0 Interrupt0	HCLOCK_LS	PS	H32MX
57	MCAN1	INT0	X	MCAN 1 Interrupt0	HCLOCK_LS	PS	H32MX

14.5.4 L2CC Auxiliary Control Register

Name: L2CC_ACR

Address: 0x00A00104

Access: Read/Write in Secure mode

Read-only in Non-secure mode

31	30	29	28	27	26	25	24
–	–	IPEN	DPEN	NSIAC	NSLEN	CRPOL	FWA

23	22	21	20	19	18	17	16
FWA	SAOEN	PEN	EMBEN	WAYSIZE			ASS

15	14	13	12	11	10	9	8
–	–	SAIE	EXCC	SBDLE	HPSO	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Note: The L2 Cache Controller (L2CC) must be disabled in the L2CC Control Register prior to any write access to this register.

HPSO: High Priority for SO and Dev Reads Enable

0: Strongly Ordered and Device reads have lower priority than cacheable accesses when arbitrated in the L2CC master ports. This is the default value.

1: Strongly Ordered and Device reads get the highest priority when arbitrated in the L2CC master ports.

SBDLE: Store Buffer Device Limitation Enable

0: Store buffer device limitation is disabled. Device writes can take all slots in the store buffer. This is the default value.

1: Store buffer device limitation is enabled.

EXCC: Exclusive Cache Configuration

0: Disabled. This is the default value.

1: Enabled.

SAIE: Shared Attribute Invalidate Enable

0: Shared invalidate behavior is disabled. This is the default value.

1: Shared invalidate behavior is enabled if the Shared Attribute Override Enable bit is not set.

Shared invalidate behavior is enabled if both:

- Shareable Attribute Invalidate Enable bit is set in the Auxiliary Control Register, bit[13]
- Shared Attribute Override Enable bit is not set in the Auxiliary Control Register, bit[22]

ASS: Associativity

0: 8-way.This is the default value.

1: Reserved.

WAYSIZE: Way Size

Value	Name	Description
0x0	RESERVED	Reserved
0x1	16KB_WAY	16-Kbyte way set associative
0x2	RESERVED	Reserved
0x3	RESERVED	Reserved

15.3 Debug and Test Block Diagrams

Figure 15-1: Debug and Test General Block Diagram

19.3.15 QSPI Clock Pad Supply Select Register

Name: QSPICLK_REG

Address: 0xF8030094

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SUP_SEL

SUP_SEL: Supply Selection

0: 1.8V supply selected.

1: 3.3V supply selected.

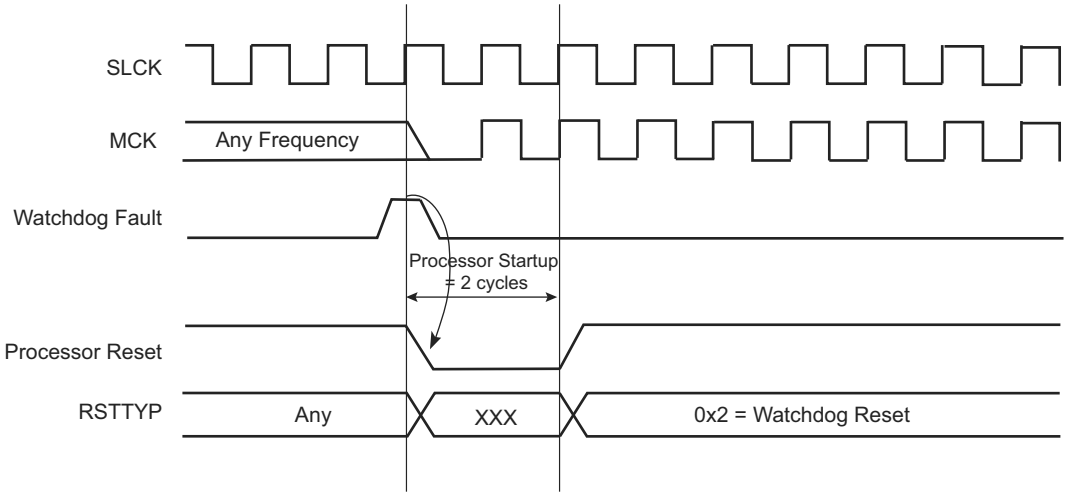
23.4.3.5 Watchdog Reset

The Watchdog Reset is entered when a watchdog fault occurs. This state lasts two Slow Clock cycles.

The Watchdog Timer is reset by the Processor Reset signal. As the watchdog fault always causes a processor reset if WDRSTEN is set, the Watchdog Timer is always reset after a Watchdog Reset and the Watchdog is enabled by default and with a period set to a maximum.

When the WDRSTEN in WDT_MR bit is reset, the watchdog fault has no impact on the reset controller.

Figure 23-7: Watchdog Reset



23.4.4 Reset State Priorities

The Reset State Manager manages the following priorities between the different reset sources, given in descending order:

- Backup Reset
- Wakeup Reset
- Watchdog Reset
- Software Reset
- User Reset

Particular cases are listed below:

- When in User Reset:
  - A watchdog event is impossible because the Watchdog Timer is being reset by the Processor Reset signal.
  - A Software Reset is impossible, since the processor reset is being activated.
- When in Software Reset:
  - A watchdog event has priority over the current state.
  - The NRST has no effect.
- When in Watchdog Reset:
  - The processor reset is active and so a Software Reset cannot be programmed.
  - A User Reset cannot be entered.

Value	Name	Description
5	H_122US	122 µs
6	H_30US	30.5 µs
7	H_15US	15.2 µs

TPERIOD: Period of the Output Pulse

Value	Name	Description
0	P_1S	1 second
1	P_500MS	500 ms
2	P_250MS	250 ms
3	P_125MS	125 ms

38.6 Linked List Descriptor Operation

38.6.1 Linked List Descriptor View

38.6.1.1 Channel Next Descriptor View 0–3 Structures

Table 38-4: Channel Next Descriptor View 0–3 Structures

Channel Next Descriptor	Offset	Structure member	Name
View 0 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Transfer Address Member	MBR_TA
View 1 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
View 2 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
	DSCR_ADDR+0x10	Configuration Register	MBR_CFG
View 3 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
	DSCR_ADDR+0x10	Configuration Member	MBR_CFG
	DSCR_ADDR+0x14	Block Control Member	MBR_BC
	DSCR_ADDR+0x18	Data Stride Member	MBR_DS
	DSCR_ADDR+0x1C	Source Microblock Stride Member	MBR_SUS
	DSCR_ADDR+0x20	Destination Microblock Stride Member	MBR_DUS

46.7.2 TWIHS Control Register (FIFO_ENABLED)

Name: TWIHS_CR (FIFO_ENABLED)

Address: 0xF8028000 (0), 0xFC028000 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	FIFODIS	FIFOEN	–	TXFLCLR	RXFCLR	TXFCLR
23	22	21	20	19	18	17	16
–	–	–	–	–	–	ACMDIS	ACMEN
15	14	13	12	11	10	9	8
CLEAR	PECRQ	PECDIS	PECEN	SMBDIS	SMBEN	HSDIS	HSEN
7	6	5	4	3	2	1	0
SWRST	QUICK	SVDIS	SVEN	MSDIS	MSEN	STOP	START

This configuration is relevant only if TWIHS_CR.FIFOEN = ‘1’.

START: Send a START Condition

0: No effect.

1: A frame beginning with a START bit is transmitted according to the features defined in the TWIHS Master Mode Register (TWIHS_MMR).

This action is necessary when the TWIHS peripheral needs to read data from a slave. When configured in Master mode with a write operation, a frame is sent as soon as the user writes a character in the Transmit Holding Register (TWIHS_THR).

STOP: Send a STOP Condition

0: No effect.

1: STOP condition is sent just after completing the current byte transmission in Master Read mode.

- In single data byte master read, both START and STOP must be set.
- In multiple data bytes master read, the STOP must be set after the last data received but one.
- In Master Read mode, if a NACK bit is received, the STOP is automatically performed.
- In master data write operation, a STOP condition will be sent after the transmission of the current data is finished.

MSEN: TWIHS Master Mode Enabled

0: No effect.

1: Enables the Master mode (MSDIS must be written to 0).

Note: Switching from Slave to Master mode is only permitted when TXCOMP = 1.

MSDIS: TWIHS Master Mode Disabled

0: No effect.

1: The Master mode is disabled, all pending data is transmitted. The shifter and holding characters (if it contains data) are transmitted in case of write operation. In read operation, the character being transferred must be completely received before disabling.

SVEN: TWIHS Slave Mode Enabled

0: No effect.

1: Enables the Slave mode (SVDIS must be written to 0).

Note: Switching from Master to Slave mode is only permitted when TXCOMP = 1.

SVDIS: TWIHS Slave Mode Disabled

0: No effect.

46.7.16 TWIHS Receive Holding Register (FIFO_ENABLED)

Name: TWIHS_RHR (FIFO_ENABLED)

Address: 0xF8028030 (0), 0xFC028030 (1)

Access: Read-only

31	30	29	28	27	26	25	24
RXDATA3							
23	22	21	20	19	18	17	16
RXDATA2							
15	14	13	12	11	10	9	8
RXDATA1							
7	6	5	4	3	2	1	0
RXDATA0							

Note: If FIFO is enabled (FIFOEN bit in TWIHS_CR), see Master Multiple Data Mode for details.

RXDATA0: Master or Slave Receive Holding Data 0

RXDATA1: Master or Slave Receive Holding Data 1

RXDATA2: Master or Slave Receive Holding Data 2

RXDATA3: Master or Slave Receive Holding Data 3

46.7.25 TWIHS FIFO Interrupt Mask Register

Name: TWIHS_FIMR

Address: 0xF802806C (0), 0xFC02806C (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXFPTEF	TXFPTEF	RXFTHF	RXFFF	RXFEF	TXFTHF	TXFFF	TXFEF

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

TXFEF: TXFEF Interrupt Mask

TXFFF: TXFFF Interrupt Mask

TXFTHF: TXFTHF Interrupt Mask

RXFEF: RXFEF Interrupt Mask

RXFFF: RXFFF Interrupt Mask

RXFTHF: RXFTHF Interrupt Mask

TXFPTEF: TXFPTEF Interrupt Mask

RXFPTEF: RXFPTEF Interrupt Mask

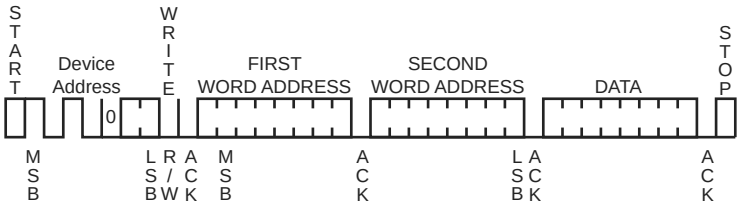
For a slave address higher than seven bits, the user must configure the address size **(**IADRSZ) and set the other slave address bits in the Internal Address Register (FLEX_TWI_IADR). The two remaining internal address bytes, IADR[15:8] and IADR[23:16], can be used the same way as in 7-bit slave addressing.

Example: Address a 10-bit device (10-bit device address is b1 b2 b3 b4 b5 b6 b7 b8 b9 b10)

1. Program IADRSZ = 1,
2. Program DADR with 1 1 1 1 0 b1 b2 (b1 is the MSB of the 10-bit address, b2, etc.)
3. Program FLEX_TWI_IADR with b3 b4 b5 b6 b7 b8 b9 b10 (b10 is the LSB of the 10-bit address)

Figure 47-93 shows a byte write to an AT24LC512 EEPROM. This demonstrates the use of internal addresses to access the device.

Figure 47-93: Internal Address Usage



47.9.3.7 Repeated Start

In addition to Internal Address mode, repeated start (Sr) can be generated manually by writing the START bit at the end of a transfer instead of the STOP bit. In such case the parameters of the next transfer (direction, SADR, etc.) will need to be set before writing the START bit at the end of the previous transfer.

See **Section 47.9.3.13 “Read/Write Flowcharts”** for detailed flowcharts.

Note that generating a repeated start after a single data read is not supported.

47.9.3.8 Bus Clear Command

The TWI interface can perform a Bus Clear Command:

1. Configure the Master mode (DADR, CKDIV, etc).
2. Start the transfer by setting the FLEX_TWI_CR.CLEAR bit.

Note: If an alternative command is used (ACMEN bit = 1), the DATAL field must be cleared.

47.9.3.9 SMBus Mode

SMBus mode is enabled when the FLEX_TWI_CR.SMBEN bit is written to one. SMBus mode operation is similar to I²C operation with the following exceptions:

1. Only 7-bit addressing can be used.
2. The SMBus standard describes a set of timeout values to ensure progress and throughput on the bus. These timeout values must be programmed into FLEX_TWI_SMBTR.
3. Transmissions can optionally include a CRC byte, called Packet Error Check (PEC).
4. A set of addresses has been reserved for protocol handling, such as alert response address (ARA) and host header (HH) address. Address matching on these addresses can be enabled by configuring FLEX_TWI_CR appropriately.

- Packet Error Checking

Each SMBus transfer can optionally end with a CRC byte, called the PEC byte. Writing the FLEX_TWI_CR.PECEN bit to one enables automatic PEC handling in the current transfer. Transfers with and without PEC can freely be intermixed in the same system, since some slaves may not support PEC. The PEC LFSR is always updated on every bit transmitted or received, so that PEC handling on combined transfers will be correct.

In Master Transmitter mode, the master calculates a PEC value and transmits it to the slave after all data bytes have been transmitted. Upon reception of this PEC byte, the slave will compare it to the PEC value it has computed itself. If the values match, the data was received correctly, and the slave will return an ACK to the master. If the PEC values differ, data was corrupted, and the slave will return a NACK value. Some slaves may not be able to check the received PEC in time to return a NACK if an error occurred. In this case, the slave should always return an ACK after the PEC byte, and some other mechanism must be implemented to verify that the transmission was received correctly.

47.10 Flexible Serial Communication Unit (FLEXCOM) User Interface

Table 47-18: Register Mapping

Offset	Register	Name	Access	Reset
0x000	FLEXCOM Mode Register	FLEX_MR	Read/Write	0x0
0x004–0x00C	Reserved	–	–	–
0x010	FLEXCOM Receive Holding Register	FLEX_RHR	Read-only	0x0
0x014–0x01C	Reserved	–	–	–
0x020	FLEXCOM Transmit Holding Register	FLEX_THR	Read/Write	0x0
0x024–0x0FC	Reserved	–	–	–
0x100–0x1FC	Reserved	–	–	–
0x200	USART Control Register	FLEX_US_CR	Write-only	–
0x204	USART Mode Register	FLEX_US_MR	Read/Write	–
0x208	USART Interrupt Enable Register	FLEX_US_IER	Write-only	–
0x20C	USART Interrupt Disable Register	FLEX_US_IDR	Write-only	–
0x210	USART Interrupt Mask Register	FLEX_US_IMR	Read-only	0x0
0x214	USART Channel Status Register	FLEX_US_CSR	Read-only	–
0x218	USART Receive Holding Register	FLEX_US_RHR	Read-only	0x0
0x21C	USART Transmit Holding Register	FLEX_US_THR	Write-only	–
0x220	USART Baud Rate Generator Register	FLEX_US_BRGR	Read/Write	0x0
0x224	USART Receiver Timeout Register	FLEX_US_RTOR	Read/Write	0x0
0x228	USART Transmitter Timeguard Register	FLEX_US_TTGR	Read/Write	0x0
0x22C–0x23C	Reserved	–	–	–
0x240	USART FI DI Ratio Register	FLEX_US_FIDI	Read/Write	0x174
0x244	USART Number of Errors Register	FLEX_US_NER	Read-only	–
0x248	Reserved	–	–	–
0x24C	USART IrDA Filter Register	FLEX_US_IF	Read/Write	0x0
0x250	USART Manchester Configuration Register	FLEX_US_MAN	Read/Write	0xB0011004
0x254	USART LIN Mode Register	FLEX_US_LINMR	Read/Write	0x0
0x258	USART LIN Identifier Register	FLEX_US_LINIR	Read/Write(1)	0x0
0x25C	USART LIN Baud Rate Register	FLEX_US_LINBRR	Read-only	0x0
0x260–0x288	Reserved	–	–	–
0x290	USART Comparison Register	FLEX_US_CMPR	Read/Write	0x0
0x2A0	USART FIFO Mode Register	FLEX_US_FMR	Read/Write	0x0
0x2A4	USART FIFO Level Register	FLEX_US_FLR	Read-only	0x0
0x2A8	USART FIFO Interrupt Enable Register	FLEX_US_FIER	Write-only	–
0x2AC	USART FIFO Interrupt Disable Register	FLEX_US_FIDR	Write-only	–
0x2B0	USART FIFO Interrupt Mask Register	FLEX_US_FIMR	Read-only	0x0

TXEMPTY: Transmitter Empty (cleared by writing FLEX_US_THR)

0: There are characters in either FLEX_US_THR or the Transmit Shift Register, or the transmitter is disabled.

1: There are no characters in FLEX_US_THR, nor in the Transmit Shift Register.

LINBK: LIN Break Sent or LIN Break Received

Applicable if USART operates in LIN Master mode (USART_MODE = 0xA):

0: No LIN break has been sent since the last RSTSTA command was issued.

1: At least one LIN break has been sent since the last RSTSTA.

If USART operates in LIN Slave mode (USART_MODE = 0xB):

0: No LIN break has received sent since the last RSTSTA command was issued.

1: At least one LIN break has been received since the last RSTSTA command was issued.

LINID: LIN Identifier Sent or LIN Identifier Received

If USART operates in LIN Master mode (USART_MODE = 0xA):

0: No LIN identifier has been sent since the last RSTSTA command was issued.

1: At least one LIN identifier has been sent since the last RSTSTA command was issued.

If USART operates in LIN Slave mode (USART_MODE = 0xB):

0: No LIN identifier has been received since the last RSTSTA command was issued.

1: At least one LIN identifier has been received since the last RSTSTA.

LINTC: LIN Transfer Completed

0: The USART is idle or a LIN transfer is ongoing.

1: A LIN transfer has been completed since the last RSTSTA command was issued.

LINBLS: LIN Bus Line Status

0: LIN bus line is set to 0.

1: LIN bus line is set to 1.

LINBE: LIN Bit Error

0: No bit error has been detected since the last RSTSTA command was issued.

1: A bit error has been detected since the last RSTSTA command was issued.

LINISFE: LIN Inconsistent Synch Field Error

0: No LIN inconsistent synch field error has been detected since the last RSTSTA

1: The USART is configured as a slave node and a LIN Inconsistent synch field error has been detected since the last RSTSTA command was issued.

LINIPE: LIN Identifier Parity Error

0: No LIN identifier parity error has been detected since the last RSTSTA command was issued.

1: A LIN identifier parity error has been detected since the last RSTSTA command was issued.

LINCE: LIN Checksum Error

0: No LIN checksum error has been detected since the last RSTSTA command was issued.

1: A LIN checksum error has been detected since the last RSTSTA command was issued.

LINSNRE: LIN Slave Not Responding Error

0: No LIN slave not responding error has been detected since the last RSTSTA command was issued.

1: A LIN slave not responding error has been detected since the last RSTSTA command was issued.

LINSTE: LIN Synch Tolerance Error

0: No LIN synch tolerance error has been detected since the last RSTSTA command was issued.

CMDIDX: Command Index Error

This bit is set to 1 if a Command Index error occurs in the command response.

This bit can only be set to 1 if SDMMC_EISTER.CMDIDX is set to 1. An interrupt can only be generated if SDMMC_EISIER.CMDIDX is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

DATTEO: Data Timeout Error

This bit is set to 1 when detecting one of following timeout conditions.

- Busy timeout for R1b, R5b response type (see “Physical Layer Simplified Specification V3.01” and “SDIO Simplified Specification V3.00”).
- Busy timeout after Write CRC status.
- Write CRC Status timeout.
- Read data timeout

This bit can only be set to 1 if SDMMC_EISTER.DATTEO is set to 1. An interrupt can only be generated if SDMMC_EISIER.DATTEO is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

DATCRC: Data CRC error

This bit is set to 1 when detecting a CRC error when transferring read data which uses the DAT line or when detecting that the Write CRC Status has a value other than “010”.

This bit can only be set to 1 if SDMMC_EISTER.DATCRC is set to 1. An interrupt can only be generated if SDMMC_EISIER.DATCRC is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

DATEND: Data End Bit Error

This bit is set to 1 either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status.

This bit can only be set to 1 if SDMMC_EISTER.DATEND is set to 1. An interrupt can only be generated if SDMMC_EISIER.DATEND is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

CURLIM: Current Limit Error

By setting SD Bus Power (SDBPWR) in SDMMC_PCR, the SDMMC is requested to supply power for the SD Bus. The SDMMC is protected from an illegal card by stopping power supply to the card, in which case this bit indicates a failure status. Reading 1 means the SDMMC is not supplying power to the card due to some failure. Reading 0 means that the SDMMC is supplying power and no error has occurred. The SDMMC may require some sampling time to detect the current limit.

This bit can only be set to 1 if SDMMC_EISTER.CURLIM is set to 1. An interrupt can only be generated if SDMMC_EISIER.CURLIM is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

52.6.2 ISC Control Disable Register 0

Name: ISC_CTRLDIS

Address: 0xF0008004

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	SWRST
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DISABLE

DISABLE: Capture Disable

0: Writing a zero to this bit has no effect.

1: Write one to end the capture at the next Vertical Synchronization Detection.

SWRST: Software Reset

0: Writing a zero to this bit has not effect.

1: Write one to perform a software reset of the interface.

52.6.25 ISC Color Correction RB OR Register

Name: ISC_CC_RB_OR

Address: 0xF0008080

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	ROFST				

23	22	21	20	19	18	17	16
ROFST							

15	14	13	12	11	10	9	8
–	–	–	–	RBGAIN			

7	6	5	4	3	2	1	0
RBGAIN							

RBGAIN: Blue Gain for Red Component (signed 12 bits, 1:3:8)

ROFST: Red Component Offset (signed 13 bits, 1:12:0)

52.6.42 ISC Contrast And Brightness Configuration Register

Name: ISC_CBC_CFG

Address: 0xF00083B8

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	CCIRMODE		CCIR

CCIR: CCIR656 Stream Enable

0: Raw mode

1: CCIR656 stream

CCIRMODE: CCIR656 Byte Ordering

Value	Name	Description
0	CBY	Byte ordering Cb0, Y0, Cr0, Y1
1	CRY	Byte ordering Cr0, Y0, Cb0, Y1
2	YCB	Byte ordering Y0, Cb0, Y1, Cr0
3	YCR	Byte ordering Y0, Cr0, Y1, Cb0

BCPC: RC Compare Effect on TIOBx

Value	Name	Description
0	NONE	None
1	SET	Set
2	CLEAR	Clear
3	TOGGLE	Toggle

BEEVT: External Event Effect on TIOBx

Value	Name	Description
0	NONE	None
1	SET	Set
2	CLEAR	Clear
3	TOGGLE	Toggle

BSWTRG: Software Trigger Effect on TIOBx

Value	Name	Description
0	NONE	None
1	SET	Set
2	CLEAR	Clear
3	TOGGLE	Toggle

CES: Counter Event Selection

The bit CES defines when the channel counter event occurs when the period is center-aligned (flag CHIDx in PWM Interrupt Status Register 1).

CALG = 0 (Left Alignment):

0/1: The channel counter event occurs at the end of the PWM period.

CALG = 1 (Center Alignment):

0: The channel counter event occurs at the end of the PWM period.

1: The channel counter event occurs at the end of the PWM period and at half the PWM period.

UPDS: Update Selection

When the period is center aligned, the bit UPDS defines when the update of the duty cycle, the polarity value/mode occurs after writing the corresponding update registers.

CALG = 0 (Left Alignment):

0/1: The update always occurs at the end of the PWM period after writing the update register(s).

CALG = 1 (Center Alignment):

0: The update occurs at the next end of the PWM period after writing the update register(s).

1: The update occurs at the next end of the PWM half period after writing the update register(s).

DPOLI: Disabled Polarity Inverted

0: When the PWM channel x is disabled (CHIDx(PWM_SR) = 0), the OCx output waveform is the same as the one defined by the CPOL bit.

1: When the PWM channel x is disabled (CHIDx(PWM_SR) = 0), the OCx output waveform is inverted compared to the one defined by the CPOL bit.

TCTS: Timer Counter Trigger Selection

0: The comparator of the channel x (OCx) is used as the trigger source for the Timer Counter (TC).

1: The counter events of the channel x is used as the trigger source for the Timer Counter (TC).

DTE: Dead-Time Generator Enable

0: The dead-time generator is disabled.

1: The dead-time generator is enabled.

DTHI: Dead-Time PWMHx Output Inverted

0: The dead-time PWMHx output is not inverted.

1: The dead-time PWMHx output is inverted.

DTLI: Dead-Time PWMLx Output Inverted

0: The dead-time PWMLx output is not inverted.

1: The dead-time PWMLx output is inverted.

PPM: Push-Pull Mode

0: The Push-Pull mode is disabled for channel x.

1: The Push-Pull mode is enabled for channel x.

63.6.2 TRNG Interrupt Enable Register

Name: TRNG_IER

Address: 0xFC01C010

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

DATRDY: Data Ready Interrupt Enable

0: No effect.

1: Enables the corresponding interrupt.