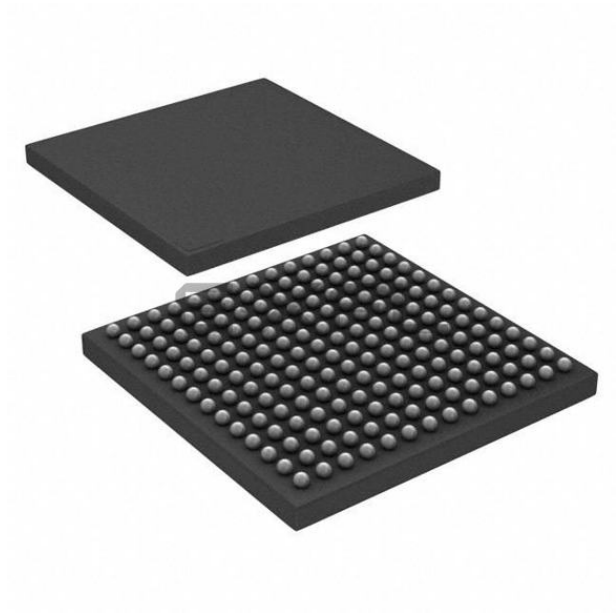

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d23a-cnr

13.4.4 CP 15 Register Access

CP15 registers can only be accessed in privileged mode by:

- MCR (Move to Coprocessor from ARM Register) instruction is used to write an ARM register to CP15.
- MRC (Move to ARM Register from Coprocessor) instruction is used to read the value of CP15 to an ARM register.

Other instructions such as CDP, LDC, STC can cause an undefined instruction exception.

The assembler code for these instructions is:

```
MCR/MRC{cond} p15, opcode_1, Rd, CRn, CRm, opcode_2.
```

The MCR/MRC instructions bit pattern is shown below:

31	30	29	28	27	26	25	24
cond				1	1	1	0

23	22	21	20	19	18	17	16
opcode_1			L	CRn			

15	14	13	12	11	10	9	8
Rd				1	1	1	1

7	6	5	4	3	2	1	0
opcode_2			1	CRm			

CRm[3:0]: Specified Coprocessor Action

Determines specific coprocessor action. Its value is dependent on the CP15 register used. For details, see CP15 specific register behavior.

opcode_2[7:5]

Determines specific coprocessor operation code. By default, set to 0.

Rd[15:12]: ARM Register

Defines the ARM register whose value is transferred to the coprocessor. If R15 is chosen, the result is unpredictable.

CRn[19:16]: Coprocessor Register

Determines the destination coprocessor register.

L: Instruction Bit

0: MCR instruction

1: MRC instruction

opcode_1[23:20]: Coprocessor Code

Defines the coprocessor specific code. Value is c15 for CP15.

cond [31:28]: Condition

13.4.5 Addresses in the Cortex-A5 processor

The Cortex-A5 processor operates using *virtual addresses* (VAs). The *Memory Management Unit* (MMU) translates these VAs into the *physical addresses* (PAs) used to access the memory system. Translation tables hold the mappings between VAs and PAs.

See the *ARM Architecture Reference Manual, ARMv7-A and ARMv7-R edition* for more information.

When the Cortex-A5 processor is executing in Non-secure state, the processor performs translation table look-ups using the Non-secure versions of the Translation Table Base Registers. In this situation, any VA can only translate into a Non-secure PA. When it is in Secure state, the Cortex-A5 processor performs translation table look-ups using the Secure versions of the Translation Table Base Registers. In this situation, the security state of any VA is determined by the NS bit of the translation table descriptors for that address.

Following is an example of the address manipulation that occurs when the Cortex-A5 processor requests an instruction:

21.9.18 AIC Interrupt Set Command Register

Name: AIC_ISCR

Address: 0xFC02004C (AIC), 0xF803C04C (SAIC)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	INTSET

INTSET: Interrupt Set

0: No effect.

1: Sets the interrupt source selected by INTSEL.

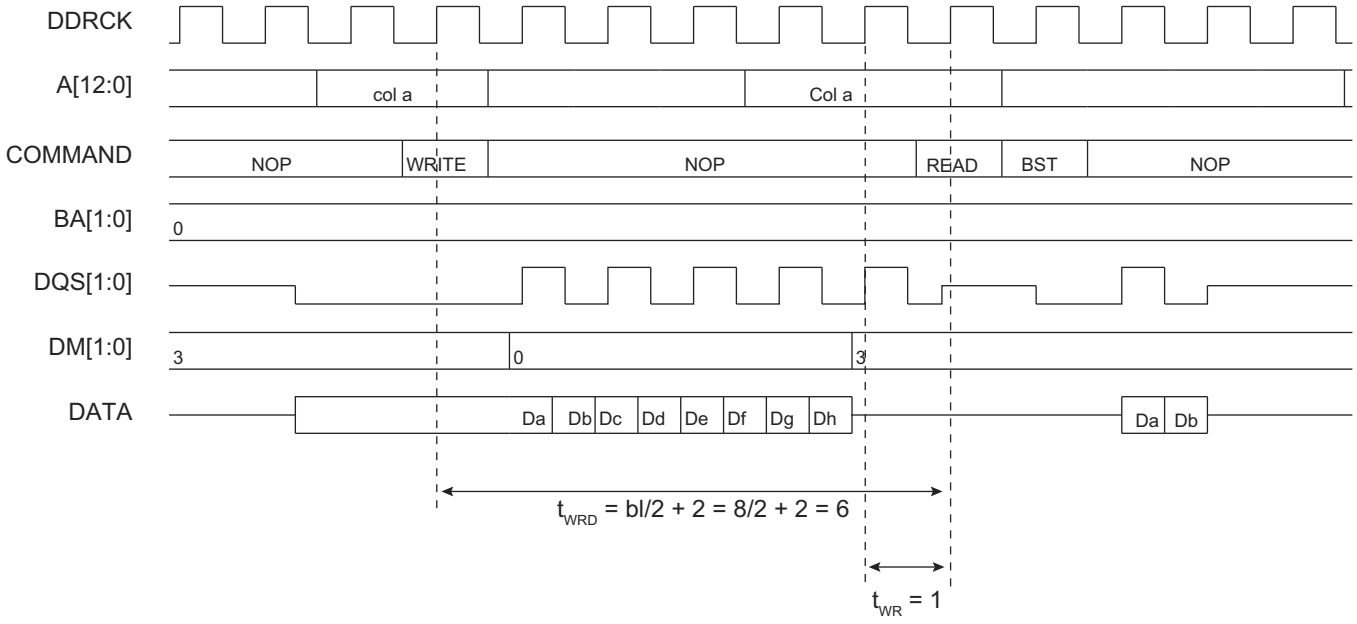
33.22 Power Management Controller (PMC) User Interface

Table 33-4: Register Mapping

Offset	Register	Name	Access	Reset
0x0000	System Clock Enable Register	PMC_SCER	Write-only	–
0x0004	System Clock Disable Register	PMC_SCDR	Write-only	–
0x0008	System Clock Status Register	PMC_SCSR	Read-only	0x0000_0005
0x000C	Reserved	–	–	–
0x0010	Peripheral Clock Enable Register 0	PMC_PCER0	Write-only	–
0x0014	Peripheral Clock Disable Register 0	PMC_PCDR0	Write-only	–
0x0018	Peripheral Clock Status Register 0	PMC_PCSR0	Read-only	0x0000_0000
0x001C	UTMI Clock Register	CKGR_UCKR	Read/Write	0x1020_0000
0x0020	Main Oscillator Register	CKGR_MOR	Read/Write	0x0100_0021
0x0024	Main Clock Frequency Register	CKGR_MCFR	Read/Write	0x0000_0000
0x0028	PLLA Register	CKGR_PLLAR	Read/Write	0x0000_3F00
0x002C	Reserved	–	–	–
0x0030	Master Clock Register	PMC_MCKR	Read/Write	0x0000_0001
0x0034	Reserved	–	–	–
0x0038	USB Clock Register	PMC_USB	Read/Write	0x0000_0000
0x003C	Reserved	–	–	–
0x0040	Programmable Clock 0 Register	PMC_PCK0	Read/Write	0x0000_0000
0x0044	Programmable Clock 1 Register	PMC_PCK1	Read/Write	0x0000_0000
0x0048	Programmable Clock 2 Register	PMC_PCK2	Read/Write	0x0000_0000
0x004C–0x005C	Reserved	–	–	–
0x0060	Interrupt Enable Register	PMC_IER	Write-only	–
0x0064	Interrupt Disable Register	PMC_IDR	Write-only	–
0x0068	Status Register	PMC_SR	Read-only	0x0001_0008
0x006C	Interrupt Mask Register	PMC_IMR	Read-only	0x0000_0000
0x0070	Fast Startup Mode Register	PMC_FSMR	Read/Write	0x0000_0000
0x0074	Fast Startup Polarity Register	PMC_FSPR	Read/Write	0x0000_0000
0x0078	Fault Output Clear Register	PMC_FOCR	Write-only	–
0x007C	Reserved	–	–	–
0x0080	PLL Charge Pump Current Register	PMC_PLLICPR	Read/Write	0x0000_0000
0x0084–0x00E0	Reserved	–	–	–
0x00E4	Write ProtectIon Mode Register	PMC_WPMR	Read/Write	0x0000_0000
0x00E8	Write Protection Status Register	PMC_WPSR	Read-only	0x0000_0000
0x00EC–0x00FC	Reserved	–	–	–
0x0100	Peripheral Clock Enable Register 1	PMC_PCER1	Write-only	–
0x0104	Peripheral Clock Disable Register 1	PMC_PCDR1	Write-only	–

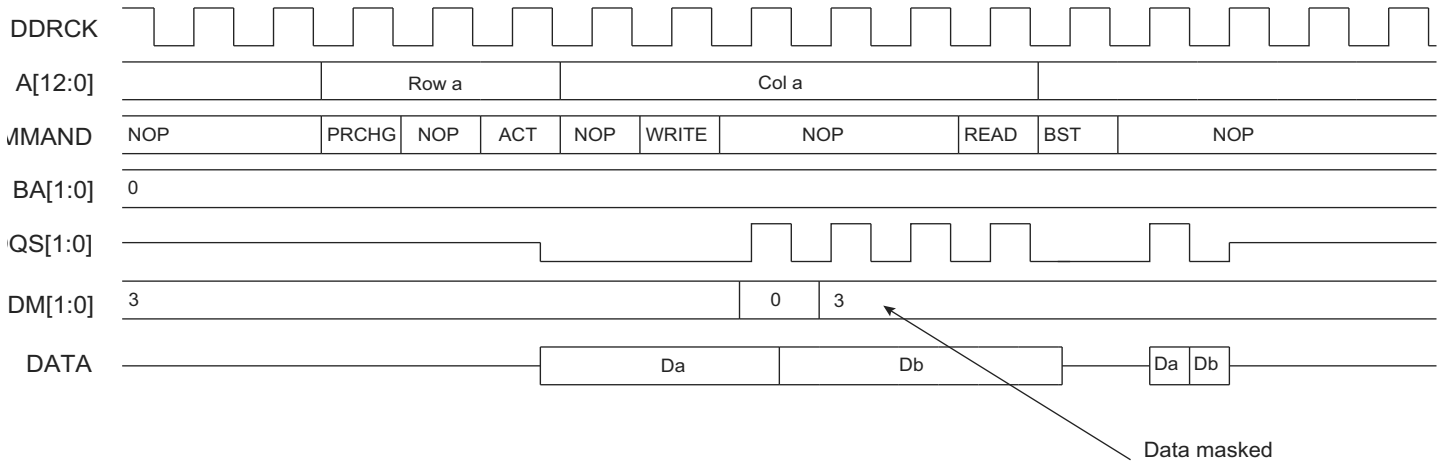
A write command can be followed by a read command. To avoid breaking the current write burst, t_{WTR}/t_{WRD} (bl/2 + 2 = 6 cycles) should be met. See Figure 36-6.

Figure 36-6: Write Command Followed by a Read Command without Burst Write Interrupt, DDR-SDRAM Devices



In case of a single write access, write operation should be interrupted by a read access but DM must be input 1 cycle prior to the read command to avoid writing invalid data. See Figure 36-7.

Figure 36-7: SINGLE Write Access Followed by a Read Access, DDR-SDRAM Devices



36.7.17 MPDDRC Timeout Register

Name: MPDDRC_TIMEOUT

Address: 0xF000C048

Access: Read/Write

31	30	29	28	27	26	25	24
TIMEOUT_P7				TIMEOUT_P6			
23	22	21	20	19	18	17	16
TIMEOUT_P5				TIMEOUT_P4			
15	14	13	12	11	10	9	8
TIMEOUT_P3				TIMEOUT_P2			
7	6	5	4	3	2	1	0
TIMEOUT_P1				TIMEOUT_P0			

TIMEOUT_Px: Timeout for Ports 0, 1, 2, 3, 4, 5, 6 and 7

Reset value is 0.

Some masters have the particularity to insert idle state between two accesses. This field defines the delay between two accesses on the same port in number of DDRCK(1) clock cycles before arbitration and handling the access over to another port.

This field is not used with round-robin and bandwidth arbitrations.

The number of cycles is between 1 and 15.

Note 1: DDRCK is the clock that drives the SDRAM device.

39.7.16 Base Layer Channel Enable Register

Name: LCDC_BASECHER

Address: 0xF0000040

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	A2QEN	UPDATEEN	CHEN

CHEN: Channel Enable

0: No effect

1: Enables the DMA channel

UPDATEEN: Update Overlay Attributes Enable

0: No effect

1: Updates windows attributes on the next start of frame.

A2QEN: Add To Queue Enable

0: No effect

1: Indicates that a valid descriptor has been written to memory, its memory location should be written to the DMA head pointer. The A2QSR status bit is set to one, and it is reset by hardware as soon as the descriptor pointed to by the DMA head pointer is added to the list.

40.6.18 Energy-efficient Ethernet Support

IEEE 802.3az adds support for energy efficiency to Ethernet. These are the key features of 802.3az:

- Allows a system's transmit path to enter a low power mode if there is nothing to transmit.
- Allows a PHY to detect whether its link partner's transmit path is in low power mode, therefore allowing the system's receive path to enter low power mode.
- Link remains up during lower power mode and no frames are dropped.
- Asymmetric, one direction can be in low power mode while the other is transmitting normally.
- LPI (Low Power Idle) signaling is used to control entry and exit to and from low power modes.
- LPI signaling can only take place if both sides have indicated support for it through auto-negotiation.

These are the key features of 802.3az operation:

- Low power control is done at the MII (reconciliation sublayer).
- As an architectural convenience in writing the 802.3az it is assumed that transmission is deferred by asserting carrier sense, in practice it will not be done this way. This system will know when it has nothing to transmit and only enter low power mode when it is not transmitting.
- LPI should not be requested unless the link has been up for at least one second.
- LPI is signaled on the transmit path by asserting 0x01 on txd with tx_en low and tx_er high.
- A PHY on seeing LPI requested on the MII will send the sleep signal before going quiet. After going quiet it will periodically transmit refresh signals.
- LPI mode ends by transmitting normal idle for the wake time. There is a default time for this but it can be adjusted in software using the Link Layer Discovery Protocol (LLDP) described in Clause 79 of 802.3az.
- LPI is indicated at the receive side when sleep and refresh signaling has been detected.

40.6.19 802.1Qav Support - Credit-based Shaping

A credit-based shaping algorithm is available on the two highest priority queues and is defined in the standard 802.1Qav: Forwarding and Queuing Enhancements for Time-Sensitive Streams. This allows traffic on these queues to be limited and to allow other queues to transmit.

Traffic shaping is enabled via the CBS (Credit Based Shaping) Control register. This enables a counter which stores the amount of transmit 'credit', measured in bytes that a particular queue has. A queue may only transmit if it has non-negative credit. If a queue has data to send, but is held off from doing as another queue is transmitting, then credit will accumulate in the credit counter at the rate defined in the IdleSlope register (GMAC_CBSISQx) for that queue.

portTransmitRate is the transmission rate, in bits per second, that the underlying MAC service that supports transmission through the Port provides. The value of this parameter is determined by the operation of the MAC.

IdleSlope is the rate of change of increasing credit when waiting to transmit and must be less than the value of the portTransmitRate.

The max value of IdleSlope (or sendSlope) is (portTransmitRate / bits_per_MII_Clock).

In case of 100Mbps, maximum IdleSlope = (100Mbps / 4) = 0x17D7840.

When this queue is transmitting, the credit counter is decremented at the rate of sendSlope, which is defined as (portTransmitRate - IdleSlope). A queue can accumulate negative credit when transmitting which will hold off any other transfers from that queue until credit returns to a non-negative value. No transfers are halted when a queue's credit becomes negative; it will accumulate negative credit until the transfer completes.

The highest priority queue always has priority regardless of which queue has the most credit.

40.6.20 LPI Operation in the GMAC

It is best to use firmware to control LPI. LPI operation happens at the system level. Firmware gives maximum control and flexibility of operation. LPI operation is straightforward and firmware should be capable of responding within the required timeframes.

Autonegotiation:

1. Indicate EEE capability using next page autonegotiation.

For the transmit path:

1. If the link has been up for 1 second and there is nothing being transmitted, write to the TXLPIEN bit in the Network Control register.
2. Wake up by clearing the TXLPIEN bit in the Network Control register.

For the receive path:

1. Enable RXLPISBC bit in GMAC_IER. The bit RXLPIS is set in Network Status Register triggering an interrupt.
2. Wait for an interrupt to indicate that LPI has been received.

40.8.50 GMAC Broadcast Frames Transmitted Register

Name: GMAC_BCFT

Address: 0xF800810C

Access: Read-only

31	30	29	28	27	26	25	24
BFTX							

23	22	21	20	19	18	17	16
BFTX							

15	14	13	12	11	10	9	8
BFTX							

7	6	5	4	3	2	1	0
BFTX							

BFTX: Broadcast Frames Transmitted without Error

Broadcast frames transmitted without error. This register counts the number of broadcast frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

40.8.82 GMAC Jabbers Received Register

Name: GMAC_JR

Address: 0xF800818C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	JRX	

7	6	5	4	3	2	1	0
JRX							

JRX: Jabbers Received

The register counts the number of frames received exceeding 1518 bytes in length (1536 if bit 8 is set in Network Configuration Register) and have either a CRC error, an alignment error or a receive symbol error. See Section 40.8.2 ”GMAC Network Configuration Register”.

41.7.5 UDPHS Clear Interrupt Register

Name: UDPHS_CLRINT

Address: 0xFC02C018

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
UPSTR_RES	ENDOFRSM	WAKE_UP	ENDRESET	INT_SOF	MICRO_SOF	DET_SUSPD	–

DET_SUSPD: Suspend Interrupt Clear

0: No effect.

1: Clear the DET_SUSPD bit in UDPHS_INTSTA.

MICRO_SOF: Micro Start Of Frame Interrupt Clear

0: No effect.

1: Clear the MICRO_SOF bit in UDPHS_INTSTA.

INT_SOF: Start Of Frame Interrupt Clear

0: No effect.

1: Clear the INT_SOF bit in UDPHS_INTSTA.

ENDRESET: End Of Reset Interrupt Clear

0: No effect.

1: Clear the ENDRESET bit in UDPHS_INTSTA.

WAKE_UP: Wake Up CPU Interrupt Clear

0: No effect.

1: Clear the WAKE_UP bit in UDPHS_INTSTA.

ENDOFRSM: End Of Resume Interrupt Clear

0: No effect.

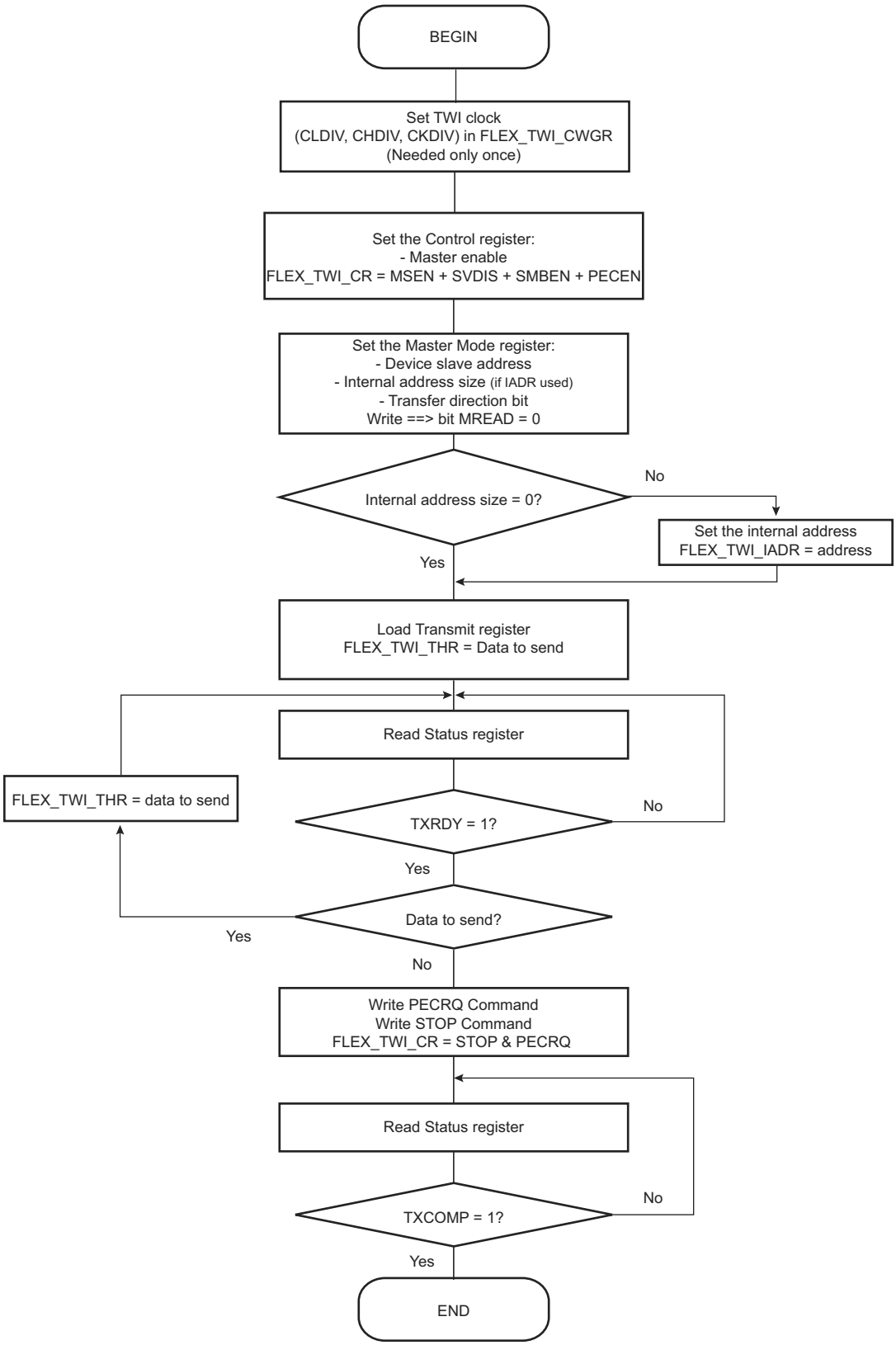
1: Clear the ENDOFRSM bit in UDPHS_INTSTA.

UPSTR_RES: Upstream Resume Interrupt Clear

0: No effect.

1: Clear the UPSTR_RES bit in UDPHS_INTSTA.

Figure 47-98: SMBus Write Operation with Multiple Data Bytes with or without Internal Address and PEC Sending



47.10.59 SPI Write Protection Status Register

Name: FLEX_SPI_WPSR

Address: 0xF80344E8 (0), 0xF80384E8 (1), 0xFC0104E8 (2), 0xFC0144E8 (3), 0xFC0184E8 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
WPVSRC							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPVS

WPVS: Write Protection Violation Status

0: No write protect violation has occurred since the last read of FLEX_SPI_WPSR.

1: A write protect violation has occurred since the last read of FLEX_SPI_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

WPVSRC: Write Protection Violation Source

When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

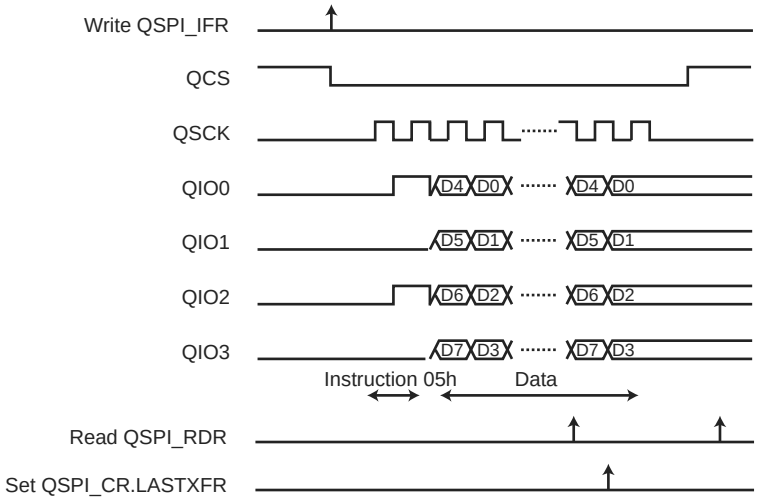
Example 10:

Instruction in Quad SPI, without address, without option, with data read in Quad SPI, without dummy cycles, without fetch, read launched through APB interface.

Command: HIGH-SPEED READ (05h)

- Set SMRM to ‘1’ in QSPI_MR
- Write 0x0000_0005 in QSPI_ICR.
- Write 0x0100_0096 in QSPI_IFR (will start the transfer).
- Wait flag RDRF and Read data in the QSPI_RDR register
  Fetch is disabled.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 50-20: Instruction Transmission Waveform 10



51.13.30 SDMMC Error Interrupt Signal Enable Register (e.MMC)

Name: SDMMC_EISIER (e.MMC)

Access: Read/Write

15	14	13	12	11	10	9	8
–	–	–	BOOTAE	–	–	ADMA	ACMD
7	6	5	4	3	2	1	0
CURLIM	DATEND	DATCRC	DATTEO	CMDIDX	CMDEND	CMDCRC	CMDTEO

CMDTEO: Command Timeout Error Signal Enable

0 (MASKED): No interrupt is generated when the CMDTEO status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the CMDTEO status rises in SDMMC_EISTR.

CMDCRC: Command CRC Error Signal Enable

0 (MASKED): No interrupt is generated when the CDMCRC status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the CMDCRC status rises in SDMMC_EISTR.

CMDEND: Command End Bit Error Signal Enable

0 (MASKED): No interrupt is generated when the CMDEND status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the CMDEND status rises in SDMMC_EISTR.

CMDIDX: Command Index Error Signal Enable

0 (MASKED): No interrupt is generated when the CMDIDX status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the CMDIDX status rises in SDMMC_EISTR.

DATTEO: Data Timeout Error Signal Enable

0 (MASKED): No interrupt is generated when the DATTEO status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the DATTEO status rises in SDMMC_EISTR.

DATCRC: Data CRC Error Signal Enable

0 (MASKED): No interrupt is generated when the DATCRC status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the DATCRC status rises in SDMMC_EISTR.

DATEND: Data End Bit Error Signal Enable

0 (MASKED): No interrupt is generated when the DATEND status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the DATEND status rises in SDMMC_EISTR.

CURLIM: Current Limit Error Signal Enable

0 (MASKED): No interrupt is generated when the CURLIM status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the CURLIM status rises in SDMMC_EISTR.

ACMD: Auto CMD Error Signal Enable

0 (MASKED): No interrupt is generated when the ACMD status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the ACMD status rises in SDMMC_EISTR.

ADMA: ADMA Error Signal Enable

0 (MASKED): No interrupt is generated when the ADMA status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the ADMA status rises in SDMMC_EISTR.

BOOTAE: Boot Acknowledge Error Signal Enable

0 (MASKED): No interrupt is generated when the BOOTAE status rises in SDMMC_EISTR.

1 (ENABLED): An interrupt is generated when the BOOTAE status rises in SDMMC_EISTR.

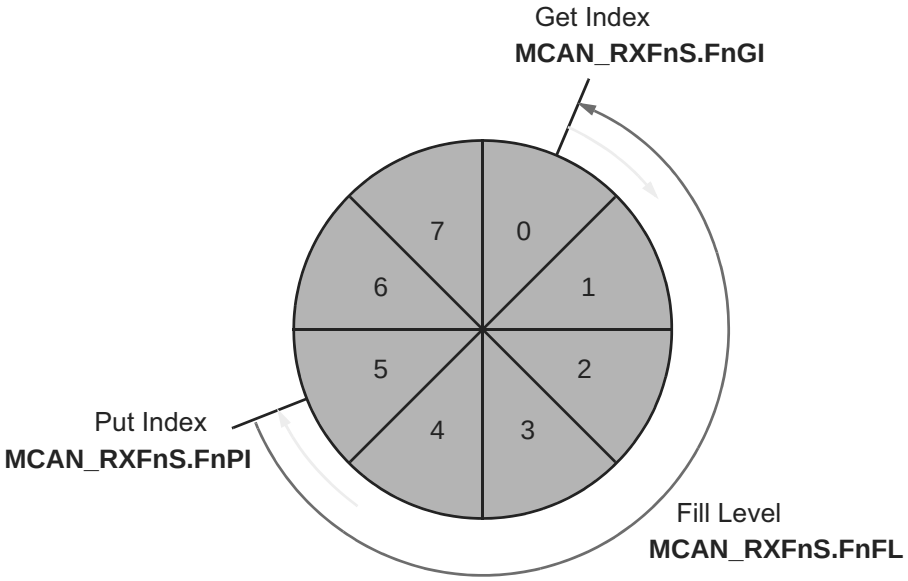
53.5.4.2 Rx FIFOs

Rx FIFO 0 and Rx FIFO 1 can be configured to hold up to 64 elements each. Configuration of the two Rx FIFOs is done via the Rx FIFO 0 Configuration register (MCAN_RXF0C) and the Rx FIFO 1 Configuration register (MCAN_RXF1C).

Received messages that passed acceptance filtering are transferred to the Rx FIFO as configured by the matching filter element. For a description of the filter mechanisms available for Rx FIFO 0 and Rx FIFO 1, see Section 53.5.4.1. The Rx FIFO element is described in Section 53.5.7.2.

To avoid an Rx FIFO overflow, the Rx FIFO watermark can be used. When the Rx FIFO fill level reaches the Rx FIFO watermark configured by MCAN_RXFnC.FnWM, interrupt flag MCAN_IR.RFnW is set. When the Rx FIFO Put Index reaches the Rx FIFO Get Index, an Rx FIFO Full condition is signalled by MCAN_RXFnS.FnF. In addition, the interrupt flag MCAN_IR.RFnF is set.

Figure 53-7: Rx FIFO Status



When reading from an Rx FIFO, Rx FIFO Get Index MCAN_RXFnS.FnGI × FIFO Element Size has to be added to the corresponding Rx FIFO start address MCAN_RXFnC.FnSA.

Table 53-4: Rx Buffer / FIFO Element Size

MCAN_RXESC.RBDS[2:0] MCAN_RXESC.FnDS[2:0]	Data Field [bytes]	FIFO Element Size [RAM words]
0	8	4
1	12	5
2	16	6
3	20	7
4	24	8
5	32	10
6	48	14
7	64	18

- Rx FIFO Blocking Mode

The Rx FIFO Blocking mode is configured by MCAN_RXFnC.FnOM = ‘0’. This is the default operating mode for the Rx FIFOs.

When an Rx FIFO full condition is reached (MCAN_RXFnS.FnPI = MCAN_RXFnS.FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signalled by MCAN_RXFnS.FnF = ‘1’. In addition, the interrupt flag MCAN_IR.RFnF is set.

53.6.34 MCAN Receive Buffer / FIFO Element Size Configuration

Name: MCAN_RXESC

Address: 0xF80540BC (0), 0xFC0500BC (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	RBDS		
7	6	5	4	3	2	1	0
–	F1DS			–	F0DS		

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Configures the number of data bytes belonging to a Receive Buffer / Receive FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

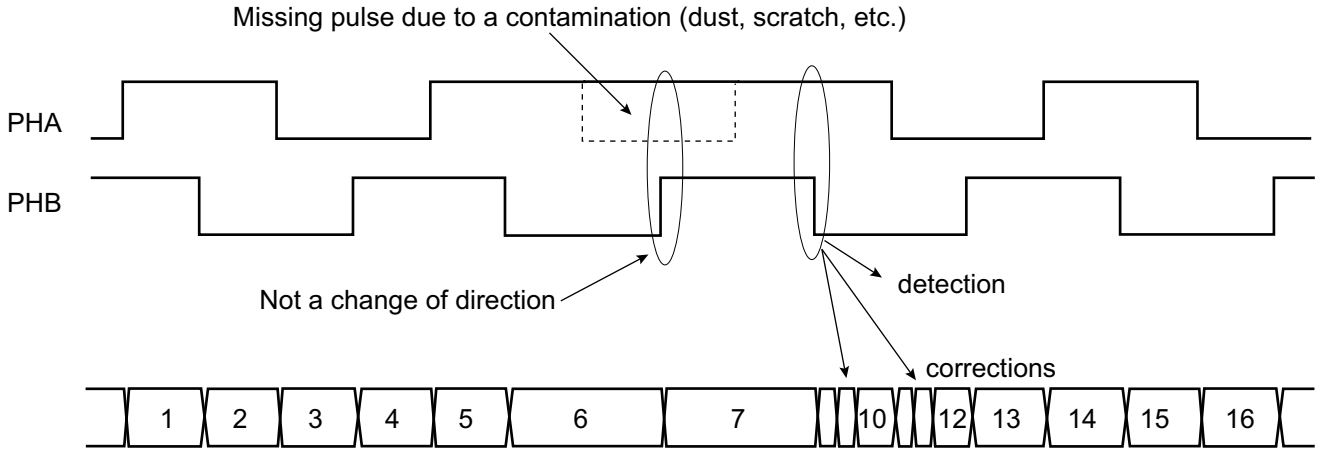
F0DS: Receive FIFO 0 Data Field Size

Value	Name	Description
0	8_BYTE	8-byte data field
1	12_BYTE	12-byte data field
2	16_BYTE	16-byte data field
3	20_BYTE	20-byte data field
4	24_BYTE	24-byte data field
5	32_BYTE	32-byte data field
6	48_BYTE	48-byte data field
7	64_BYTE	64-byte data field

F1DS: Receive FIFO 1 Data Field Size

Value	Name	Description
0	8_BYTE	8-byte data field
1	12_BYTE	12-byte data field
2	16_BYTE	16-byte data field
3	20_BYTE	20-byte data field
4	24_BYTE	24-byte data field
5	32_BYTE	32-byte data field
6	48_BYTE	48-byte data field
7	64_BYTE	64-byte data field

Figure 54-22: Detection and Autocorrection of Missing Pulses



If a quadrature device is undamaged, the number of pulses counted for a predefined period of time must be the same with or without detection and autocorrection feature.

Therefore, if the measurement results differ, a contamination exists on the device producing the quadrature signals.

This does not substitute the measurements of the number of pulses between two index pulses (if available) but provides a complementary method to detect damaged quadrature devices.

When the device providing quadrature signals is severely damaged, potentially leading to a number of consecutive missing pulses greater than 1, the downstream processing may be affected. It is possible to define the maximum admissible number of consecutive missing pulses before issuing a Missing Pulse Error flag (TC_QISR.MPE). The threshold triggering a MPE flag report can be configured in TC_BMR.MAXCMP. If the field MAXCMP is cleared, MPE never rises. The flag MAXCMP can trigger an interrupt while the QDEC is operating, thus providing a real time report of a potential problem on the quadrature device.

54.6.17 2-bit Gray Up/Down Counter for Stepper Motor

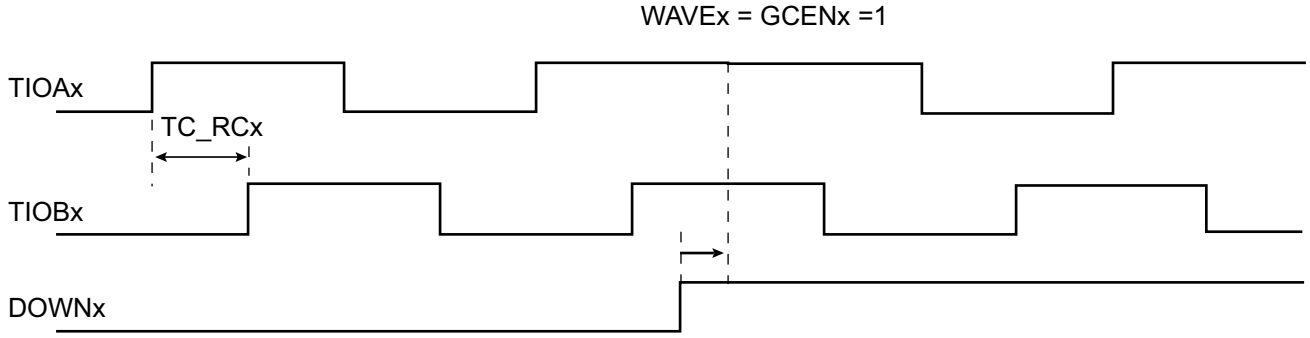
Each channel can be independently configured to generate a 2-bit Gray count waveform on corresponding TIOAx, TIOBx outputs by means of TC_SMMRx.GCEN.

Up or Down count can be defined by writing TC_SMMRx.DOWN.

It is mandatory to configure the channel in Waveform mode in the TC_CMR.

The period of the counters can be programmed in TC_RCx.

Figure 54-23: 2-bit Gray Up/Down Counter



54.6.18 Fault Mode

At any time, the TC_RCx registers can be used to perform a comparison on the respective current channel counter value (TC_CVx) with the value of TC_RCx register.

The CPCSx flags can be set accordingly and an interrupt can be generated.

This interrupt is processed but requires an unpredictable amount of time to be achieve the required action.

60.4.2 Operating Modes

The AES supports the following modes of operation:

- ECB: Electronic Codebook
- CBC: Cipher Block Chaining
- OFB: Output Feedback
- CFB: Cipher Feedback
  - CFB8 (CFB where the length of the data segment is 8 bits)
  - CFB16 (CFB where the length of the data segment is 16 bits)
  - CFB32 (CFB where the length of the data segment is 32 bits)
  - CFB64 (CFB where the length of the data segment is 64 bits)
  - CFB128 (CFB where the length of the data segment is 128 bits)
- CTR: Counter
- GCM: Galois/Counter Mode

The data preprocessing, data postprocessing and data chaining for the concerned modes are performed automatically. Refer to the *NIST Special Publication 800-38A* and *NIST Special Publication 800-38D* for more complete information.

Mode selection is done by configuring the OPMOD field in AES_MR.

In CFB mode, five data sizes are possible (8, 16, 32, 64 or 128 bits), configurable by means of AES_MR.CFBS (Section 60.5.2 “AES Mode Register”).

In CTR mode, the size of the block counter embedded in the module is 16 bits. Therefore, there is a rollover after processing 1 Mbyte of data. If the file to be processed is greater than 1 Mbyte, this file must be split into fragments of 1 Mbyte or less for the first fragment if the initial value of the counter is greater than 0. Prior to loading the first fragment into AES_IDATARx, AES_IVRx must be fully programmed with the initial counter value. For any fragment, after the transfer is completed and prior to transferring the next fragment, AES_IVRx must be programmed with the appropriate counter value.

60.4.3 Double Input Buffer

AES_IDATARx can be double-buffered to reduce the runtime of large files.

This mode allows a new message block to be written when the previous message block is being processed. This is only possible when DMA accesses are performed (AES_MR.SMOD = 2).

AES_MR.DUALBUFF must be set to ‘1’ to access the double buffer.

60.4.4 Start Modes

AES_MR.SMOD allows selection of the encryption (or decryption) Start mode.

60.4.4.1 Manual Mode

The sequence of actions is as follows:

1. Write AES_MR with all required fields, including but not limited to SMOD and OPMOD.
2. Write the 128-bit/192-bit/256-bit AES key in AES_KEYWRx.
3. Write the initialization vector (or counter) in AES_IVRx.

   Note: AES_IVRx concerns all modes except ECB.
4. Set the bit DATRDY (Data Ready) in the AES Interrupt Enable register (AES_IER), depending on whether an interrupt is required or not at the end of processing.
5. Write the data to be encrypted/decrypted in the authorized AES_IDATARx (see Table 60-2).
6. Set the START bit in the AES Control register (AES_CR) to begin the encryption or the decryption process.
7. When processing completes, the DATRDY flag in the AES Interrupt Status register (AES_ISR) is raised. If an interrupt has been enabled by setting AES_IER.DATRDY, the interrupt line of the AES is activated.
8. When software reads one of AES_ODATARx, AES_IER.DATRDY is automatically cleared.

Table 60-2: Authorized Input Data Registers

Operating Mode	Input Data Registers to Write
ECB	All
CBC	All

61.5.10 SHA Input/Output Data Register x

Name: SHA_IODATARx [x=0..15]

Address: 0xF0028080

Access: Read/Write

31	30	29	28	27	26	25	24
IODATA							

23	22	21	20	19	18	17	16
IODATA							

15	14	13	12	11	10	9	8
IODATA							

7	6	5	4	3	2	1	0
IODATA							

IODATA: Input/Output Data

These registers can be used to read the resulting message digest and to write the second part of the message block when the SHA algorithm is SHA-384 or SHA-512.

SHA_IODATA0R to SHA_IODATA15R can be written or read but reading these offsets does not return the content of corresponding parts (words) of the message block. Only results from SHA calculation can be read through these registers.

When SHA processing is in progress, these registers return 0x0000.

SHA_IODATAR0 corresponds to the first word of the message digest; SHA_IODATAR4 to the last one in SHA1 mode, SHA_ODATAR6 in SHA224, SHA_IODATAR7 in SHA256, SHA_IODATAR11 in SHA384 or SHA_IODATAR15 in SHA512.

When SHA224 is selected, the content of SHA_ODATAR7 must be ignored.

When SHA384 is selected, the content of SHA_IODATAR12 to SHA_IODATAR15 must be ignored.

Figure 66-10: SMC Timings - NCS Controlled Read and Write

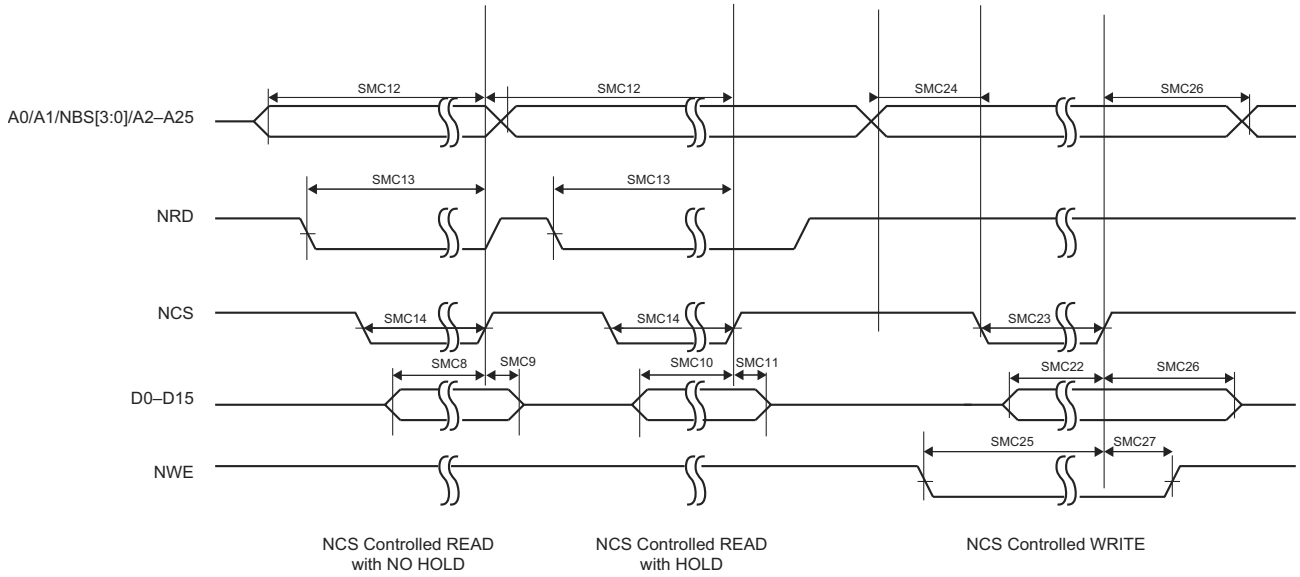
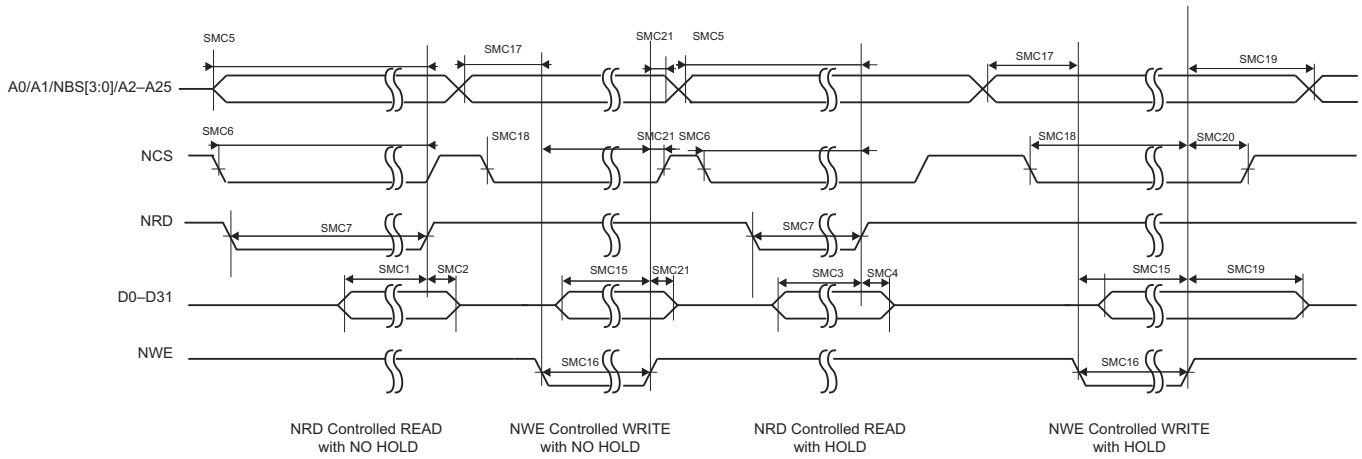


Figure 66-11: SMC Timings - NRD Controlled Read and NWE Controlled Write



66.15 FLEXCOM Timings

66.15.1 FLEXCOM USART in Asynchronous Modes

Refer to Section 66.16 “USART in Asynchronous Modes”.

66.15.2 FLEXCOM SPI Timings

66.15.2.1 Timing Conditions

Timings assuming a capacitance load on MISO, SPCK and MOSI are given in Table 66-63.

Table 66-52: Capacitance Load for MISO, SPCK and MOSI (FLEXCOM 0, 1, 2, 3, 4)

	Corner	
Supply	**Max**	**Min**
3.3V	40 pF	5 pF
1.8V	20 pF	5 pF