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Understanding Embedded - Microprocessors

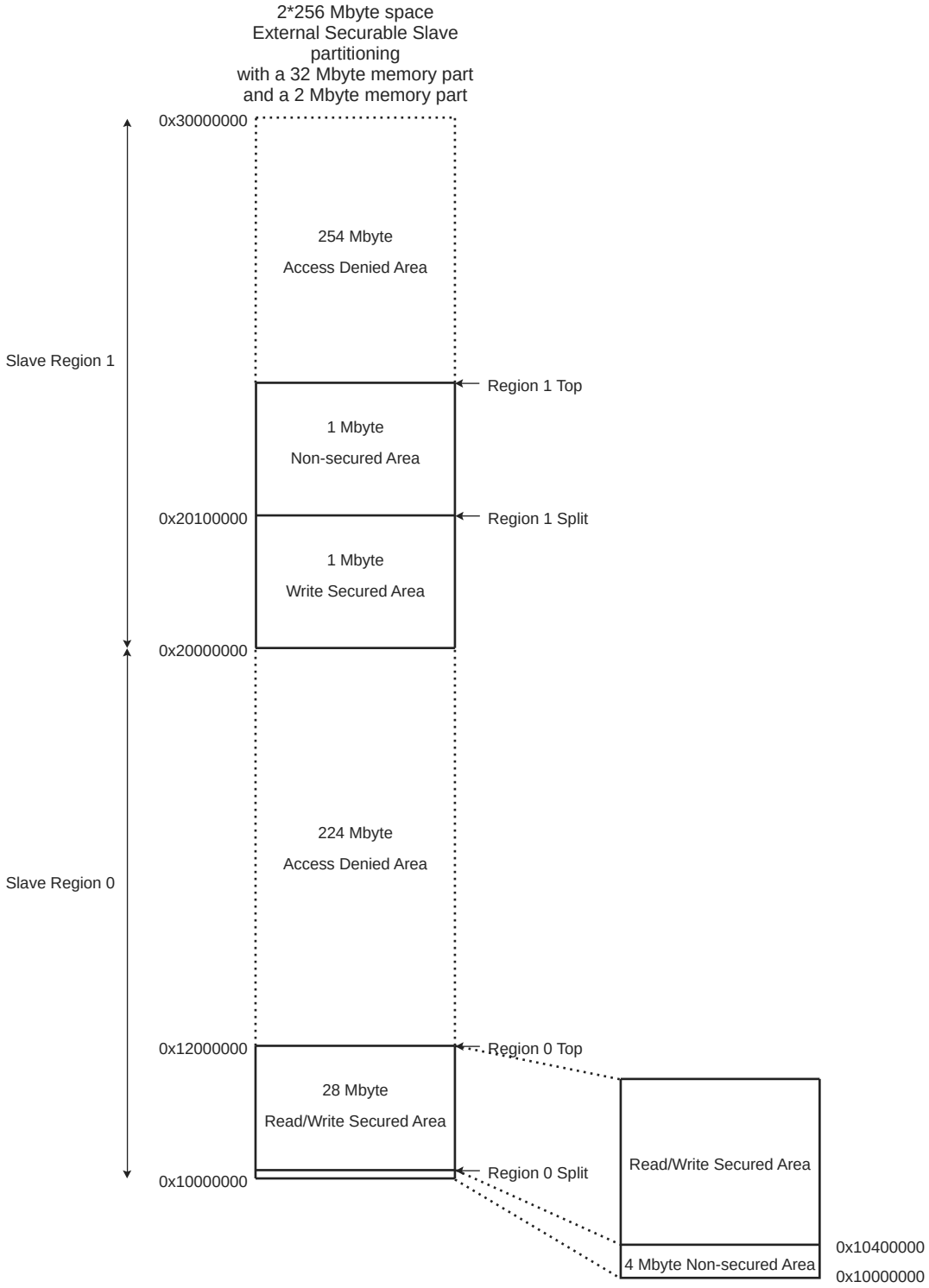
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d23b-cnr

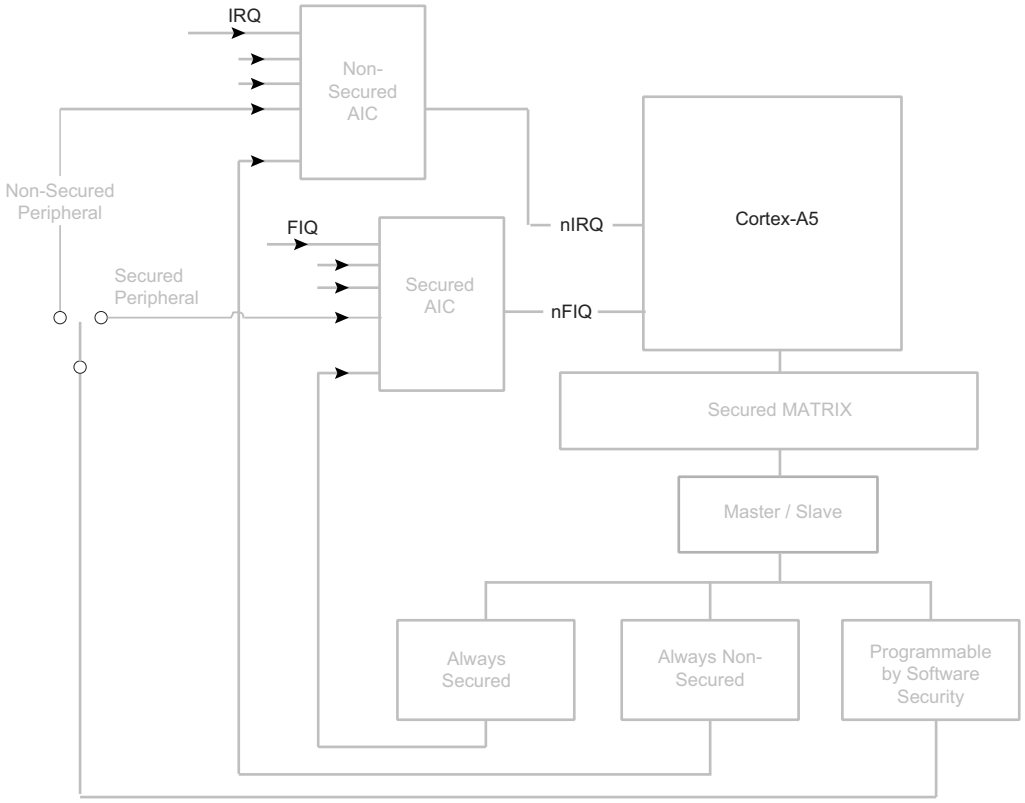
Figure 18-3: Partitioning Example of an External Securable Slave Featuring 2 Security Regions of 4 Kbytes to 128 Mbytes each and up to 4 Security Areas of 4 Kbytes to 128 Mbytes



Note: The slave region sizes are configured by writing into the Security Region Top Slave Registers.
The slave security area split inside each region is configured by writing into the Security Areas Split Slave Registers.

21.5 AIC Detailed Block Diagram

Figure 21-3: AIC Detailed Block Diagram



21.6 I/O Line Description

Table 21-1: I/O Line Description

Pin Name	Pin Description	Type
FIQ	Fast Interrupt	Input
IRQ0–IRQn	Interrupt 0–Interrupt n	Input

TZQIO: IO Calibration

This field defines the delay between the start up of the amplifier and the beginning of the calibration in number of DDRCK(1) clock cycles. The value of this field must be set to 600 ns.

The number of cycles is between 0 and 127.

The TZQIO configuration code must be set correctly depending on the clock frequency using the following formula:

TZQIO = (DDRCK × 600e-9) + 1

where DDRCK frequency is in Hz.

For example, for a frequency of 176 MHz, the value of the TZQIO field is configured (176 × 10e6) × (600e-9) + 1.

EN_CALIB: Enable Calibration

Reset value is 0.

This field enables calibration for the LPDDR1 and DDR2 devices. When the calibration is enabled, it is recommended to define the COUNT_CAL field (see “COUNT_CAL: LPDDR2 LPDDR3 and DDR3 Calibration Timer Count”).

This 16-bit field is loaded into a timer which generates the calibration pulse. Each time the calibration pulse is generated, a calibration sequence is initiated.

Value	Name	Description
0	DISABLE_CALIBRATION	Calibration is disabled.
1	ENABLE_CALIBRATION	Calibration is enabled.

CALCODEP: Number of Transistor P (read-only)

Reset value is 7.

This value gives the number of transistor P to perform the calibration.

CALCODEN: Number of Transistor N (read-only)

Reset value is 8.

This value gives the number of transistor N to perform the calibration.

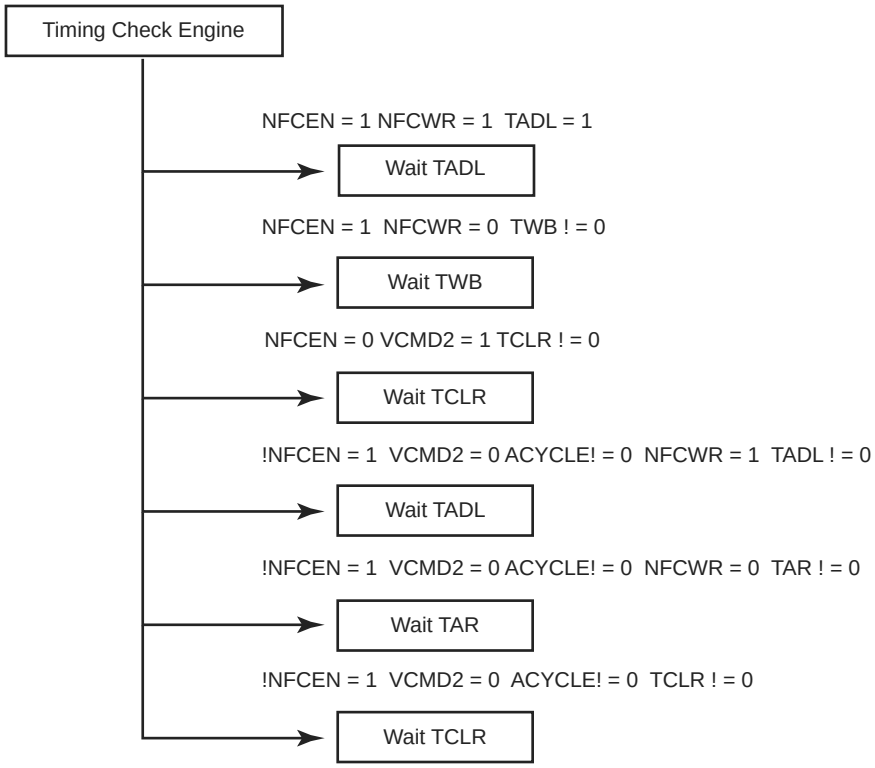
Note 1: DDRCK is the clock that drives the SDRAM device.

37.17.3.1 NFC Timing Engine

When the NFC Command register is written, the NFC issues a NAND Flash Command and optionally performs a data transfer between the NFC SRAM and the NAND Flash device. The NFC Timing Engine guarantees valid NAND Flash timings, depending on the set of parameters decoded from the address bus. These timings are defined in the HSMC_TIMINGS register.

For information on the timing used depending on the command, see Figure 37-36.

Figure 37-36: NFC Timing Engine



See the NFC Address Command register description and the Timings Register.

39.7.142 Post Processing Interrupt Mask Register

Name: LCDC_PPIMR

Address: 0xF0000554

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	DONE	ADD	DSCR	DMA	–	–

DMA: End of DMA Transfer Interrupt Mask

0: Interrupt source is disabled

1: Interrupt source is enabled

DSCR: Descriptor Loaded Interrupt Mask

0: Interrupt source is disabled

1: Interrupt source is enabled

ADD: Head Descriptor Loaded Interrupt Mask

0: Interrupt source is disabled

1: Interrupt source is enabled

DONE: End of List Interrupt Mask

0: Interrupt source is disabled

1: Interrupt source is enabled

39.7.157 High-End Overlay CLUT Register x

Name: LCDC_HEOCLUTx [x=0..255]

Address: 0xF0001200

Access: Read/Write

31	30	29	28	27	26	25	24
ACLUT							

23	22	21	20	19	18	17	16
RCLUT							

15	14	13	12	11	10	9	8
GCLUT							

7	6	5	4	3	2	1	0
BCLUT							

BCLUT: Blue Color Entry

This field indicates the 8-bit width Blue color of the color lookup table.

GCLUT: Green Color Entry

This field indicates the 8-bit width Green color of the color lookup table.

RCLUT: Red Color Entry

This field indicates the 8-bit width Red color of the color lookup table.

ACLUT: Alpha Color Entry

This field indicates the 8-bit width Alpha channel of the color lookup table.

REGA: Register Address

Specifies the register in the PHY to access.

PHYA: PHY Address

OP: Operation

01: Write

10: Read

CLTTO: Clause 22 Operation

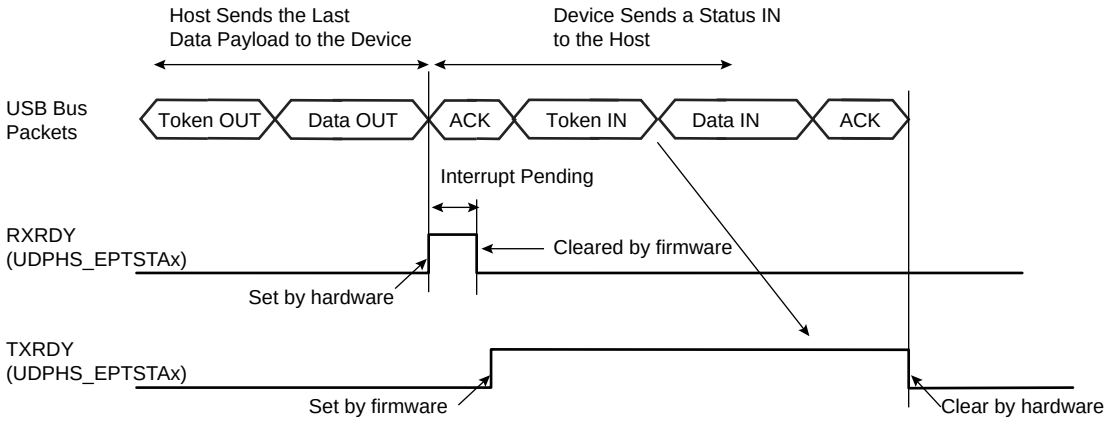
0: Clause 45 operation

1: Clause 22 operation

WZO: Write ZERO

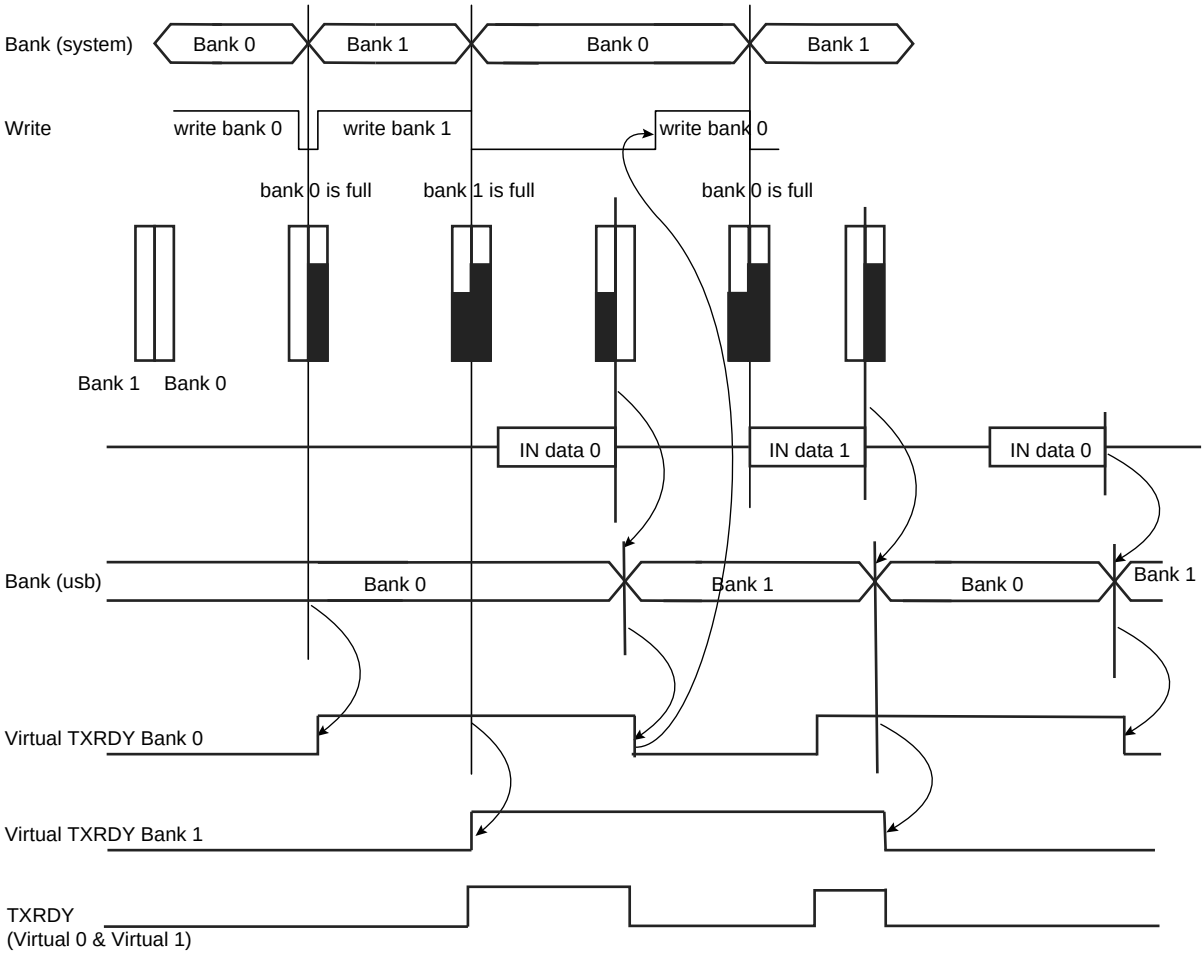
Must be written with 0.

Figure 41-12: Data OUT Followed by Status IN Transfer



Note: Before proceeding to the status stage, the software should determine that there is no risk of extra data from the host (data stage). If not certain (non-predictable data stage length), then the software should wait for a NAK-IN interrupt before proceeding to the status stage. This precaution should be taken to avoid collision in the FIFO.

Figure 41-13: Autovalid with DMA



Note: In the illustration above Autovalid validates a bank as full, although this might not be the case, in order to continue processing data and to send to DMA.

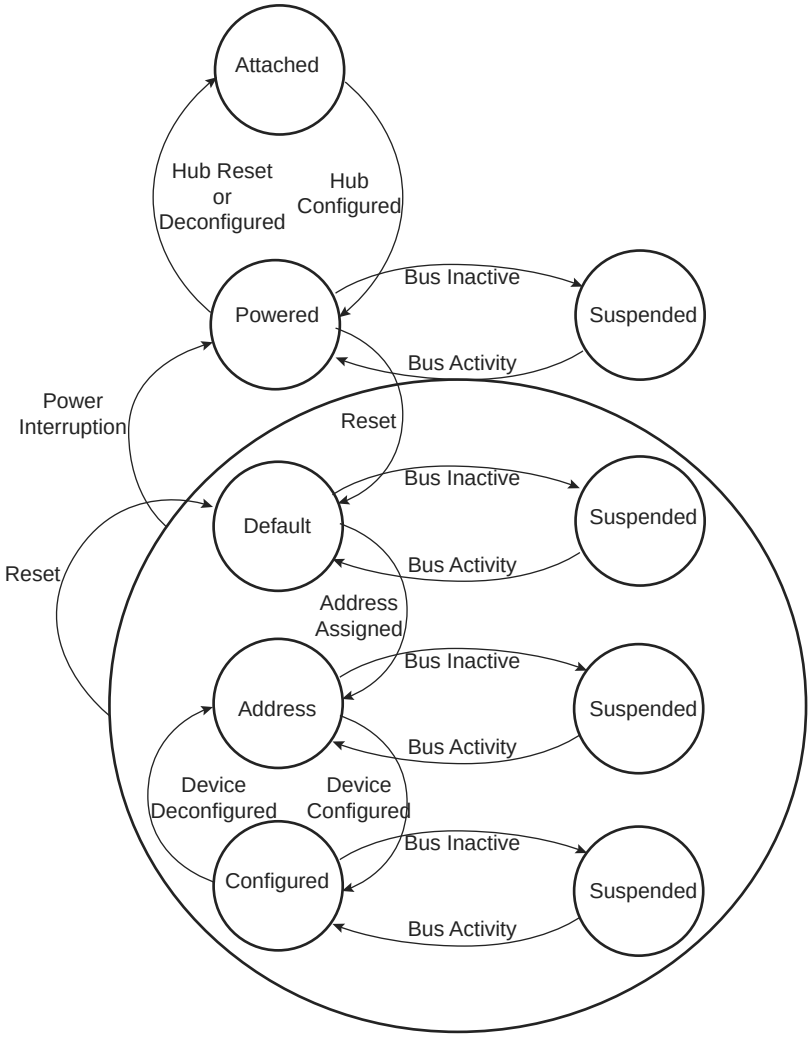
- Isochronous IN

41.6.14 Power Modes

41.6.14.1 Controlling Device States

A USB device has several possible states. Refer to Chapter 9 (USB Device Framework) of the Universal Serial Bus Specification, Rev 2.0.

Figure 41-20: UDPHS Device State Diagram



Movement from one state to another depends on the USB bus state or on standard requests sent through control transactions via the default endpoint (endpoint 0).

After a period of bus inactivity, the USB device enters Suspend mode. Accepting Suspend/Resume requests from the USB host is mandatory. Constraints in Suspend mode are very strict for bus-powered applications; devices may not consume more than 500 µA on the USB bus.

While in Suspend mode, the host may wake up a device by sending a resume signal (bus activity) or a USB device may send a wakeup request to the host, e.g., waking up a PC by moving a USB mouse.

The wakeup feature is not mandatory for all devices and must be negotiated with the host.

41.6.14.2 Not Powered State

Self powered devices can detect 5V VBUS using a PIO. When the device is not connected to a host, device power consumption can be reduced by the DETACH bit in UDPHS_CTRL. Disabling the transceiver is automatically done. HSDM, HSDP, FSDP and FSDP lines are tied to GND pulldowns integrated in the hub downstream ports.

PED: Port Enabled/Disabled (read/write)

0: Disable (default value).

1: Enable.

Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this field. The host controller will only set this bit to 1 when the reset sequence determines that the attached device is a high-speed device.

Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events.

When the port is disabled (0b), downstream propagation of data is blocked on this port, except for reset.

This field is 0 if Port Power is 0.

PEDC: Port Enable/Disable Change (read/write clear)

0: No change (default value).

1: Port enabled/disabled status has changed.

For the root hub, this bit gets set to 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it.

This field is 0 if Port Power is 0.

OCA: Over-current Active (read-only)

0: This port does not have an over-current condition (default value).

1: This port currently has an over-current condition.

This bit will automatically transition from 1 to 0 when the over current condition is removed.

OCC: Over-current Change (read/write clear)

0: Default value.

1: This bit gets set to 1 when there is a change to Over-current Active.

Software clears this bit by writing 1 to this bit position.

FPR: Force Port Resume (read/write)

0: No resume (K-state) detected/driven on port (default value).

1: Resume detected/driven on port.

This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are set to 1) and software transitions this bit to 1, then the effects on the bus are undefined.

Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to 1 because a J-to-K transition is detected, the Port Change Detect bit in the UHPHS_USBSTS register is also set to 1. If software sets this bit to 1, the host controller must not set the Port Change Detect bit.

Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains set to 1. Software must appropriately time the Resume and set this bit to 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to High-Speed mode (forcing the bus below the port into a high-speed idle).This bit will remain set to 1 until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to 0.

This field is 0 if Port Power is 0.

SUS: Suspend (read/write)

0: Port not in suspend state (default value).

1: Port in suspend state.

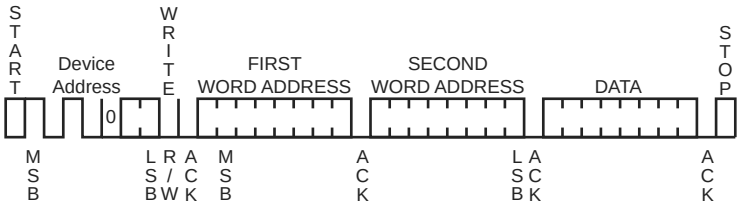
For a slave address higher than seven bits, the user must configure the address size **(**IADRSZ) and set the other slave address bits in the Internal Address Register (FLEX_TWI_IADR). The two remaining internal address bytes, IADR[15:8] and IADR[23:16], can be used the same way as in 7-bit slave addressing.

Example: Address a 10-bit device (10-bit device address is b1 b2 b3 b4 b5 b6 b7 b8 b9 b10)

1. Program IADRSZ = 1,
2. Program DADR with 1 1 1 1 0 b1 b2 (b1 is the MSB of the 10-bit address, b2, etc.)
3. Program FLEX_TWI_IADR with b3 b4 b5 b6 b7 b8 b9 b10 (b10 is the LSB of the 10-bit address)

Figure 47-93 shows a byte write to an AT24LC512 EEPROM. This demonstrates the use of internal addresses to access the device.

Figure 47-93: Internal Address Usage



47.9.3.7 Repeated Start

In addition to Internal Address mode, repeated start (Sr) can be generated manually by writing the START bit at the end of a transfer instead of the STOP bit. In such case the parameters of the next transfer (direction, SADR, etc.) will need to be set before writing the START bit at the end of the previous transfer.

See **Section 47.9.3.13 “Read/Write Flowcharts”** for detailed flowcharts.

Note that generating a repeated start after a single data read is not supported.

47.9.3.8 Bus Clear Command

The TWI interface can perform a Bus Clear Command:

1. Configure the Master mode (DADR, CKDIV, etc).
2. Start the transfer by setting the FLEX_TWI_CR.CLEAR bit.

Note: If an alternative command is used (ACMEN bit = 1), the DATAL field must be cleared.

47.9.3.9 SMBus Mode

SMBus mode is enabled when the FLEX_TWI_CR.SMBEN bit is written to one. SMBus mode operation is similar to I²C operation with the following exceptions:

1. Only 7-bit addressing can be used.
2. The SMBus standard describes a set of timeout values to ensure progress and throughput on the bus. These timeout values must be programmed into FLEX_TWI_SMBTR.
3. Transmissions can optionally include a CRC byte, called Packet Error Check (PEC).
4. A set of addresses has been reserved for protocol handling, such as alert response address (ARA) and host header (HH) address. Address matching on these addresses can be enabled by configuring FLEX_TWI_CR appropriately.

- Packet Error Checking

Each SMBus transfer can optionally end with a CRC byte, called the PEC byte. Writing the FLEX_TWI_CR.PECEN bit to one enables automatic PEC handling in the current transfer. Transfers with and without PEC can freely be intermixed in the same system, since some slaves may not support PEC. The PEC LFSR is always updated on every bit transmitted or received, so that PEC handling on combined transfers will be correct.

In Master Transmitter mode, the master calculates a PEC value and transmits it to the slave after all data bytes have been transmitted. Upon reception of this PEC byte, the slave will compare it to the PEC value it has computed itself. If the values match, the data was received correctly, and the slave will return an ACK to the master. If the PEC values differ, data was corrupted, and the slave will return a NACK value. Some slaves may not be able to check the received PEC in time to return a NACK if an error occurred. In this case, the slave should always return an ACK after the PEC byte, and some other mechanism must be implemented to verify that the transmission was received correctly.

47.10.30 USART Manchester Configuration Register

Name: FLEX_US_MAN

Address: 0xF8034250 (0), 0xF8038250 (1), 0xFC010250 (2), 0xFC014250 (3), 0xFC018250 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
RXIDLEV	DRIFT	ONE	RX_MPOL	–	–	RX_PP	

23	22	21	20	19	18	17	16
–	–	–	–	RX_PL			

15	14	13	12	11	10	9	8
–	–	–	TX_MPOL	–	–	TX_PP	

7	6	5	4	3	2	1	0
–	–	–	–	TX_PL			

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

TX_PL: Transmitter Preamble Length

0: The transmitter preamble pattern generation is disabled

1–15: The preamble length is TX_PL × Bit Period

TX_PP: Transmitter Preamble Pattern

The following values assume that TX_MPOL field is not set:

Value	Name	Description
0	ALL_ONE	The preamble is composed of ‘1’s
1	ALL_ZERO	The preamble is composed of ‘0’s
2	ZERO_ONE	The preamble is composed of ‘01’s
3	ONE_ZERO	The preamble is composed of ‘10’s

TX_MPOL: Transmitter Manchester Polarity

0: Logic zero is coded as a zero-to-one transition, Logic one is coded as a one-to-zero transition.

1: Logic zero is coded as a one-to-zero transition, Logic one is coded as a zero-to-one transition.

RX_PL: Receiver Preamble Length

0: The receiver preamble pattern detection is disabled

1–15: The detected preamble length is RX_PL × Bit Period

RX_PP: Receiver Preamble Pattern detected

The following values assume that RX_MPOL field is not set:

Value	Name	Description
0	ALL_ONE	The preamble is composed of ‘1’s
1	ALL_ZERO	The preamble is composed of ‘0’s
2	ZERO_ONE	The preamble is composed of ‘01’s
3	ONE_ZERO	The preamble is composed of ‘10’s

RX_MPOL: Receiver Manchester Polarity

The OPTL field determines the length of the option code. The value written in OPTL must be consistent with the value written in the field WIDTH. For example, OPTL = 0 (1-bit option code) is not consistent with WIDTH = 6 (option code sent with QuadSPI protocol, thus the minimum length of the option code is 4 bits).

Value	Name	Description
0	OPTION_1BIT	The option code is 1 bit long.
1	OPTION_2BIT	The option code is 2 bits long.
2	OPTION_4BIT	The option code is 4 bits long.
3	OPTION_8BIT	The option code is 8 bits long.

ADDRL: Address Length

The ADDRL bit determines the length of the address.

0 (24_BIT): The address is 24 bits long.

1 (32_BIT): The address is 32 bits long.

TFRTYP: Data Transfer Type

Value	Name	Description
0	TRSFR_READ	Read transfer from the serial memory. Scrambling is not performed. Read at random location (fetch) in the serial Flash memory is not possible.
1	TRSFR_READ_MEMORY	Read data transfer from the serial memory. If enabled, scrambling is performed. Read at random location (fetch) in the serial Flash memory is possible.
2	TRSFR_WRITE	Write transfer into the serial memory. Scrambling is not performed.
3	TRSFR_WRITE_MEMORY	Write data transfer into the serial memory. If enabled, scrambling is performed.

CRM: Continuous Read Mode

0 (DISABLED): Continuous Read mode is disabled.

1 (ENABLED): Continuous Read mode is enabled.

NBDUM: Number Of Dummy Cycles

The NBDUM field defines the number of dummy cycles required by the serial Flash memory before data transfer.

52.6.30 ISC Gamma Correction Control Register

Name: ISC_GAM_CTRL

Address: 0xF0008094

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–			RENABLE	GENABLE	BENABLE	ENABLE

ENABLE: Gamma Correction Enable

0: Gamma correction is disabled.

1: Gamma correction is enabled.

BENABLE: Gamma Correction Enable for B Channel

0: 12 bits to 10 bits compression is performed skipping two bits.

1: Piecewise interpolation is used to perform 12 bits to 10 bits compression for the blue channel.

GENABLE: Gamma Correction Enable for G Channel

0: 12 bits to 10 bits compression is performed skipping two bits.

1: Piecewise interpolation is used to perform 12 bits to 10 bits compression for the green channel.

RENABLE: Gamma Correction Enable for R Channel

0: 12 bits to 10 bits compression is performed skipping two bits.

1: Piecewise interpolation is used to perform 12 bits to 10 bits compression for the red channel.

52.6.33 ISC Gamma Correction Red Entry Register

Name: ISC_GAM_RENTRYx[x=0..63]

Address: 0xF0008298

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	RCONSTANT	

23	22	21	20	19	18	17	16
RCONSTANT							

15	14	13	12	11	10	9	8
–	–	–	–	–	–	RSLOPE	

7	6	5	4	3	2	1	0
RSLOPE							

RSLOPE: Red Color Slope for Piecewise Interpolation (signed 10 bits 1:3:6)

RCONSTANT: Red Color Constant for Piecewise Interpolation (unsigned 10 bits 0:10:0)

52.6.48 ISC Rounding, Limiting and Packing Configuration Register

Name: ISC_RLP_CFG

Address: 0xF00083D0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ALPHA							

7	6	5	4	3	2	1	0
–	–	–	–	MODE			

MODE: Rounding, Limiting and Packing Mode

Value	Name	Description
0	DAT8	8-bit data
1	DAT9	9-bit data
2	DAT10	10-bit data
3	DAT11	11-bit data
4	DAT12	12-bit data
5	DATY8	8-bit luminance only
6	DATY10	10-bit luminance only
7	ARGB444	12-bit RGB+4-bit Alpha (MSB)
8	ARGB555	15-bit RGB+1-bit Alpha (MSB)
9	RGB565	16-bit RGB
10	ARGB32	24-bits RGB mode+8-bit Alpha
11	YYCC	YCbCr mode (full range, [0–255])
12	YYCC_LIMITED	YCbCr mode (limited range)

ALPHA: Alpha Value for Alpha-enabled RGB Mode

58.5.2.2 ICM Region Configuration Structure Member

Name: ICM_RCFG

Address: ICM_DSCR+0x004+RID*(0x10)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	ALGO			–	PROCDLY	SUIEN	ECIEN
7	6	5	4	3	2	1	0
WCIEN	BEIEN	DMIEN	RHIEN	–	EOM	WRAP	CDWBN

CDWBN: Compare Digest or Write Back Digest

0: The digest is written to the Hash area.

1: The digest value is compared to the digest stored in the Hash area.

WRAP: Wrap Command

0: The next region descriptor address loaded is the current region identifier descriptor address incremented by 0x10.

1: The next region descriptor address loaded is ICM_DSCR.

EOM: End Of Monitoring

0: The current descriptor does not terminate the monitoring.

1: The current descriptor terminates the Main List. WRAP value has no effect.

RHIEN: Region Hash Completed Interrupt Disable (Default Enabled)

0: The ICM_ISR.RHC[*i*] flag is set when the field NEXT = 0 in a descriptor of the main or second list.

1: The ICM_ISR.RHC[*i*] flag remains cleared even if the setting condition is met.

DMIEN: Digest Mismatch Interrupt Disable (Default Enabled)

0: The ICM_ISR.RBE[*i*] flag is set when the hash value just calculated from the processed region differs from expected hash value.

1: The ICM_ISR.RBE[*i*] flag remains cleared even if the setting condition is met.

BEIEN: Bus Error Interrupt Disable (Default Enabled)

0: The flag is set when an error is reported on the system bus by the bus matrix.

1: The flag remains cleared even if the setting condition is met.

WCIEN: Wrap Condition Interrupt Disable (Default Enabled)

0: The ICM_ISR.RWC[*i*] flag is set when the WRAP bit is set in a descriptor of the main list.

1: The ICM_ISR.RWC[*i*] flag remains cleared even if the setting condition is met.

ECIEN: End Bit Condition Interrupt (Default Enabled)

0: The ICM_ISR.REC[*i*] flag is set when the descriptor with the EOM bit set is processed.

1: The ICM_ISR.REC[*i*] flag remains cleared even if the setting condition is met.

SUIEN: Monitoring Status Updated Condition Interrupt (Default Enabled)

0: The ICM_ISR.RSU[*i*] flag is set when the corresponding descriptor is loaded from memory to ICM.

1: The ICM_ISR.RSU[*i*] flag remains cleared even if the setting condition is met.

64.3.1 I/O Lines Description

Table 64-1: I/O Lines Description

Name	Description	Type
CLK32KHZ	32 kHz system clock from crystal or RC oscillator (SLCK)	Input
ICLK	64 kHz RC Oscillator	Input
PIOBU[7:0]	Parallel IO backup controller, 8 pads	I/O
IRQ[1:0]	Interrupt signals going to secure AIC	Output
SWKUP	Wakeup signal going to system controller WKUP1 pin	Output
FNTRST	Force Cortex-A5 test port reset	Output

64.4 Product Dependencies

64.4.1 Interrupt Sources

The SECUMOD provides two interrupt lines, each connected to one of the internal sources of the Advanced Interrupt Controller. Using these interrupts requires the AIC to be programmed first. Note that it is not recommended to use the interrupt lines in Edge-sensitive mode.

The first interrupt line (SECURAM ID) is dedicated to backup memories access right violations signaling, or end of erase (automatic or software erase) signaling.

The second interrupt line (SECUMOD ID) is shared by all the protection mechanisms.

See the User Interface description (Section 64.6 “Security Module (SECUMOD) User Interface”) for more information about interrupt acknowledgement.

The SECURAM and the SECUMOD interrupt lines are connected to the Interrupt Controller. The Interrupt Controller must be programmed before configuring the SECURAM or the SECUMOD.

Table 64-2: Peripheral IDs

Instance	ID
SECUMOD	16
SECURAM	51

Table 66-14: Typical Power Consumption for Backup Mode

V_{DDBU} (V)	Conditions	Consumption (µA)				Unit
		T_A = 25°C	T_A = 70°C	T_A = 85°C	T_A = 105°C	
1.6	V_{DDBU} Only	4.2	12.1	19.3	36.8	µA
1.7		4.2	12.1	19.3	36.9	
1.8		4.3	12.1	19.4	36.9	
1.9		4.3	12.1	19.4	36.9	
2		4.3	12.1	19.4	37	
2.1		4.3	12.2	19.4	37	
2.2		4.3	12.2	19.5	37	
2.3		4.4	12.2	19.5	37	
2.4		4.4	12.2	19.5	37	
2.5		4.4	12.3	19.5	37.1	
2.6		4.4	12.3	19.6	37.1	
2.7		4.4	12.3	19.6	37.1	
2.8		4.4	12.3	19.6	37.2	
2.9		4.5	12.4	19.6	37.2	
3		4.5	12.4	19.7	37.3	
3.1		4.5	12.5	19.8	37.7	
3.2		4.6	12.8	20.3	38.3	
3.3		4.9	13.4	20.9	38.9	
3.4		5.5	14.1	21.6	39.7	
3.5		6.2	14.9	22.4	40.5	
3.6		7	15.7	23.3	41.4	

66.6 Clock Characteristics

66.6.1 Processor Clock Characteristics

Table 66-15: Processor Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPPCK})$	Processor Clock Frequency	VDDCORE[1.1V, 1.32V], T_A = [-40°C, +85°C]	250(1)	400	MHz
		VDDCORE[1.2V, 1.32V], T_A = [-40°C, +85°C]	250(1)	500	

Note 1: Limitation for DDR2 (125 MHz) usage only. There are no limitations to DDR3, DDR3L, LPDDR1, LPDDR2 and LPDDR3.

Table 72-5: SAMA5D2 Datasheet Rev. 11267C Revision History (Continued)

Issue Date	Changes
8-Jan-16	Section 29. “Real-time Clock (RTC)” Removed RTC Milliseconds Register (RTC_MSR) and all related information in Section 29.1 “Description”, Section 29.2 “Embedded Characteristics”, Section 29.5 “Functional Description” and Section 29.6 “Real-time Clock (RTC) User Interface”. Table 29-1 “Register Mapping”: modified RTC_CALR reset value Section 29.6.1 “RTC Control Register”: updated CALEVSEL field description Updated Section 29.6.22 “RTC TimeStamp Source Register”
	Section 29. “Clock Generator” Section 29.2 “Embedded Characteristics”: replaced "400 to 1000 MHz programmable PLL" with "600 to 1200 MHz programmable PLL" and replaced “HCLOCK” with “HCLOCK_LS/HS” and “PCLOCK” with “PCLOCK_LS/HS” Section 29.4 “Slow Clock”: removed “This allows the slow clock to be valid in a short time (about 100 µs)” Section 29.8 “Audio PLL”: updated all equations and added “in the 700 MHz range” after “The PLL core operates at 700 MHz (AUDIOCORECLOCK)” Updated Figure 29-3. Main Clock Block Diagram and Figure 29-4. Main Clock Source Selection
	Section 30. “Power Management Controller (PMC)” Updated Section 30.6 “Matrix Clock Controller” Updated Section 30-1 “General Clock Block Diagram” Section 30.19 “Programming Sequence”, sub-section “Selecting Master Clock and Processor Clock”: updated sequence following "If a new value for CSS field corresponds to PLL Clock" Section 30.22.11 “PMC Master Clock Register”: updated H32MXDIV field description
	Section 33. “Multi-port DDR-SDRAM Controller (MPDDRC)” Section 33-2 “Single Write Access, Row Closed, DDR-SDRAM Devices” to Section 33-8 “SINGLE Write Access Followed by a Read Access, DDR2-SDRAM Devices”: replaced “D[15:0]” with “DATA” Updated Section 33.7.9 “MPDDRC Low-power DDR2 Low-power DDR3 Low-power Register” Section 33.7.10 “MPDDRC Low-power DDR2 Low-power DDR3 and DDR3 Calibration and MR4 Register”: updated MR4_READ field description
	Section 34. “Static Memory Controller (SMC)” Removed NFCCMD field and modified Section 34.17.2.1 “Building NFC Address Command Example” and Section 34.17.2.2 “NFC Address Command” accordingly Table 34-20 “Register Mapping”: corrected offset values of PMECC Error Location 31 Register and of subsequent reserved range; removed reset value from HSMC_CTRL (register is write-only)
	Section 42. “DMA Controller (XDMAC)” Section 42.5.4.1 “Single Block With Single Microblock Transfer”: added text on memory-to-memory transfer Section 42.8 “XDMAC Software Requirements”: added bullet on memory-to-memory transfer Table 42-5 “Register Mapping”: corrected access of XDMAC_GTYPE, XDMAC_GWAC, XDMAC_CIM Section 42.9.6 “XDMAC Global Interrupt Mask Register”: corrected access to Read-only Section 42.9.28 “XDMAC Channel x [x = 0..15] Configuration Register”: corrected INITD and PERID field descriptions
	Section 36. “LCD Controller (LCDC)” Modified width of fields in Section 36.7.2 “LCD Controller Configuration Register 1” and Section 36.7.3 “LCD Controller Configuration Register 2”
	Section 40. “Audio Class D Amplifier (CLASSD)” Replaced ‘audio clock’ with ‘generic clock’ and ‘ACLK’ with ‘GCLK’ throughout the section