Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d23b-cu

13.4.3.1 CP15 Coprocessor

Coprocessor 15, or System Control Coprocessor CP15, is used to configure and control all the items in the list below:

- Cortex A5
- Caches (ICache, DCache and write buffer)
- MMU
- Security
- Other system options

To control these features, CP15 provides 16 additional registers. See Table 13-4.

Table 13-4: CP15 Registers

Register	Name	Read/Write
0	ID Code(1)	Read/Unpredictable
0	Cache type(1)	Read/Unpredictable
1	Control(1)	Read/Write
1	Security(1)	Read/Write
2	Translation Table Base	Read/Write
3	Domain Access Control	Read/Write
4	Reserved	None
5	Data fault Status(1)	Read/Write
5	Instruction fault status	Read/Write
6	Fault Address	Read/Write
7	Cache and MMU Operations(1)	Read/Write
8	TLB operations	Unpredictable/Write
9	Cache lockdown(1)	Read/Write
10	TLB lockdown	Read/Write
11	Reserved	None
12	Interrupts management	Read/Write
12	Monitor vectors	Read-only
13	FCSE PID(1)	Read/Write
13	Context ID(1)	Read/Write
14	Reserved	None
15	Test configuration	Read/Write

Note 1: This register provides access to more than one register. The register accessed depends on the value of the CRm field or Opcode_2 field.

14.5.18 L2CC Invalidate Way Register

Name: L2CC_IWR

Address: 0x00A0077C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
WAY7	WAY6	WAY5	WAY4	WAY3	WAY2	WAY1	WAY0

WAYx: Invalidate Way Number x

0: The corresponding way is totally invalidated.

1: Invalidates the way. This bit is read as ‘1’ as long as invalidation of the way is in progress.

21. Advanced Interrupt Controller (AIC)

21.1 Description

The Advanced Interrupt Controller (AIC) is an 8-level priority, individually maskable, vectored interrupt controller providing handling of up to one hundred and twenty-eight interrupt sources. It is designed to substantially reduce the software and real-time overhead in handling internal and external interrupts.

The AIC drives the nFIQ (fast interrupt request) and the nIRQ (standard interrupt request) inputs of an ARM processor. Inputs of the AIC are either internal peripheral interrupts or external interrupts coming from the product's pins.

The 8-level Priority Controller allows the user to define the priority for each interrupt source, thus permitting higher priority interrupts to be serviced even if a lower priority interrupt is being processed.

Internal interrupt sources can be programmed to be level-sensitive or edge-triggered. External interrupt sources can be programmed to be rising-edge or falling-edge triggered or high-level or low-level sensitive.

21.2 Embedded Characteristics

- Controls the Interrupt Lines (nIRQ and nFIQ) of an ARM Processor
- 128 Individually Maskable and Vectored Interrupt Sources
  - Source 0 is reserved for the fast interrupt input (FIQ)
  - Source 74 is reserved for system peripheral interrupts
  - Sources 2 to 73 and Sources 75 to 127 control up to 125 embedded peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable rising/falling edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt of the processor
  - Handles priority of the interrupt sources 1 to 127
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register for all interrupt sources
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect models are enabled
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt
- Register Write Protection
- AIC0 is Non-Secure AIC, AIC1 is Secure AIC
- AIC0 manages nIRQ line, AIC1 manages nFIQ line

33. Power Management Controller (PMC)

33.1 Description

The Power Management Controller (PMC) optimizes power consumption by controlling all system and user peripheral clocks. The PMC enables/disables the clock inputs to many of the peripherals and the Core.

33.2 Embedded Characteristics

The Power Management Controller provides the following clocks:

- Master Clock (MCK)—programmable from a few hundred Hz to the maximum operating frequency of the device. It is available to the modules running permanently.
- Processor Clock (PCK)—must be switched off when processor is entering Idle mode
- HS USB Device Clock (UDPCK)
- H64MX Matrix Clock (MCK) and H32MX Matrix Clock (MCK or MCK/2)
- Peripheral Clocks—provided to the embedded peripherals and independently controllable
- Programmable Clock outputs can be selected from the clocks provided by the clock generator and driven on the PCKx pins.
- Generic Clock (GCLK) for peripherals that can accept a second clock source
- Asynchronous partial wakeup (SleepWalking) for FLEXCOMx, SPIx, TWIx, UARTx and ADC

Figure 36-2: Single Write Access, Row Closed, DDR-SDRAM Devices

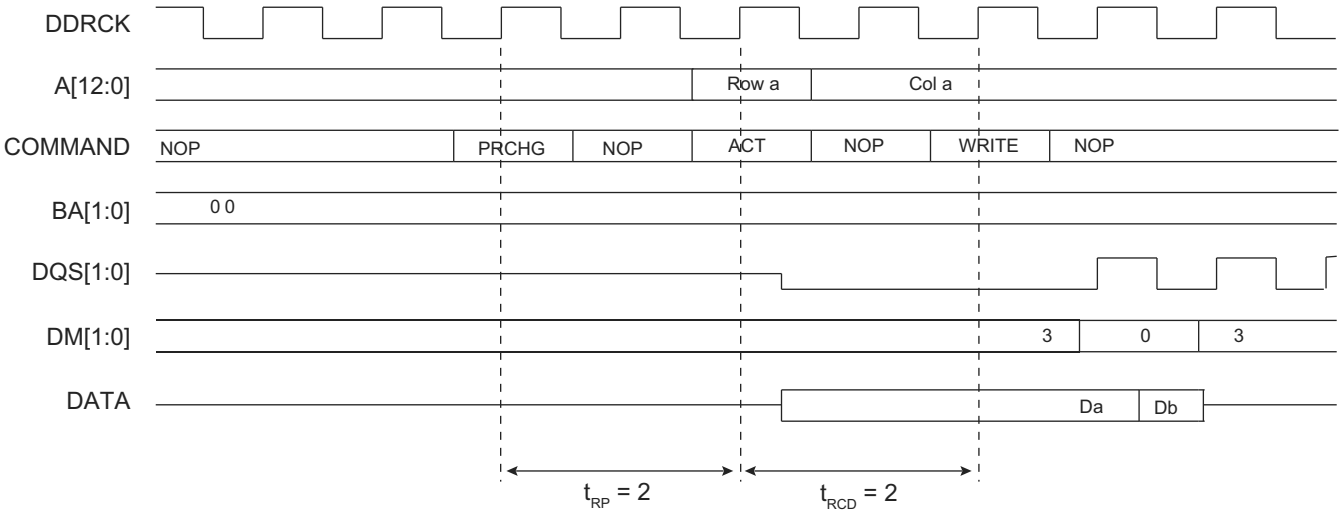
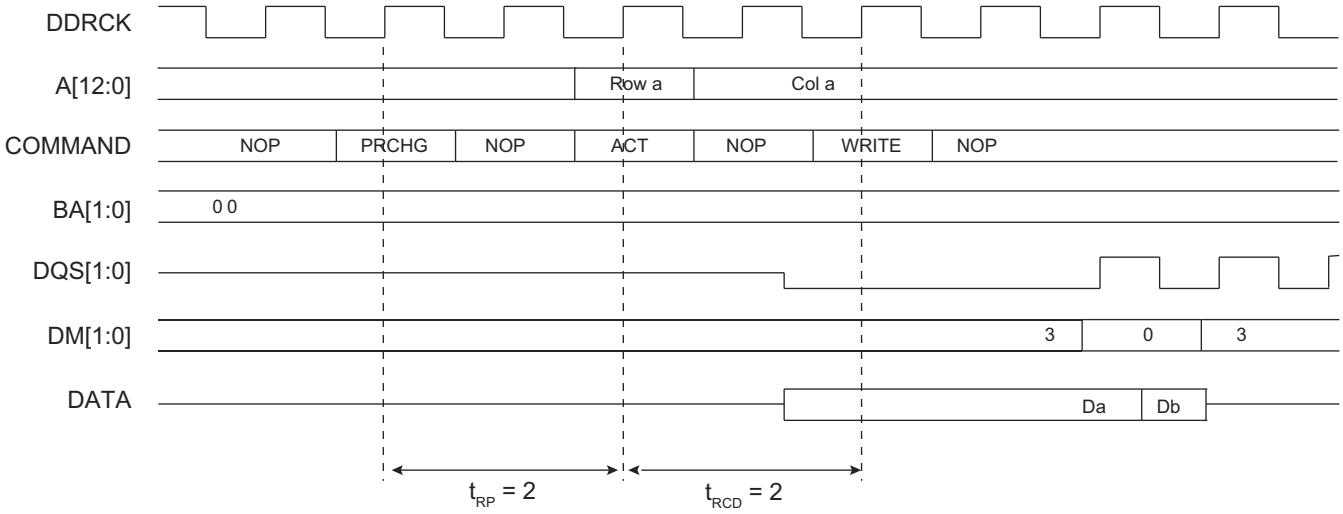


Figure 36-3: Single Write Access, Row Closed, DDR2-SDRAM Devices



39.7.134 High-End Overlay Configuration Register 39

Name: LCDC_HEOCFG39

Address: 0xF0000428

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
YPHI6COEFF2							

15	14	13	12	11	10	9	8
YPHI6COEFF1							

7	6	5	4	3	2	1	0
YPHI6COEFF0							

YPHI6COEFF0: Vertical Coefficient for phase 6 tap 0

Coefficient format is 1 sign bit and 7 fractional bits.

YPHI6COEFF1: Vertical Coefficient for phase 6 tap 1

Coefficient format is 1 magnitude bit and 7 fractional bits.

YPHI6COEFF2: Vertical Coefficient for phase 6 tap 2

Coefficient format is 1 sign bit and 7 fractional bits.

40.8.29 GMAC Specific Address 4 Top Register

Name: GMAC_SAT4

Address: 0xF80080A4

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

ADDR: Specific Address 4

The most significant bits of the destination address, that is, bits 47:32.

STALL_SNT: Stall Sent (cleared upon USB reset)

– (for Control, Bulk and Interrupt endpoints)

This bit is set by hardware after a STALL handshake has been sent as requested by the UDPHS_EPTSTAx register FRCESTALL bit.

This bit is reset by UDPHS_EPTRST register EPT_x (reset endpoint) and by UDPHS_EPTCTLDISx (disable endpoint).

NAK_IN: NAK IN (cleared upon USB reset)

This bit is set by hardware when a NAK handshake has been sent in response to an IN request from the Host.

This bit is cleared by software.

NAK_OUT: NAK OUT (cleared upon USB reset)

This bit is set by hardware when a NAK handshake has been sent in response to an OUT or PING request from the Host.

This bit is reset by UDPHS_EPTRST register EPT_x (reset endpoint) and by EPT_CTL_DISx (disable endpoint).

CURBK_CTLDIR: Current Bank/Control Direction (cleared upon USB reset)

– **Current Bank** (not relevant for Control endpoint):

These bits are set by hardware to indicate the number of the current bank.

Value	Name	Description
0	BANK0	Bank 0 (or single bank)
1	BANK1	Bank 1
2	BANK2	Bank 2

Note: The current bank is updated each time the user:
- Sets the TX Packet Ready bit to prepare the next IN transfer and to switch to the next bank.
- Clears the received OUT data bit to access the next bank.

This bit is reset by UDPHS_EPTRST register EPT_x (reset endpoint) and by UDPHS_EPTCTLDISx (disable endpoint).

– **Control Direction** (for Control endpoint only):

0: A Control Write is requested by the Host.

1: A Control Read is requested by the Host.

Note 1: This bit corresponds with the 7th bit of the bmRequestType (Byte 0 of the Setup Data).

2: This bit is updated after receiving new setup data.

BUSY_BANK_STA: Busy Bank Number (cleared upon USB reset)

These bits are set by hardware to indicate the number of busy banks.

IN endpoint: It indicates the number of busy banks filled by the user, ready for IN transfer.

OUT endpoint: It indicates the number of busy banks filled by OUT transaction from the Host.

Value	Name	Description
0	0BUSYBANK	All banks are free
1	1BUSYBANK	1 busy bank
2	2BUSYBANKS	2 busy banks
3	3BUSYBANKS	3 busy banks

43.7 Audio Class D Amplifier (CLASSD) User Interface

Table 43-5: Register Mapping

Offset	Register	Name	Access	Reset
0x00	Control Register	CLASSD_CR	Write-only	–
0x04	Mode Register	CLASSD_MR	Read/Write	0x00010022
0x08	Interpolator Mode Register	CLASSD_INTPMR	Read/Write	0x00304E4E
0x0C	Interpolator Status Register	CLASSD_INTSR	Read-only	0x00000000
0x10	Transmit Holding Register	CLASSD_THR	Read/Write	0x00000000
0x14	Interrupt Enable Register	CLASSD_IER	Write-only	–
0x18	Interrupt Disable Register	CLASSD_IDR	Write-only	–
0x1C	Interrupt Mask Register	CLASSD_IMR	Read/Write	0x00000000
0x20	Interrupt Status Register	CLASSD_ISR	Read-only	0x00000000
0x24–0xE0	Reserved	–	–	–
0xE4	Write Protection Mode Register	CLASSD_WPMR	Read/Write	0x00000000
0xE8–0xFC	Reserved	–	–	–

Figure 47-102: TWI Read Operation with Single Data Byte without Internal Address

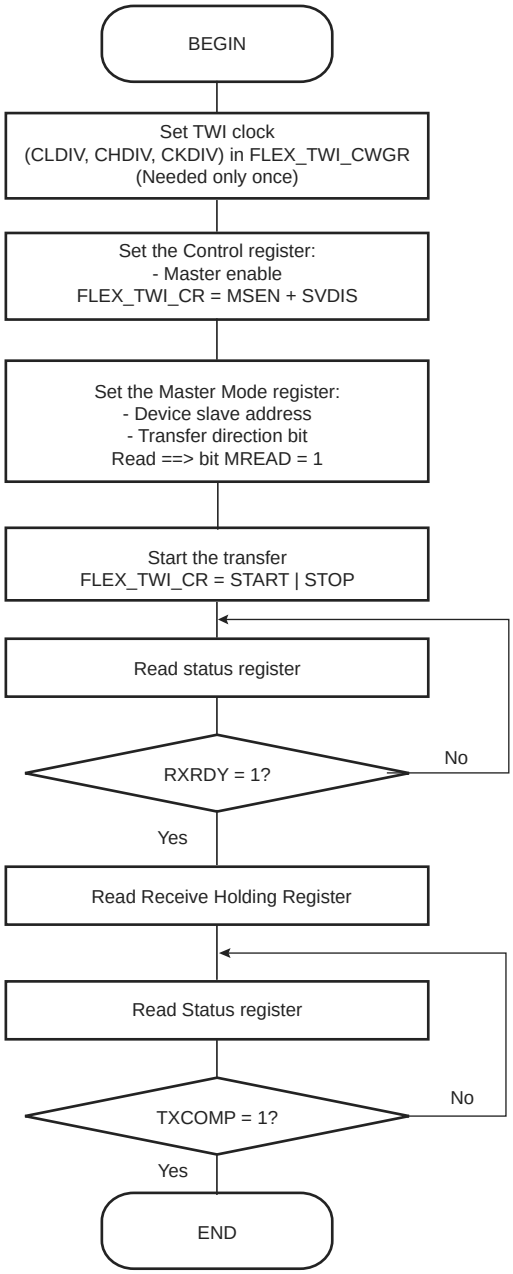


Table 47-18: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x630	TWI Receive Holding Register	FLEX_TWI_RHR	Read-only	0x00000000
0x634	TWI Transmit Holding Register	FLEX_TWI_THR	Write-only	–
0x638	TWI SMBus Timing Register	FLEX_TWI_SMBTR	Read/Write	0x00000000
0x63C	Reserved	–	–	–
0x640	TWI Alternative Command Register	FLEX_TWI_ACR	Read/Write	0x0
0x644	TWI Filter Register	FLEX_TWI_FILTR	Read/Write	0x00000000
0x648	Reserved	–	–	–
0x64C	TWI SleepWalking Matching Register	FLEX_TWI_SWMR	Read/Write	0x00000000
0x650	TWI FIFO Mode Register	FLEX_TWI_FMR	Read/Write	0x0
0x654	TWI FIFO Level Register	FLEX_TWI_FLR	Read-only	0x0
0x658–0x65C	Reserved	–	–	–
0x660	TWI FIFO Status Register	FLEX_TWI_FSR	Read-only	0x0
0x664	TWI FIFO Interrupt Enable Register	FLEX_TWI_FIER	Write-only	–
0x668	TWI FIFO Interrupt Disable Register	FLEX_TWI_FIDR	Write-only	–
0x66C	TWI FIFO Interrupt Mask Register	FLEX_TWI_FIMR	Read-only	0x0
0x670–0x6CC	Reserved	–	–	–
0x6D0	Reserved	–	–	–
0x6D4–0x6E0	Reserved	–	–	–
0x6E4	TWI Write Protection Mode Register	FLEX_TWI_WPMR	Read/Write	0x00000000
0x6E8	TWI Write Protection Status Register	FLEX_TWI_WPSR	Read-only	0x00000000
0x6EC–0x6FC	Reserved	–	–	–
0x700–0x7FC	Reserved	–	–	–

Note 1: Write is possible only in LIN master node configuration.

47.10.78 TWI SleepWalking Matching Register

Name: FLEX_TWI_SWMR

Address: 0xF803464C (0), 0xF803864C (1), 0xFC01064C (2), 0xFC01464C (3), 0xFC01864C (4)

Access: Read/Write

31	30	29	28	27	26	25	24
DATAM							

23	22	21	20	19	18	17	16
–	SADR3						

15	14	13	12	11	10	9	8
–	SADR2						

7	6	5	4	3	2	1	0
–	SADR1						

SADR1: Slave Address 1

Slave address 1. The TWI module will match on this additional address if SADR1EN bit is enabled.

SADR2: Slave Address 2

Slave address 2. The TWI module will match on this additional address if SADR2EN bit is enabled.

SADR3: Slave Address 3

Slave address 3. The TWI module will match on this additional address if SADR3EN bit is enabled.

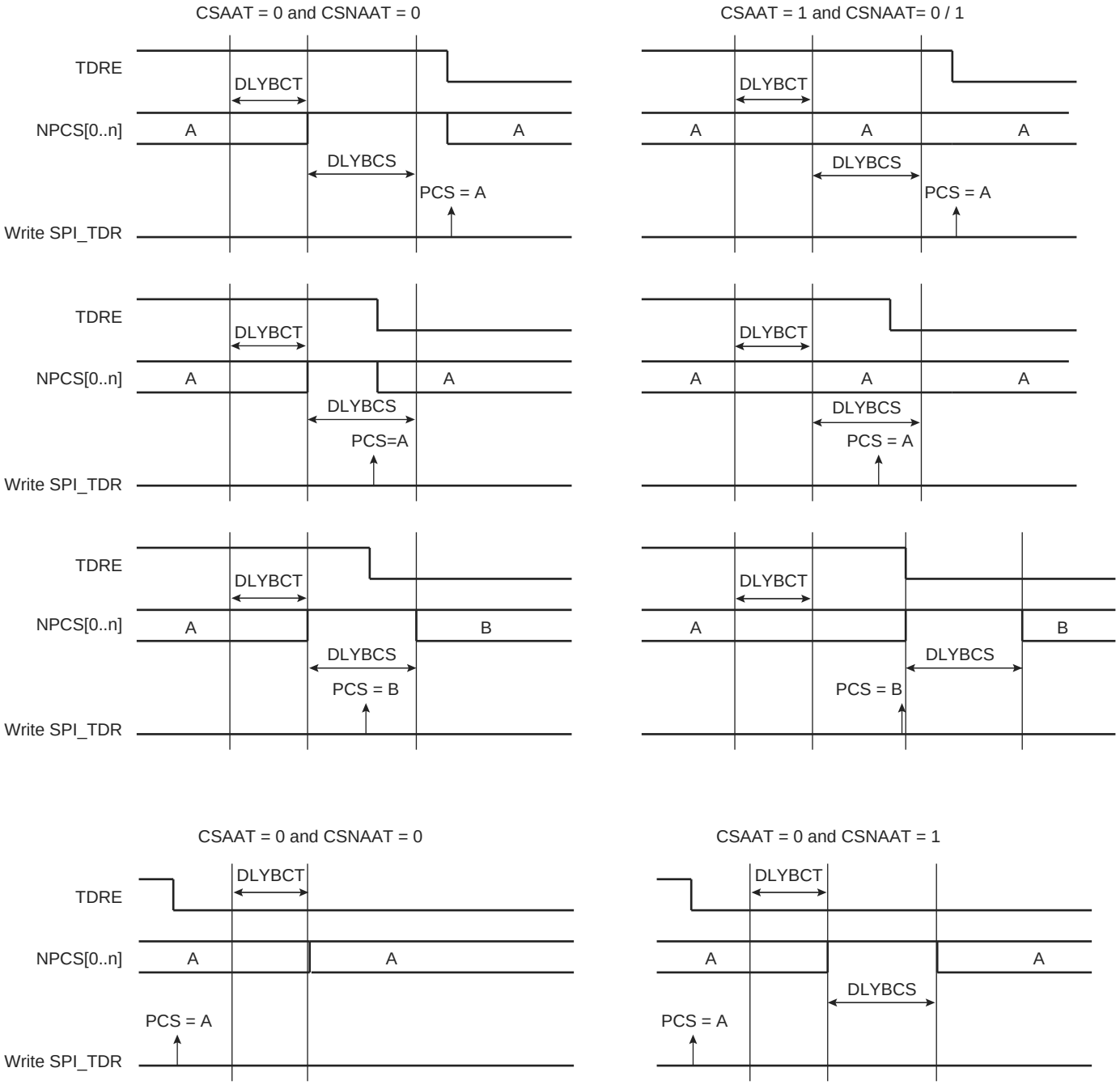
DATAM: Data Match

The TWI module will extend the SleepWalking matching process to the first received data comparing it with DATAM if DATAMEN bit is enabled.

When the CSAAT bit is configured to 0, the NPCS does not rise in all cases between two transfers on the same peripheral. During a transfer on a chip select, the TDRE flag rises as soon as the content of SPI_TDR is transferred into the internal shift register. When this flag is detected, SPI_TDR can be reloaded. If this reload occurs before the end of the current transfer and if the next transfer is performed on the same chip select as the current transfer, the chip select is not deasserted between the two transfers. This can lead to difficulties to interface with some serial peripherals requiring the chip select to be deasserted after each transfer. To facilitate interfacing with such devices, SPI_CSR can be programmed with the Chip Select Not Active After Transfer (CSNAAT) bit at 1. This allows the chip select lines to be deasserted systematically during a time “DLYBCS” (the value of the CSNAAT bit is processed only if the CSAAT bit is configured to 0 for the same chip select).

Figure 49-11 shows different peripheral deselection cases and the effect of the CSAAT and CSNAAT bits.

Figure 49-11: Peripheral Deselection



49.8 Serial Peripheral Interface (SPI) User Interface

In the “Offset” column of Table 49-5, ‘CS_number’ denotes the chip select number.

Table 49-5: Register Mapping

Offset	Register	Name	Access	Reset
0x00	Control Register	SPI_CR	Write-only	–
0x04	Mode Register	SPI_MR	Read/Write	0x0
0x08	Receive Data Register	SPI_RDR	Read-only	0x0
0x0C	Transmit Data Register	SPI_TDR	Write-only	–
0x10	Status Register	SPI_SR	Read-only	0x0
0x14	Interrupt Enable Register	SPI_IER	Write-only	–
0x18	Interrupt Disable Register	SPI_IDR	Write-only	–
0x1C	Interrupt Mask Register	SPI_IMR	Read-only	0x0
0x20–0x2C	Reserved	–	–	–
0x30 + (CS_number * 0x04)	Chip Select Register	SPI_CSR	Read/Write	0x0
0x40	FIFO Mode Register	SPI_FMR	Read/Write	0x0
0x44	FIFO Level Register	SPI_FLR	Read-only	0x0
0x48	Comparison Register	SPI_CMPR	Read-only	0x0
0x4C–0xE0	Reserved	–	–	–
0xE4	Write Protection Mode Register	SPI_WPMR	Read/Write	0x0
0xE8	Write Protection Status Register	SPI_WPSR	Read-only	0x0
0xEC–0xF8	Reserved	–	–	–
0xFC	Reserved	–	–	–

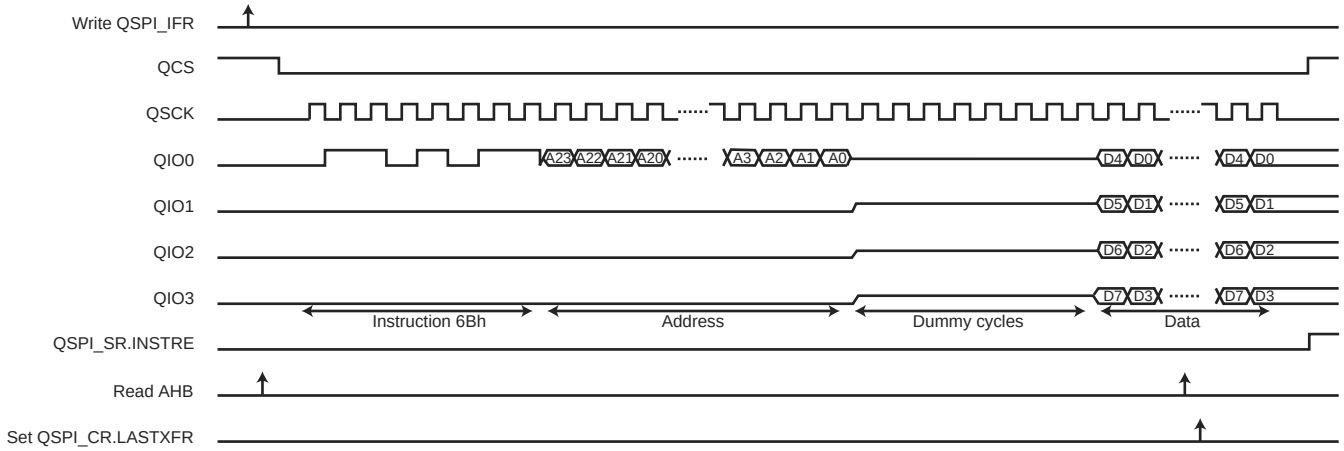
Example 6:

Instruction in Single-bit SPI, with address in Single-bit SPI, without option, with data read in Quad SPI, with eight dummy cycles.

Command: QUAD_OUTPUT READ ARRAY (6Bh)

- Write 0x0000_006B in QSPI_ICR.
- Write 0x0008_10B2 in QSPI_IFR.
- Read QSPI_IR (dummy read) to synchronize system bus accesses.
- Read data in the QSPI system bus memory space (0x9000_00000-0x9800_00000/0XD000_0000--0XD800_0000).
  The address of the first system bus read access is sent in the instruction frame.
  The address of the next system bus read accesses is not used.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 50-16: Instruction Transmission Waveform 6



51.13.2 SDMMC Block Size Register

Name: SDMMC_BSR

Access: Read/Write

15	14	13	12	11	10	9	8
–	BOUNDARY			–	–	BLKSIZE	
7	6	5	4	3	2	1	0
BLKSIZE							

BLKSIZE: Transfer Block Size

This field specifies the block size of data transfers for CMD14, CMD17, CMD18, CMD19, CMD24, CMD25, CMD53 and other data transfer commands such as CMD6, CMD8, ACMD13 and ACMD51. Values ranging from 1 to 512 can be set. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations are ignored.

BOUNDARY: SDMA Buffer Boundary

This field specifies the size of the contiguous buffer in the system memory. The SDMA transfer waits at every boundary specified by this field and the SDMMC generates the DMA Interrupt to instruct the software to update SDMMC_SSAR. If this field is set to 0 (buffer size = 4 Kbytes), the lowest 12 bits of SDMMC_SSAR.ADDRESS point to data in the contiguous buffer, and the upper 20 bits point to the location of the buffer in the system memory. This function is active when the DMAEN bit is set in SDMMC_TMR.

Value	Name	Description
0	4K	4-Kbyte boundary
1	8K	8-Kbyte boundary
2	16K	16-Kbyte boundary
3	32K	32-Kbyte boundary
4	64K	64-Kbyte boundary
5	128K	128-Kbyte boundary
6	256k	256-Kbyte boundary
7	512K	512-Kbyte boundary

51.13.11 SDMMC Host Control 1 Register (e.MMC)

Name: SDMMC_HC1R (e.MMC)

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	EXTDW	DMASEL		HSEN	DW	–

DW: Data Width

This bit selects the data width of the SDMMC. It must be set to match the data width of the card.

0 (1_BIT): 1-bit mode.

1 (4_BIT): 4-bit mode.

Note: If the Extended Data Transfer Width is 1, this bit has no effect and the data width is 8-bit mode.

HSEN: High Speed Enable

Before setting this bit, the user must check High Speed Support (HSSUP) in SDMMC_CA0R.

If this bit is set to 0 (default), the SDMMC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz). If this bit is set to 1, the SDMMC outputs the CMD line and the DAT lines at the rising edge of the SD clock (up to 50 MHz).

If Preset Value Enable (PVALEN) in SDMMC_HC2R is set to 1, the user needs to reset the SD Clock Enable (SDCLKEN) before changing this bit to avoid generating clock glitches. After setting this bit to 1, the user sets SDCLEN to 1 again.

0: Normal Speed mode.

1: High Speed mode.

Note 1: This bit is effective only if SDMMC_MC1R.DDR is set to 0.

2: The clock divider (DIV) in SDMMC_CCR must be set to a value different from 0 when HSEN is 1.

DMASEL: DMA Select

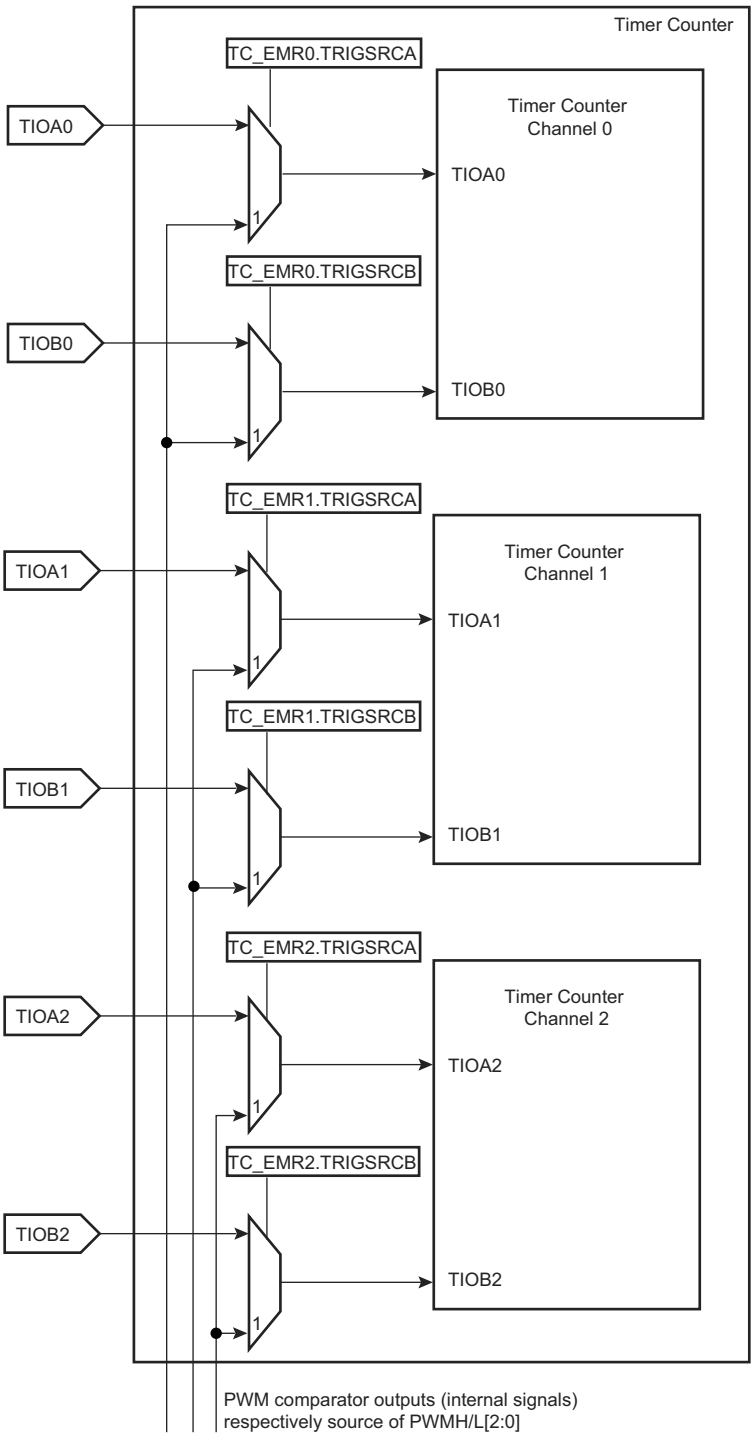
One of the supported DAM modes can be selected. The user must check support of DMA modes by referring the SDMMC_CA0R. Use of selected DMA is determined by DMA Enable (DMAEN) in SDMMC_TMR.

Value	Name	Description
0	SDMA	SDMA is selected
1	–	Reserved
2	ADMA32	32-bit Address ADMA2 is selected
3	–	Reserved

EXTDW: Extended Data Width

This bit controls the 8-bit Bus Width mode for embedded devices. Support of this function is indicated in 8-bit Support for Embedded Device in SDMMC_CA0R. If a device supports the 8-bit mode, this may be set to 1. If this bit is 0, the bus width is controlled by Data Width (DW).

Figure 54-16: Synchronization with PWM



65.7.2 ADC Mode Register

Name: ADC_MR

Address: 0xFC030004

Access: Read/Write

31	30	29	28	27	26	25	24
USEQ	MAXSPEED	TRANSFER		TRACKTIM			
23	22	21	20	19	18	17	16
ANACH	–	–	–	STARTUP			
15	14	13	12	11	10	9	8
PRESCAL							
7	6	5	4	3	2	1	0
–	FWUP	SLEEP	–	TRGSEL			–

This register can only be written if the WPEN bit is cleared in the ADC Write Protection Mode Register.

TRGSEL: Trigger Selection

Value	Name	Description
0	ADC_TRIG0	ADTRG
1	ADC_TRIG1	TIOA0
2	ADC_TRIG2	TIOA1
3	ADC_TRIG3	TIOA2
4	ADC_TRIG4	PWM event line 0
5	ADC_TRIG5	PWM event line 1
6	ADC_TRIG6	TIOA3
7	ADC_TRIG7	RTCOUT0

Note: The trigger selection can be performed only if TRGMOD = 1, 2 or 3 in ADC Trigger Register.

SLEEP: Sleep Mode

Value	Name	Description
0	NORMAL	Normal Mode: The ADC core and reference voltage circuitry are kept ON between conversions.
1	SLEEP	Sleep Mode: The wakeup time can be modified by programming the FWUP bit.

FWUP: Fast Wakeup

Value	Name	Description
0	OFF	If SLEEP is 1, then both ADC core and reference voltage circuitry are OFF between conversions
1	ON	If SLEEP is 1, then Fast Wakeup Sleep mode: The voltage reference is ON between conversions and ADC core is OFF

PRESCAL: Prescaler Rate Selection

$PRESCAL = (f_{peripheral\ clock} / (2 \times f_{ADCCLK})) - 1.$

71.3.20 MPDDRC t_{FAW}

Issue: t_{FAW} timing violation

DDR2/LPDDR2 memory devices with 8 banks have an additional requirement for t_{FAW}: no more than four Activate commands must be issued in any given t_{FAW} period.

Workaround: Increase the value of t_{RRD} to 3 to avoid the issue.

71.3.21 Audio PLL

Issue: Audio PLL output frequency range

The frequency range of the AUDIOCORECLK signal (AUDIOPLL output) provided in Table 66-26 “Audio PLL Characteristics” (f_{CORE} parameter) does not comply with the applicable specification.

Workaround: The AUDIOCORECLK signal can be operated from 720 MHz to 790 MHz if the following restricted operating conditions are met:

- Junction temperature (T_j) range: 0°C to +40°C
- VDDCORE/VDDPLL supply range: 1.20V to 1.32V
- Bits <29:28> in register PMC_AUDIO_PLL0 are set to $(01)_2$

71.3.22 SSC TD Output

Issue: Unexpected delay on TD output

When SSC is configured with the following conditions:

- RCMR.START = Start on falling edge/Start on Rising edge/Start on any edge,
- RFMR.FSOS = None (input),
- TCMR.START = Receive Start,

an unexpected delay of 2 or 3 system clock cycles is added to the TD output.

Workaround: None

71.3.23 I2SC First Sent Data

Issue: I2SC first sent data corrupted

Right after I2SC reset, the first data sent by I2SC controller on the I2SDO line is corrupted. The following data are not affected.

Workaround: None

71.3.24 Quad I/O Serial Peripheral Interface (QSPI)

Issue: QSPI hangs with long DLYCS

QSPI hangs if a command is written to any QSPI register during the DLYCS delay. There is no status bit to flag the end of the delay.

Workaround: The field DLYCS defines a minimum period for which Chip Select is de-asserted, required by some memories. This delay is generally < 60 ns and comprises internal execution time, arbitration and latencies. Thus, DLYCS must be configured to be slightly higher than the value specified for the slave device. The software must wait for this same period of time plus an additional delay before a command can be written to the QSPI.