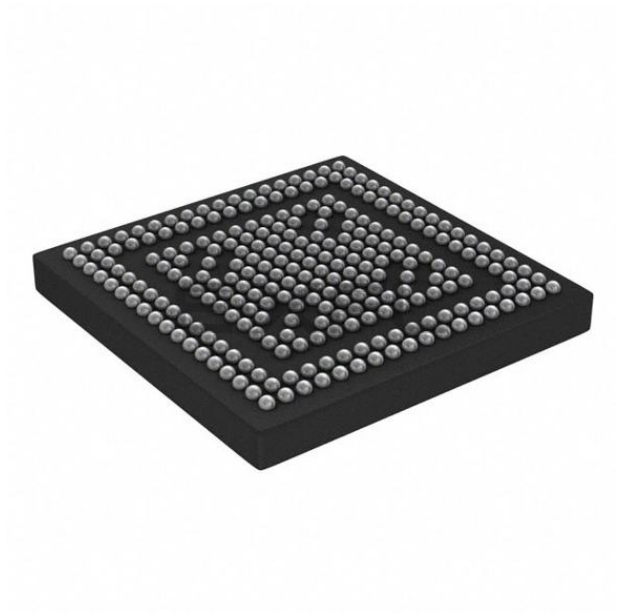

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Table 4-1: Signal Description List (Continued)

Signal Name	Function	Type	Comments	Active Level
Serial Peripheral Interface - SPIx [1..0]				
SPIx_MISO	Master In Slave Out	I/O	–	–
SPIx_MOSI	Master Out Slave In	I/O	–	–
SPIx_SPCK	SPI Serial Clock	I/O	–	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	–	Low
SPIx_NPCS[3..1]	SPI Peripheral Chip Select	Output	–	Low
Two-wire Interface - TWIx [1..0]				
TWDx	Two-wire Serial Data	I/O	–	–
TWCKx	Two-wire Serial Clock	I/O	–	–
Pulse Width Modulation Controller - PWM				
PWMH0–3	PWM Waveform Output High	Output	–	–
PWML0–3	PWM Waveform Output Low	Output	–	–
PWMFI0–1	PWM Fault Inputs	Input	–	–
PWMEXTRG1–2	PWM External Trigger	Input	–	–
USB Host High Speed Port - UHPHS				
HHSDPA	USB Host Port A High Speed Data +	Analog	–	–
HHSDMA	USB Host Port A High Speed Data -	Analog	–	–
HHSDPB	USB Host Port B High Speed Data +	Analog	–	–
HHSDMB	USB Host Port B High Speed Data -	Analog	–	–
USB Device High Speed Port - UDPHS				
DHSDP	USB Device High Speed Data +	Analog	–	–
DHSDM	USB Device High Speed Data -	Analog	–	–
USB High-Speed Inter-Chip Port - HSIC				
HHSTROBE	USB High-Speed Inter-Chip Strobe	I/O	–	–
HHDATA	USB High-Speed Inter-Chip Data	I/O	–	–
Ethernet 10/100 - GMAC				
GREFCK	Reference Clock	Input	–	–
GTXCK	Transmit Clock	Input	–	–
GRXCK	Receive Clock	Input	–	–
GTXEN	Transmit Enable	Output	–	–
GTX0–GTX3	Transmit Data	Output	–	–
GTXER	Transmit Coding Error	Output	–	–
GRXDV	Receive Data Valid	Input	–	–
GRX0–GRX3	Receive Data	Input	–	–
GRXER	Receive Error	Input	–	–
GCRS	Carrier Sense	Input	–	–

21.9.1 AIC Source Select Register

Name: AIC_SSR

Address: 0xFC020000 (AIC), 0xF803C000 (SAIC)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	INTSEL						

INTSEL: Interrupt Line Selection

0–127 = Selects the interrupt line to handle.

See Section 21.8.1.1 “Interrupt Source Mode”.

37.17.4 NFC SRAM

37.17.4.1 NFC SRAM Mapping

If the NFC is used to read and write data from and to the NAND Flash, the configuration depends on the page size (PAGESIZE field in HSMC_CFG register). See Table 37-9 to Table 37-13 for detailed mapping.

The NFC can handle the NAND Flash with a page size of 8 Kbytes or lower (such as 2 Kbytes, for example). In case of a 4 Kbyte or lower page size, the NFC SRAM can be split into two banks. The BANK bit in the HSMC_BANK register is used to select where NAND flash data are written or read. For an 8 Kbyte page size this field is not relevant.

Note that a “Ping-Pong” mode (write or read to a bank while the NFC writes or reads to another bank) is accessible with the NFC (using two different banks).

If the NFC is not used, the NFC SRAM can be used for a general purpose by the application.

Table 37-9: NFC SRAM Bank Mapping for 512 bytes

Offset	Use	Access
0x00000000–0x000001FF	Main Area Bank 0	Read/Write
0x00000200–0x000003FF	Spare Area Bank 0	Read/Write
0x00001200–0x000013FF	Main Area Bank 1	Read/Write
0x00001400–0x000015FF	Spare Area Bank 1	Read/Write

Table 37-10: NFC SRAM Bank Mapping for 1 Kbyte

Offset	Use	Access
0x00000000–0x000003FF	Main Area Bank 0	Read/Write
0x00000400–0x000005FF	Spare Area Bank 0	Read/Write
0x00001200–0x000015FF	Main Area Bank 1	Read/Write
0x00001600–0x000017FF	Spare Area Bank 1	Read/Write

Table 37-11: NFC SRAM Bank Mapping for 2 Kbytes

Offset	Use	Access
0x00000000–0x000007FF	Main Area Bank 0	Read/Write
0x00000800–0x000009FF	Spare Area Bank 0	Read/Write
0x00001200–0x000019FF	Main Area Bank 1	Read/Write
0x00001A00–0x00001BFF	Spare Area Bank 1	Read/Write

Table 37-12: NFC SRAM Bank Mapping for 4 Kbytes

Offset	Use	Access
0x00000000–0x00000FFF	Main Area Bank 0	Read/Write
0x00001000–0x000011FF	Spare Area Bank 0	Read/Write
0x00001200–0x000021FF	Main Area Bank 1	Read/Write
0x00002200–0x000023FF	Spare Area Bank 1	Read/Write

Table 37-13: NFC SRAM Bank Mapping for 8 Kbytes, only one bank is available

Offset	Use	Access
0x00000000–0x00001FFF	Main Area Bank 0	Read/Write
0x00002000–0x000023FF	Spare Area Bank 0	Read/Write

38.9.25 XDMAC Channel x [x = 0..15] Next Descriptor Control Register

Name: XDMAC_CNDCx [x = 0..15]

Address: 0xF000406C (1)[0], 0xF00040AC (1)[1], 0xF00040EC (1)[2], 0xF000412C (1)[3], 0xF000416C (1)[4], 0xF00041AC (1)[5], 0xF00041EC (1)[6], 0xF000422C (1)[7], 0xF000426C (1)[8], 0xF00042AC (1)[9], 0xF00042EC (1)[10], 0xF000432C (1)[11], 0xF000436C (1)[12], 0xF00043AC (1)[13], 0xF00043EC (1)[14], 0xF000442C (1)[15], 0xF001006C (0)[0], 0xF00100AC (0)[1], 0xF00100EC (0)[2], 0xF001012C (0)[3], 0xF001016C (0)[4], 0xF00101AC (0)[5], 0xF00101EC (0)[6], 0xF001022C (0)[7], 0xF001026C (0)[8], 0xF00102AC (0)[9], 0xF00102EC (0)[10], 0xF001032C (0)[11], 0xF001036C (0)[12], 0xF00103AC (0)[13], 0xF00103EC (0)[14], 0xF001042C (0)[15]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	NDVIEW		NDDUP	NDSUP	NDE

NDE: Channel x Next Descriptor Enable

0 (DSCR_FETCH_DIS): Descriptor fetch is disabled.

1 (DSCR_FETCH_EN): Descriptor fetch is enabled.

NDSUP: Channel x Next Descriptor Source Update

0 (SRC_PARAMS_UNCHANGED): Source parameters remain unchanged.

1 (SRC_PARAMS_UPDATED): Source parameters are updated when the descriptor is retrieved.

NDDUP: Channel x Next Descriptor Destination Update

0 (DST_PARAMS_UNCHANGED): Destination parameters remain unchanged.

1 (DST_PARAMS_UPDATED): Destination parameters are updated when the descriptor is retrieved.

NDVIEW: Channel x Next Descriptor View

Value	Name	Description
0	NDV0	Next Descriptor View 0
1	NDV1	Next Descriptor View 1
2	NDV2	Next Descriptor View 2
3	NDV3	Next Descriptor View 3

38.9.28 XDMAC Channel x [x = 0..15] Configuration Register

Name: XDMAC_CCx[x = 0..15]

Address: 0xF0004078 (1)[0], 0xF00040B8 (1)[1], 0xF00040F8 (1)[2], 0xF0004138 (1)[3], 0xF0004178 (1)[4], 0xF00041B8 (1)[5], 0xF00041F8 (1)[6], 0xF0004238 (1)[7], 0xF0004278 (1)[8], 0xF00042B8 (1)[9], 0xF00042F8 (1)[10], 0xF0004338 (1)[11], 0xF0004378 (1)[12], 0xF00043B8 (1)[13], 0xF00043F8 (1)[14], 0xF0004438 (1)[15], 0xF0010078 (0)[0], 0xF00100B8 (0)[1], 0xF00100F8 (0)[2], 0xF0010138 (0)[3], 0xF0010178 (0)[4], 0xF00101B8 (0)[5], 0xF00101F8 (0)[6], 0xF0010238 (0)[7], 0xF0010278 (0)[8], 0xF00102B8 (0)[9], 0xF00102F8 (0)[10], 0xF0010338 (0)[11], 0xF0010378 (0)[12], 0xF00103B8 (0)[13], 0xF00103F8 (0)[14], 0xF0010438 (0)[15]

Access: Read/Write

31	30	29	28	27	26	25	24
–	PERID						

23	22	21	20	19	18	17	16
WRIP	RDIP	INITD	–	DAM		SAM	

15	14	13	12	11	10	9	8
–	DIF	SIF	DWIDTH		CSIZE		

7	6	5	4	3	2	1	0
MEMSET	SWREQ	PROT	DSYNC	–	MBSIZE		TYPE

TYPE: Channel x Transfer Type

0 (MEM_TRAN): Self-triggered mode (memory-to-memory transfer).

1 (PER_TRAN): Synchronized mode (peripheral-to-memory or memory-to-peripheral transfer).

MBSIZE: Channel x Memory Burst Size

Value	Name	Description
0	SINGLE	The memory burst size is set to one.
1	FOUR	The memory burst size is set to four.
2	EIGHT	The memory burst size is set to eight.
3	SIXTEEN	The memory burst size is set to sixteen.

DSYNC: Channel x Synchronization

0 (PER2MEM): Peripheral-to-memory transfer.

1 (MEM2PER): Memory-to-peripheral transfer.

PROT: Channel x Protection

0 (SEC): Channel is secured.

1 (UNSEC): Channel is unsecured.

SWREQ: Channel x Software Request Trigger

0 (HWR_CONNECTED): Hardware request line is connected to the peripheral request line.

1 (SWR_CONNECTED): Software request is connected to the peripheral request line.

MEMSET: Channel x Fill Block of Memory

0 (NORMAL_MODE): Memset is not activated.

1 (HW_MODE): Sets the block of memory pointed by DA field to the specified value. This operation is performed on 8-, 16- or 32-bit basis.

39.7.10 LCD Controller Status Register

Name: LCDC_LCDSR

Address: 0xF0000028

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	SIPSTS	PWMSTS	DISPSTS	LCDSTS	CLKSTS

CLKSTS: Clock Status

0: Pixel clock is disabled.

1: Pixel clock is running.

LCDSTS: LCD Controller Synchronization status

0: Timing engine is disabled.

1: Timing engine is running.

DISPSTS: LCD Controller DISP Signal Status

0: DISP is disabled.

1: DISP signal is activated.

PWMSTS: LCD Controller PWM Signal Status

0: PWM is disabled.

1: PWM signal is activated.

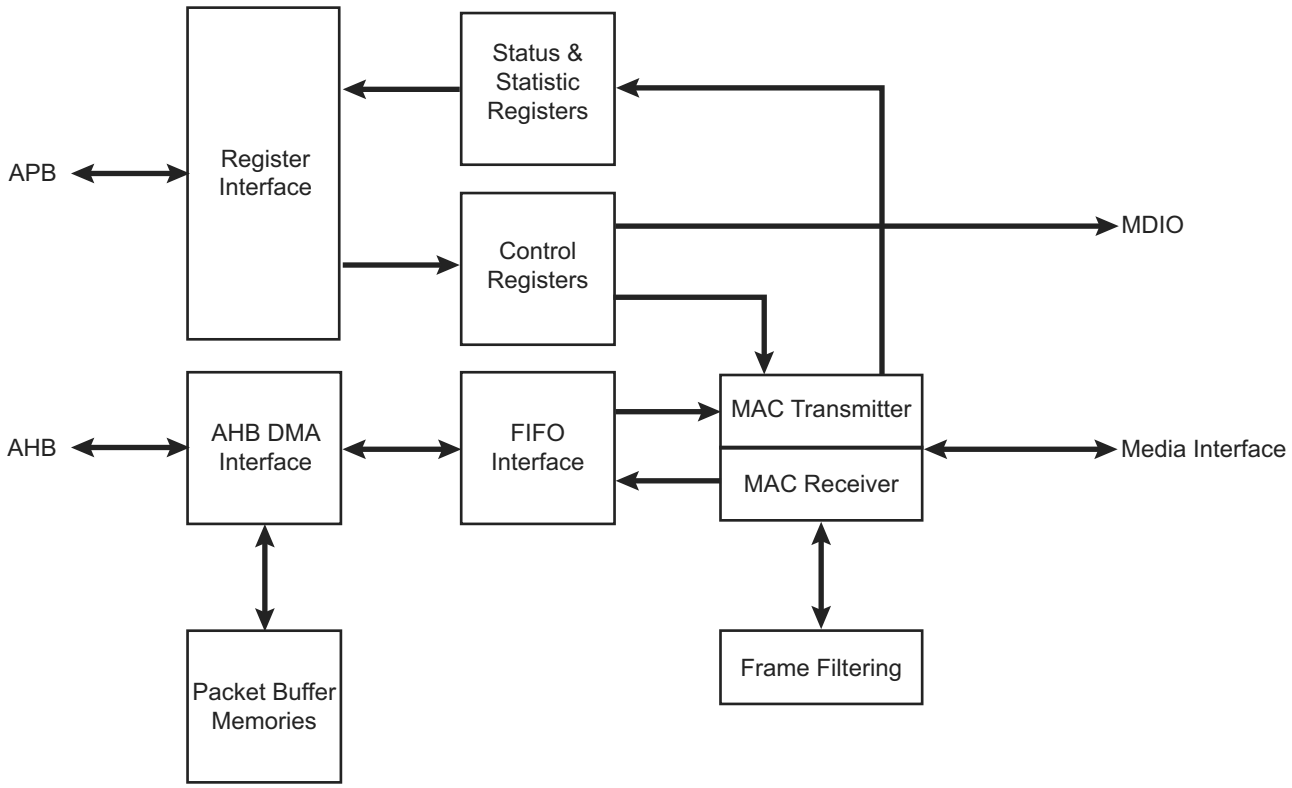
SIPSTS: Synchronization In Progress

0: Clock domain synchronization is terminated.

1: Synchronization is in progress. Access to the registers LCDC_LCDCCFG[0..6], LCDC_LCDEN and LCDC_LCDDIS has no effect.

40.3 Block Diagram

Figure 40-1: Block Diagram



40.4 Signal Interfaces

The GMAC includes the following signal interfaces:

- MII, RMII to an external PHY
- MDIO interface for external PHY management
- Slave APB interface for accessing GMAC registers
- Master AHB interface for memory access
- GTSUCOMP signal for TSU timer count value comparison

Table 40-1: GMAC Connections in Different Modes

Signal Name	Function	MII	RMII
GTXCK[1]	Transmit Clock or Reference Clock	TXCK	REFCK
GTXEN	Transmit Enable	TXEN	TXEN
GTX[3..0]	Transmit Data	TXD[3:0]	TXD[1:0]
GTXER	Transmit Coding Error	TXER	Not Used
GRXCK	Receive Clock	RXCK	Not Used
GRXDV	Receive Data Valid	RXDV	CRSDV
GRX[3..0]	Receive Data	RXD[3:0]	RXD[1:0]
GRXER	Receive Error	RXER	RXER
GCRS	Carrier Sense and Data Valid	CRS	Not Used

40.7.2 Statistics Registers

Statistics registers are described in the User Interface beginning with Section 40.8.47 ”GMAC Octets Transmitted Low Register” and ending with Section 40.8.91 ”GMAC UDP Checksum Errors Register”.

The statistics register block begins at 0x100 and runs to 0x1B0, and comprises the registers listed below.

- Octets Transmitted Low Register
- Octets Transmitted High Register
- Frames Transmitted Register
- Broadcast Frames Transmitted Register
- Multicast Frames Transmitted Register
- Pause Frames Transmitted Register
- 64 Byte Frames Transmitted Register
- 65 to 127 Byte Frames Transmitted Register
- 128 to 255 Byte Frames Transmitted Register
- 256 to 511 Byte Frames Transmitted Register
- 512 to 1023 Byte Frames Transmitted Register
- 1024 to 1518 Byte Frames Transmitted Register
- Greater Than 1518 Byte Frames Transmitted Register
- Transmit Underruns Register
- Single Collision Frames Register
- Multiple Collision Frames Register
- Excessive Collisions Register
- Late Collisions Register
- Deferred Transmission Frames Register
- Carrier Sense Errors Register
- Octets Received Low Register
- Octets Received High Register
- Frames Received Register
- Broadcast Frames Received Register
- Multicast Frames Received Register
- Pause Frames Received Register
- 64 Byte Frames Received Register
- 65 to 127 Byte Frames Received Register
- 128 to 255 Byte Frames Received Register
- 256 to 511 Byte Frames Received Register
- 512 to 1023 Byte Frames Received Register
- 1024 to 1518 Byte Frames Received Register
- 1519 to Maximum Byte Frames Received Register
- Undersize Frames Received Register
- Oversize Frames Received Register
- Jabbers Received Register
- Frame Check Sequence Errors Register
- Length Field Frame Errors Register
- Receive Symbol Errors Register
- Alignment Errors Register
- Receive Resource Errors Register
- Receive Overrun Register
- IP Header Checksum Errors Register
- TCP Checksum Errors Register
- UDP Checksum Errors Register

These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of data.

The receive statistics registers are only incremented when the receive enable bit (RXEN) is set in the Network Control register.

Once a statistics register has been read, it is automatically cleared. When reading the Octets Transmitted and Octets Received registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

40.8.10 GMAC Interrupt Status Register

Name: GMAC_ISR

Address: 0xF8008024

Access: Read-only

31	30	29	28	27	26	25	24
–	–	TSUTIMCOMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
23	22	21	20	19	18	17	16
PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR	–	–
15	14	13	12	11	10	9	8
–	PFTR	PTZ	PFNZ	HRESP	ROVR	–	–
7	6	5	4	3	2	1	0
TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS

This register indicates the source of the interrupt. In order that the bits of this register read 1, the corresponding interrupt source must be enabled in the mask register. If any bit is set in this register, the GMAC interrupt signal will be asserted in the system.

MFS: Management Frame Sent

The PHY Maintenance Register has completed its operation. Cleared on read.

RCOMP: Receive Complete

A frame has been stored in memory. Cleared on read.

RXUBR: RX Used Bit Read

Set when a receive buffer descriptor is read with its used bit set. Cleared on read.

TXUBR: TX Used Bit Read

Set when a transmit buffer descriptor is read with its used bit set. Cleared on read.

TUR: Transmit Underrun

This interrupt is set if the transmitter was forced to terminate a frame that it has already began transmitting due to further data being unavailable.

This interrupt is set if a transmitter status write back has not completed when another status write back is attempted.

This interrupt is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB not OK response was returned, or because the used bit was read.

RLEX: Retry Limit Exceeded

Transmit error. Cleared on read.

TFC: Transmit Frame Corruption Due to AHB Error

Transmit frame corruption due to AHB error. Set if an error occurs while midway through reading transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame.

TCOMP: Transmit Complete

Set when a frame has been transmitted. Cleared on read.

ROVR: Receive Overrun

Set when the receive overrun status bit is set. Cleared on read.

HRESP: HRESP Not OK

Set when the DMA block sees HRESP not OK. Cleared on read.

PFNZ: Pause Frame with Non-zero Pause Quantum Received

PULLD_DIS: Pulldown Disable (cleared upon USB reset)

When set, there is no pulldown on DP & DM. (DM Pulldown = DP Pulldown = 0).

Note: If the DETACH bit is also set, device DP & DM are left in high impedance state. (Refer to “DETACH: Detach Command” .

)

DETACH	PULLD_DIS	DP	DM	Condition
0	0	Pullup	Pulldown	Not recommended
0	1	Pullup	High impedance state	VBUS present
1	0	Pulldown	Pulldown	No VBUS
1	1	High impedance state	High impedance state	VBUS present & software disconnect

43.7.5 CLASSD Transmit Holding Register

Name: CLASSD_THR

Address: 0xFC048010

Access: Read/Write

31	30	29	28	27	26	25	24
RDATA							
23	22	21	20	19	18	17	16
RDATA							
15	14	13	12	11	10	9	8
LDATA							
7	6	5	4	3	2	1	0
LDATA							

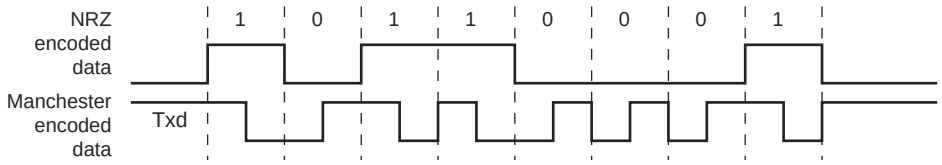
LDATA: Left Channel Data

RDATA: Right Channel Data

47.7.3.2 Manchester Encoder

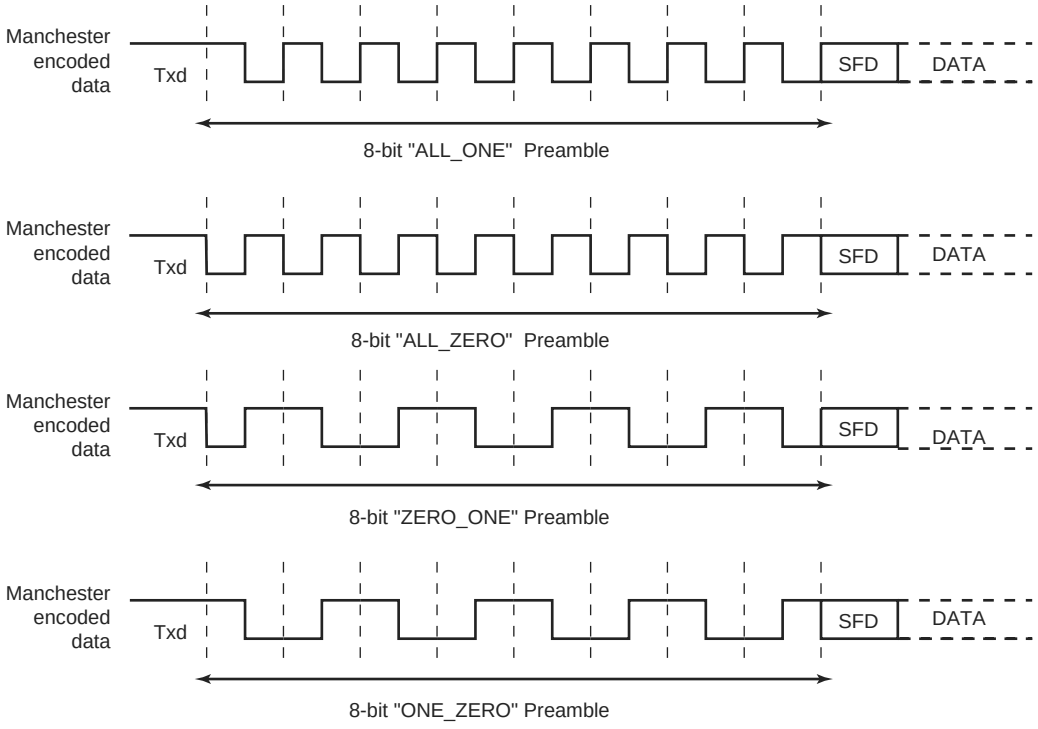
When the Manchester encoder is in use, characters transmitted through the USART are encoded based on biphase Manchester II format. To enable this mode, set the FLEX_US_MR.MAN bit to 1. Depending on polarity configuration, a logic level (zero or one), is transmitted as a coded signal one-to-zero or zero-to-one. Thus, a transition always occurs at the midpoint of each bit time. It consumes more bandwidth than the original NRZ signal (2x) but the receiver has more error control since the expected input must show a change at the center of a bit cell. An example of Manchester encoded sequence is: the byte 0xB1 or 10110001 encodes to 10 01 10 10 01 01 01 10, assuming the default polarity of the encoder. Figure 47-7 illustrates this coding scheme.

Figure 47-7: NRZ to Manchester Encoding



The Manchester encoded character can also be encapsulated by adding both a configurable preamble and a start frame delimiter pattern. Depending on the configuration, the preamble is a training sequence, composed of a predefined pattern with a programmable length from 1 to 15 bit times. If the preamble length is set to 0, the preamble waveform is not generated prior to any character. The preamble pattern is chosen among the following sequences: ALL_ONE, ALL_ZERO, ONE_ZERO or ZERO_ONE, writing the FLEX_US_MAN.TX_PP field. The TX_PL field is used to configure the preamble length. Figure 47-8 illustrates and defines the valid patterns. To improve flexibility, the encoding scheme can be configured using the FLEX_US_MAN.TX_MPOL bit. If the TX_MPOL bit is set to zero (default), a logic zero is encoded with a zero-to-one transition and a logic one is encoded with a one-to-zero transition. If the TX_MPOL bit is set to one, a logic one is encoded with a one-to-zero transition and a logic zero is encoded with a zero-to-one transition.

Figure 47-8: Preamble Patterns, Default Polarity Assumed



A start frame delimiter is to be configured using the FLEX_US_MR.ONEBIT bit. It consists of a user-defined pattern that indicates the beginning of a valid data. Figure 47-9 illustrates these patterns. If the start frame delimiter, also known as the start bit, is one bit, (ONEBIT = 1), a logic zero is Manchester encoded and indicates that a new character is being sent serially on the line. If the start frame delimiter is a synchronization pattern also referred to as sync (ONEBIT = 0), a sequence of three bit times is sent serially on the line to indicate the start of a new character. The sync waveform is in itself an invalid Manchester waveform as the transition occurs at the middle of the second bit time. Two distinct sync patterns are used: the command sync and the data sync. The command sync has a logic one level for one and

47.10.79 TWI FIFO Mode Register

Name: FLEX_TWI_FMR

Address: 0xF8034650 (0), 0xF8038650 (1), 0xFC010650 (2), 0xFC014650 (3), 0xFC018650 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	RXFTHRES					
23	22	21	20	19	18	17	16
–	–	TXFTHRES					
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	RXRDYM		–	–	TXRDYM	

TXRDYM: Transmitter Ready Mode

If FIFOs are enabled, the FLEX_TWI_SR.TXRDY flag behaves as follows.

Value	Name	Description
0	ONE_DATA	TXRDY will be at level ‘1’ when at least one data can be written in the Transmit FIFO
1	TWO_DATA	TXRDY will be at level ‘1’ when at least two data can be written in the Transmit FIFO
2	FOUR_DATA	TXRDY will be at level ‘1’ when at least four data can be written in the Transmit FIFO

RXRDYM: Receiver Ready Mode

If FIFOs are enabled, the FLEX_TWI_SR.RXRDY flag behaves as follows.

Value	Name	Description
0	ONE_DATA	RXRDY will be at level ‘1’ when at least one unread data is in the Receive FIFO
1	TWO_DATA	RXRDY will be at level ‘1’ when at least two unread data are in the Receive FIFO
2	FOUR_DATA	RXRDY will be at level ‘1’ when at least four unread data are in the Receive FIFO

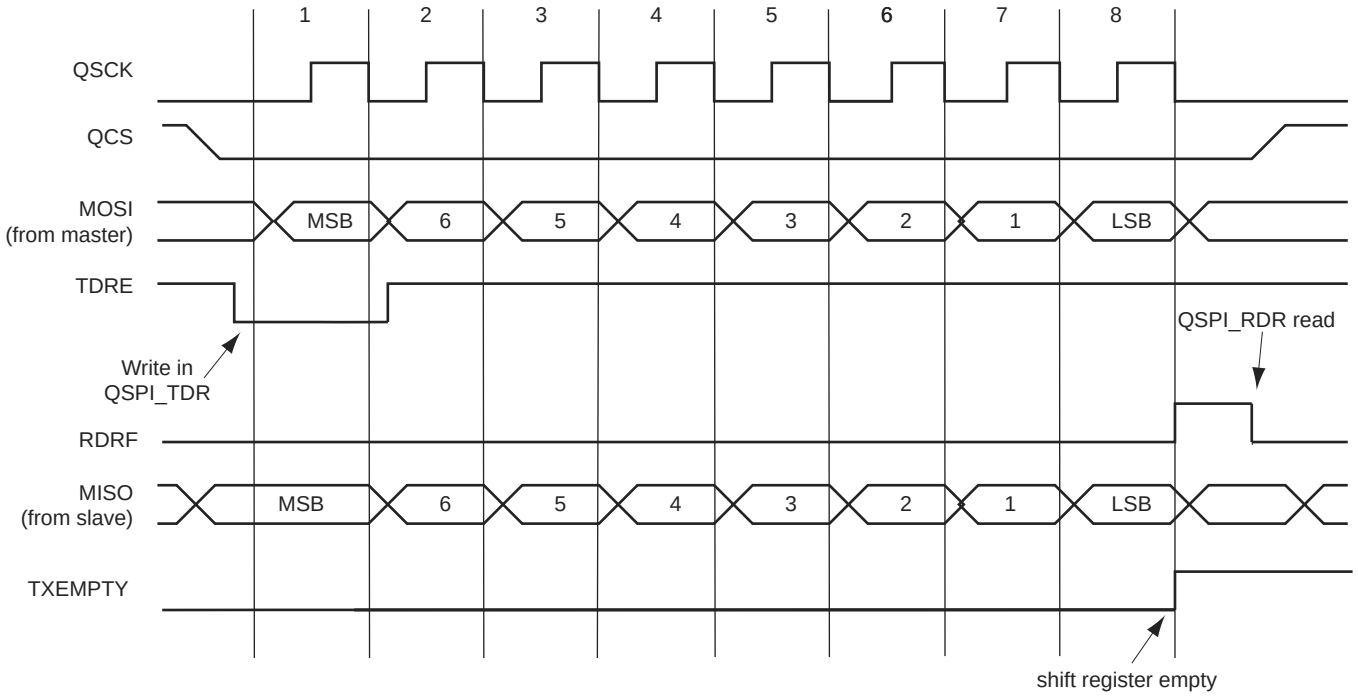
TXFTHRES: Transmit FIFO Threshold

0–16: Defines the Transmit FIFO threshold value (number of data). The FLEX_TWI_FSR.TXFTH flag will be set when Transmit FIFO goes from “above” threshold state to “equal or below” threshold state.

RXFTHRES: Receive FIFO Threshold

0–16: Defines the Receive FIFO threshold value (number of data). The FLEX_TWI_FSR.RXFTH flag will be set when Receive FIFO goes from “below” threshold state to “equal to or above” threshold state.

Figure 50-7: Status Register Flags Behavior



50.6.4.4 Peripheral Deselection without DMA

During a transfer of more than one data on a Chip Select without the DMA, the QSPI_TDR is loaded by the processor and the flag TDRE rises as soon as the content of the QSPI_TDR is transferred into the internal shift register. When this flag is detected high, the QSPI_TDR can be reloaded. If this reload by the processor occurs before the end of the current transfer and if the next transfer is performed on the same chip select as the current transfer, the Chip Select is not deasserted between the two transfers. Depending on the application software handling the QSPI_SR flags (by interrupt or polling method) or servicing other interrupts or other tasks, the processor may not reload the QSPI_TDR in time to keep the chip select active (low). A null Delay Between Consecutive Transfer (DLYBCT) value in the QSPI_MR gives even less time for the processor to reload the QSPI_TDR. With some SPI slave peripherals, requiring the chip select line to remain active (low) during a full set of transfers may lead to communication errors.

To facilitate interfacing with such devices, QSPI_MR.CSMODE may be configured to ‘1’. This allows the chip select lines to remain in their current state (low = active) until the end of transfer is indicated by the Last Transfer (LASTXFER) bit in the Control register (QSPI_CR). Even if the QSPI_TDR is not reloaded, the chip select remains active. To have the chip select line rise at the end of the last data transfer, QSPI_CR.LASTXFER must be written to ‘1’ at the same time or after writing the last data to transmit into the QSPI_TDR.

50.6.4.5 Peripheral Deselection with DMA

When the DMA Controller is used, the Chip Select line remains low during the transfer since the TDRE flag is managed by the DMA itself. Reloading the QSPI_TDR by the DMA is done as soon as the TDRE flag is set. In this case, writing QSPI_MR.CSMODE to ‘1’ may not be needed. However, when other DMA channels connected to other peripherals are also in use, the QSPI DMA could be delayed by another DMA with a higher priority on the bus. Having DMA buffers in slower memories like Flash memory or SDRAM compared to fast internal SRAM, may lengthen the reload time of the QSPI_TDR by the DMA as well. This means that the QSPI_TDR might not be reloaded in time to keep the chip select line low. In this case, the chip select line may toggle between data transfer and according to some SPI Slave devices, the communication might get lost. It may be necessary to configure QSPI_MR.CSMODE to ‘1’.

When QSPI_MR.CSMODE is configured to ‘0’, the QCS does not rise in all cases between two transfers on the same peripheral. During a transfer on a Chip Select, the flag TDRE rises as soon as the content of the QSPI_TDR is transferred into the internal shifter. When this flag is detected, the QSPI_TDR can be reloaded. If this reload occurs before the end of the current transfer and if the next transfer is performed on the same chip select as the current transfer, the Chip Select is not deasserted between the two transfers. This might lead to difficulties for interfacing with some serial peripherals requiring the chip select to be deasserted after each transfer. To facilitate interfacing with such devices, the QSPI_MR may be configured with QSPI_MR.CSMODE at ‘2’.

50.7.12 QSPI Instruction Frame Register

Name: QSPI_IFR

Address: 0xF0020038 (0), 0xF0024038 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	NBDUM				
15	14	13	12	11	10	9	8
–	CRM	TFRTYP		–	ADDRL	OPTL	
7	6	5	4	3	2	1	0
DATAEN	OPTEN	ADDREN	INSTEN	–	WIDTH		

WIDTH: Width of Instruction Code, Address, Option Code and Data

Value	Name	Description
0	SINGLE_BIT_SPI	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Single-bit SPI
1	DUAL_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Dual SPI
2	QUAD_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Quad SPI
3	DUAL_IO	Instruction: Single-bit SPI / Address-Option: Dual SPI / Data: Dual SPI
4	QUAD_IO	Instruction: Single-bit SPI / Address-Option: Quad SPI / Data: Quad SPI
5	DUAL_CMD	Instruction: Dual SPI / Address-Option: Dual SPI / Data: Dual SPI
6	QUAD_CMD	Instruction: Quad SPI / Address-Option: Quad SPI / Data: Quad SPI

INSTEN: Instruction Enable

0: The instruction is not sent to the serial Flash memory.

1: The instruction is sent to the serial Flash memory.

ADDREN: Address Enable

0: The transfer address is not sent to the serial Flash memory.

1: The transfer address is sent to the serial Flash memory.

OPTEN: Option Enable

0: The option is not sent to the serial Flash memory.

1: The option is sent to the serial Flash memory.

DATAEN: Data Enable

0: No data is sent/received to/from the serial Flash memory.

1: Data is sent/received to/from the serial Flash memory.

OPTL: Option Code Length

- When all valid data blocks in the SDMMC have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request (STPBGR) of SDMMC_BGCR being set to 1.

A change from 1 to 0 raises the Transfer Complete (TRFC) status flag in SDMMC_NISTR if SDMMC_NISTER.TRFC is set to 1. An interrupt is generated if SDMMC_NISIER.TRFC is set to 1.

BUFWREN: Buffer Write Enable

This bit is used for nonDMA write transfers. This flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer.

A change from 1 to 0 occurs when all the block data are written to the buffer.

A change from 0 to 1 occurs when top of block data can be written to the buffer. This raises the Buffer Write Ready (BWRRDY) status flag in SDMMC_NISTR if SDMMC_NISTER.BWRRDY is set to 1. An interrupt is generated if SDMMC_NISIER.BWRRDY is set to 1.

BUFRDEN: Buffer Read Enable

This bit is used for nonDMA read transfers. This flag indicates that valid data exists in the SDMMC data buffer. If this bit is 1, readable data exists in the buffer.

A change from 1 to 0 occurs when all the block data is read from the buffer.

A change from 0 to 1 occurs when block data is ready in the buffer. This raises the Buffer Read Ready (BRDRDY) status flag in SDMMC_NISTR if SDMMC_NISTER.BRDRDY is set to 1. An interrupt is generated if SDMMC_NISIER.BRDRDY is set to 1.

CARDINS: Card Inserted

This bit indicates wether a card has been inserted. The SDMMC debounces this signal so that the user does not need to wait for it to stabilize.

A change from 0 to 1 raises the Card Insertion (CINS) status flag in SDMMC_NISTR if SDMMC_NISTER.CINS is set to 1. An interrupt is generated if SDMMC_NISIER.CINS is set to 1.

A change from 1 to 0 raises the Card Removal (CREM) status flag in SDMMC_NISTR if SDMMC_NISTER.CREM is set to 1. An interrupt is generated if SDMMC_NISIER.CREM is set to 1.

The Software Reset For All (SWRSTALL) in SDMMC_SRR does not affect this bit.

CARDSS: Card State Stable

This bit is used for testing. If it is 0, the CARDDPL is not stable. If this bit is set to 1, it means that the CARDDPL is stable. No Card state can be detected if this bit is set to 1 and CARDINS is set to 0.

The Software Reset For All (SWRSTALL) in SDMMC_SRR does not affect this bit.

0: Reset or debouncing.

1: No card or card inserted.

CARDDPL: Card Detect Pin Level

This bit reflects the inverse value of the SDMMC_CD pin. Debouncing is not performed on this bit. This bit may be valid when CARDSS is set to 1, but it is not guaranteed because of the propagation delay. Use of this bit is limited to testing since it must be debounced by software.

0: No card present (SDMMC_CD = 1).

1: Card present (SDMMC_CD = 0).

WRPPL: Write Protect Pin Level

The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDMMC_WP pin.

0: Write protected (SDMMC_WP = 0)

1: Write enabled (SDMMC_WP = 1)

DATLL: DAT[3:0] Line Level

This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the Busy signal level from DAT[0].

CMDLL: CMD Line Level

This status is used to check the CMD line level to recover from errors, and for debugging.

Table 66-14: Typical Power Consumption for Backup Mode

V_{DDBU} (V)	Conditions	Consumption (µA)				Unit
		T_A = 25°C	T_A = 70°C	T_A = 85°C	T_A = 105°C	
1.6	V_{DDBU} Only	4.2	12.1	19.3	36.8	µA
1.7		4.2	12.1	19.3	36.9	
1.8		4.3	12.1	19.4	36.9	
1.9		4.3	12.1	19.4	36.9	
2		4.3	12.1	19.4	37	
2.1		4.3	12.2	19.4	37	
2.2		4.3	12.2	19.5	37	
2.3		4.4	12.2	19.5	37	
2.4		4.4	12.2	19.5	37	
2.5		4.4	12.3	19.5	37.1	
2.6		4.4	12.3	19.6	37.1	
2.7		4.4	12.3	19.6	37.1	
2.8		4.4	12.3	19.6	37.2	
2.9		4.5	12.4	19.6	37.2	
3		4.5	12.4	19.7	37.3	
3.1		4.5	12.5	19.8	37.7	
3.2		4.6	12.8	20.3	38.3	
3.3		4.9	13.4	20.9	38.9	
3.4		5.5	14.1	21.6	39.7	
3.5		6.2	14.9	22.4	40.5	
3.6		7	15.7	23.3	41.4	

66.6 Clock Characteristics

66.6.1 Processor Clock Characteristics

Table 66-15: Processor Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPPCK})$	Processor Clock Frequency	VDDCORE[1.1V, 1.32V], T_A = [-40°C, +85°C]	250(1)	400	MHz
		VDDCORE[1.2V, 1.32V], T_A = [-40°C, +85°C]	250(1)	500	

Note 1: Limitation for DDR2 (125 MHz) usage only. There are no limitations to DDR3, DDR3L, LPDDR1, LPDDR2 and LPDDR3.

66.7.3 32.768 kHz Crystal Oscillator Characteristics

Table 66-21: 32.768 kHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	Normal mode with crystal		–	32.768	–	kHz
t_{START}	Startup Time	C_m > 3fF		–	–	1200	ms
I_{DDON}	Current Consumption	ESR < 50k ohm	$C_{CRYSTAL32}$ = 12.5 pF	–	440	900	nA
			$C_{CRYSTAL32}$ = 6 pF		600	900	
		ESR < 100k ohm	$C_{CRYSTAL32}$ = 12.5 pF		800	1200	
			$C_{CRYSTAL32}$ = 6 pF		700	1200	
C_{PARA32}	Internal Parasitic Capacitance	Between XIN32 and XOUT32		1.4	1.6	1.8	pF

Figure 66-4: 32 kHz Oscillator Schematics

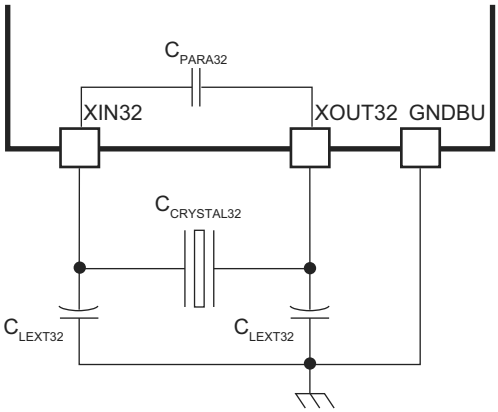


Table 66-22: Recommended 32.768 kHz Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor	Crystal at 32.768 kHz	–	–	100	kΩ
–	Duty Cycle	–	40	50	60	%
C_m	Motional Capacitance	Crystal at 32.768 kHz	3	–	8	fF
C_{SHUNT}	Shunt Capacitance	Crystal at 32.768 kHz	0.6	–	2	pF
$C_{CRYSTAL32}$	Allowed Crystal Capacitance Load(1)	From crystal specification	6	–	12.5	pF
P_{ON}	Drive Level	–	–	–	0.2	µW

Note: 1. The external capacitors value can be determined by using the following formula:

$C_{LEXT32} = (2 \times C_{CRYSTAL32}) - C_{BOARD} - (C_{PARA32} \times 2)$

where:

C_{LEXT32} is the external capacitor value which must be soldered from XIN32 to GND and XOUT32 to GND

$C_{CRYSTAL32}$ is the crystal targeted load

C_{BOARD} is the external board parasitic capacitance (from XIN to GND or XOUT to GND)

C_{PARA32} is the internal parasitic capacitance

66.7.4 64 kHz RC Oscillator Characteristics

Table 66-23: 64 kHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	RC Oscillator Frequency	–	40		90	kHz
t_{START}	Startup Time	–	11	17	30	µs
I_{DDON}	Current Consumption	After startup time	–	93	140	nA

66.8 PLL Characteristics

Table 66-24: PLLA Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IN}	Input Frequency	–	8	–	24	MHz
f_{OUT}	Output Frequency	–	600	–	1200	MHz
I_{PLL}	Current Consumption	Active mode	–	–	14.5	mA
		Standby mode	–	–	2	µA
t_{START}	Startup Time	–	–	–	60	µs

Table 66-25: UTMI PLL Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IN}	Input Frequency	–	12	–	24	MHz
f_{OUT}	Output Frequency	–		480		MHz
$I_{VDDUTMII}$	Current Consumption	In Active mode, on VDDUTMII, @480 MHz	–	6.3	7.0	mA
t_{START}	Startup Time	–	–	–	60	µs

Table 66-26: Audio PLL Characteristics

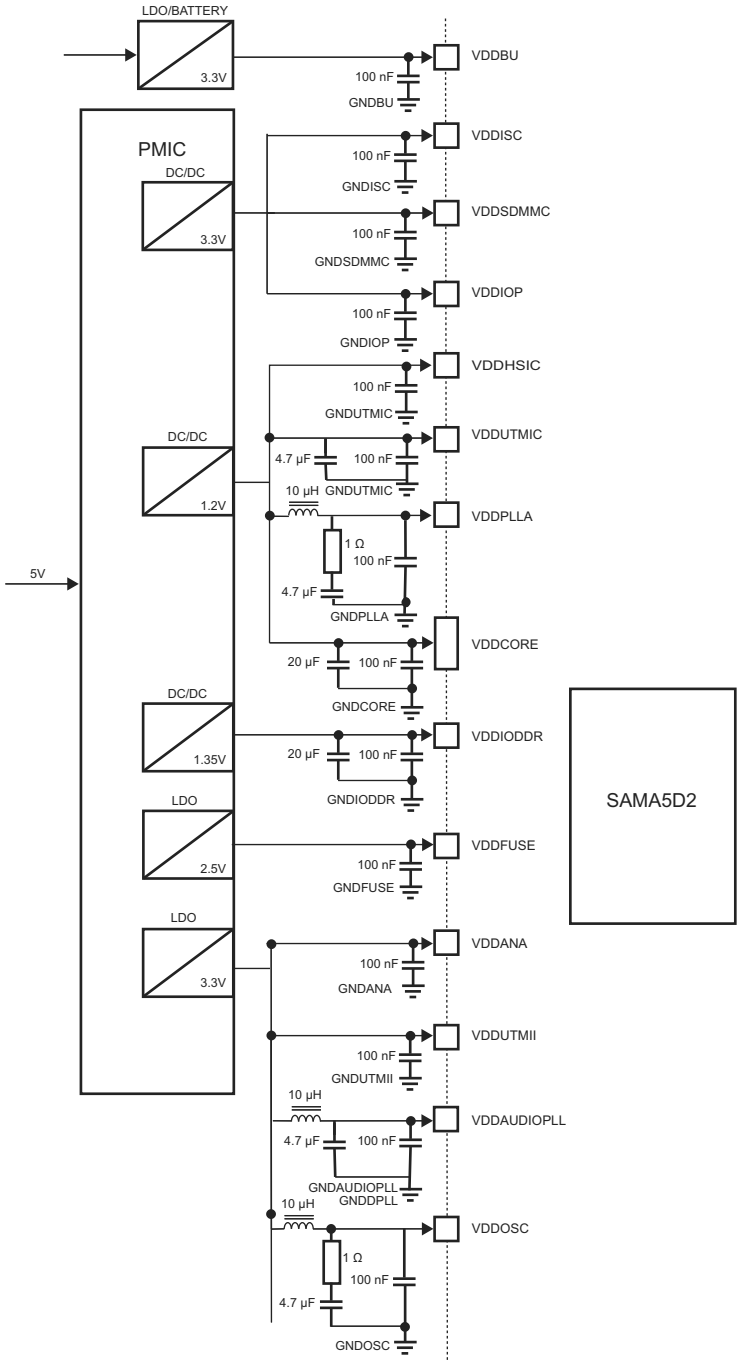
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IN}	Input Frequency	–	12	–	24	MHz
$f_{AUDIOCORECLK}$	AUDIOCORECLK frequency range	–	620	–	700	MHz
$f_{AUDIOPINCLK}$	AUDIOPINCLK frequency range	–	8	12.288	48	MHz
$f_{AUDIOPLLCLK}$	AUDIOPLLCLK frequency range	–	–	–	150	MHz
I_{PLL}	Current Consumption	On VDDAUDIOPLL	6	–	20	mA
t_{START}	Startup Time	From OFF to stable AUDIOCORECLK frequency	–	–	100	µs
t_{SET}	Settling Time(1)	When changing FRACR or NR in PMC_AUDIO_PLL0 or PMC_AUDIO_PLL1	–	–	100	µs

Note: 1. Loop filter is set as recommended in fields BIAS_FILTER and DCO_FILTER of PMC_AUDIO_PLL0.

68.1 Power Supply

CAUTION: The board design must comply with the powerup and powerdown sequence guidelines provided in the datasheet to guarantee reliable operation of the device.

Figure 68-1: 1.2V, 1.35V/1.5V, 2V, 2.5V, 3.3V Power Supplies Schematics(1)



Note 1: These values are given only as typical examples.