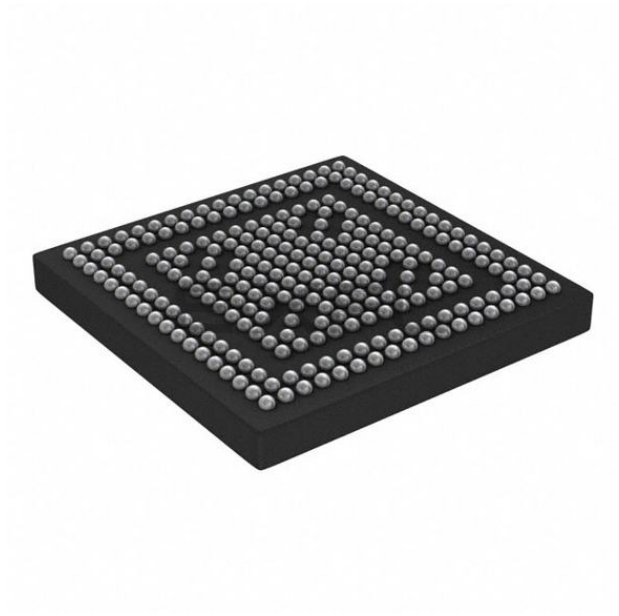

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	256-TFBGA
Supplier Device Package	256-TFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d24c-cur

Table 18-10: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x025C	Security Areas Split Slave 7 Register	MATRIX_SASSR7	Read/Write	(1)
0x0260	Security Areas Split Slave 8 Register	MATRIX_SASSR8	Read/Write	(1)
0x0264	Security Areas Split Slave 9 Register	MATRIX_SASSR9	Read/Write	(1)
0x0268	Security Areas Split Slave 10 Register	MATRIX_SASSR10	Read/Write	(1)
0x026C	Security Areas Split Slave 11 Register	MATRIX_SASSR11	Read/Write	(1)
0x0270	Security Areas Split Slave 12 Register	MATRIX_SASSR12	Read/Write	(1)
0x0274	Security Areas Split Slave 13 Register	MATRIX_SASSR13	Read/Write	(1)
0x0278	Security Areas Split Slave 14 Register	MATRIX_SASSR14	Read/Write	(1)
0x027C–0x0280	Reserved	–	–	–
0x0284	Security Region Top Slave 1 Register	MATRIX_SRTSR1	Read/Write	0x00000000
0x0288	Security Region Top Slave 2 Register	MATRIX_SRTSR2	Read/Write	0x00000000
0x028C	Security Region Top Slave 3 Register	MATRIX_SRTSR3	Read/Write	0x00000000
0x0290	Security Region Top Slave 4 Register	MATRIX_SRTSR4	Read/Write	0x00000000
0x0294	Security Region Top Slave 5 Register	MATRIX_SRTSR5	Read/Write	0x00000000
0x0298	Security Region Top Slave 6 Register	MATRIX_SRTSR6	Read/Write	0x00000000
0x029C	Security Region Top Slave 7 Register	MATRIX_SRTSR7	Read/Write	0x00000000
0x02A0	Security Region Top Slave 8 Register	MATRIX_SRTSR8	Read/Write	0x00000000
0x02A4	Security Region Top Slave 9 Register	MATRIX_SRTSR9	Read/Write	0x00000000
0x02A8	Security Region Top Slave 10 Register	MATRIX_SRTSR10	Read/Write	0x00000000
0x02AC	Security Region Top Slave 11 Register	MATRIX_SRTSR11	Read/Write	0x00000000
0x02B0	Security Region Top Slave 12 Register	MATRIX_SRTSR12	Read/Write	0x00000000
0x02B4	Security Region Top Slave 13 Register	MATRIX_SRTSR13	Read/Write	0x00000000
0x02B8	Security Region Top Slave 14 Register	MATRIX_SRTSR14	Read/Write	0x00000000
0x02BC	Reserved	–	–	–
0x02C0	Security Peripheral Select 1 Register	MATRIX_SPSELR1	Read/Write	0x00000000(2)
0x02C4	Security Peripheral Select 2 Register	MATRIX_SPSELR2	Read/Write	0x00000000(3)
0x02C8	Security Peripheral Select 3 Register	MATRIX_SPSELR3	Read/Write	0x00000000(4)

Note 1: When applicable to an AHB slave region, the initial value of MATRIX_SASSRx.SASPLITy is 0xF. When not applicable to an AHB slave region, the initial value of MATRIX_SASSRx.SASPLITy is 0x0.

2: This value is 0x000D2504 for H32MX and 0xFFF2DAFB for H64MX.

3: This value is 0x011C0000 for H32MX and 0xFFE7FFFF for H64MX.

4: This value is 0xFFFFFFFA for H32MX and 0xFFFFFFE7 for H64MX.

26.5.7 RTC Accurate Clock Calibration

The crystal oscillator that drives the RTC may not be as accurate as expected mainly due to temperature variation. The RTC is equipped with circuitry able to correct slow clock crystal drift.

To compensate for possible temperature variations over time, this accurate clock calibration circuitry can be programmed on-the-fly and also programmed during application manufacturing, in order to correct the crystal frequency accuracy at room temperature (20–25°C). The typical clock drift range at room temperature is ±20 ppm.

In the device operating temperature range, the 32.768 kHz crystal oscillator clock inaccuracy can be up to -200 ppm.

The RTC clock calibration circuitry allows positive or negative correction in a range of 1.5 ppm to 1950 ppm.

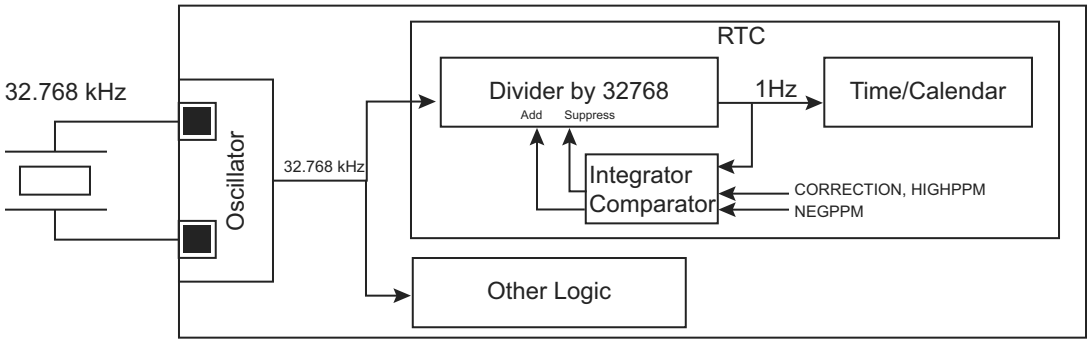
The calibration circuitry is fully digital. Thus, the configured correction is independent of temperature, voltage, process, etc., and no additional measurement is required to check that the correction is effective.

If the correction value configured in the calibration circuitry results from an accurate crystal frequency measure, the remaining accuracy is bounded by the values listed below:

- Below 1 ppm, for an initial crystal drift between 1.5 ppm up to 20 ppm, and from 30 ppm to 90 ppm
- Below 2 ppm, for an initial crystal drift between 20 ppm up to 30 ppm, and from 90 ppm to 130 ppm
- Below 5 ppm, for an initial crystal drift between 130 ppm up to 200 ppm

The calibration circuitry does not modify the 32.768 kHz crystal oscillator clock frequency but it acts by slightly modifying the 1 Hz clock period from time to time. The correction event occurs every 1 + [(20 - (19 x HIGHPPM)) x CORRECTION] seconds. When the period is modified, depending on the sign of the correction, the 1 Hz clock period increases or reduces by around 4 ms. Depending on the CORRECTION, NEGPPM and HIGHPPM values configured in RTC_MR, the period interval between two correction events differs.

Figure 26-6: Calibration Circuitry



34.7.24 Secure PIO Interrupt Mask Register

Name: S_PIO_IMRx [x=0..3]

Address: 0xFC039028 [0], 0xFC039068 [1], 0xFC0390A8 [2], 0xFC0390E8 [3]

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0–P31: Input Change Interrupt Mask

0: Input Change interrupt is disabled on the I/O line of the I/O group x.

1: Input Change interrupt is enabled on the I/O line of the I/O group x.

38.9.21 XDMAC Channel x [x = 0..15] Interrupt Status Register

Name: XDMAC_CISx [x = 0..15]

Address: 0xF000405C (1)[0], 0xF000409C (1)[1], 0xF00040DC (1)[2], 0xF000411C (1)[3], 0xF000415C (1)[4], 0xF000419C (1)[5], 0xF00041DC (1)[6], 0xF000421C (1)[7], 0xF000425C (1)[8], 0xF000429C (1)[9], 0xF00042DC (1)[10], 0xF000431C (1)[11], 0xF000435C (1)[12], 0xF000439C (1)[13], 0xF00043DC (1)[14], 0xF000441C (1)[15], 0xF001005C (0)[0], 0xF001009C (0)[1], 0xF00100DC (0)[2], 0xF001011C (0)[3], 0xF001015C (0)[4], 0xF001019C (0)[5], 0xF00101DC (0)[6], 0xF001021C (0)[7], 0xF001025C (0)[8], 0xF001029C (0)[9], 0xF00102DC (0)[10], 0xF001031C (0)[11], 0xF001035C (0)[12], 0xF001039C (0)[13], 0xF00103DC (0)[14], 0xF001041C (0)[15]

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS

BIS: End of Block Interrupt Status Bit

0: End of block interrupt has not occurred.

1: End of block interrupt has occurred since the last read of the Status register.

LIS: End of Linked List Interrupt Status Bit

0: End of linked list condition has not occurred.

1: End of linked list condition has occurred since the last read of the Status register.

DIS: End of Disable Interrupt Status Bit

0: End of disable condition has not occurred.

1: End of disable condition has occurred since the last read of the Status register.

FIS: End of Flush Interrupt Status Bit

0: End of flush condition has not occurred.

1: End of flush condition has occurred since the last read of the Status register.

RBEIS: Read Bus Error Interrupt Status Bit

0: Read bus error condition has not occurred.

1: At least one bus error has been detected in a read access since the last read of the Status register.

WBEIS: Write Bus Error Interrupt Status Bit

0: Write bus error condition has not occurred.

1: At least one bus error has been detected in a write access since the last read of the Status register.

ROIS: Request Overflow Error Interrupt Status Bit

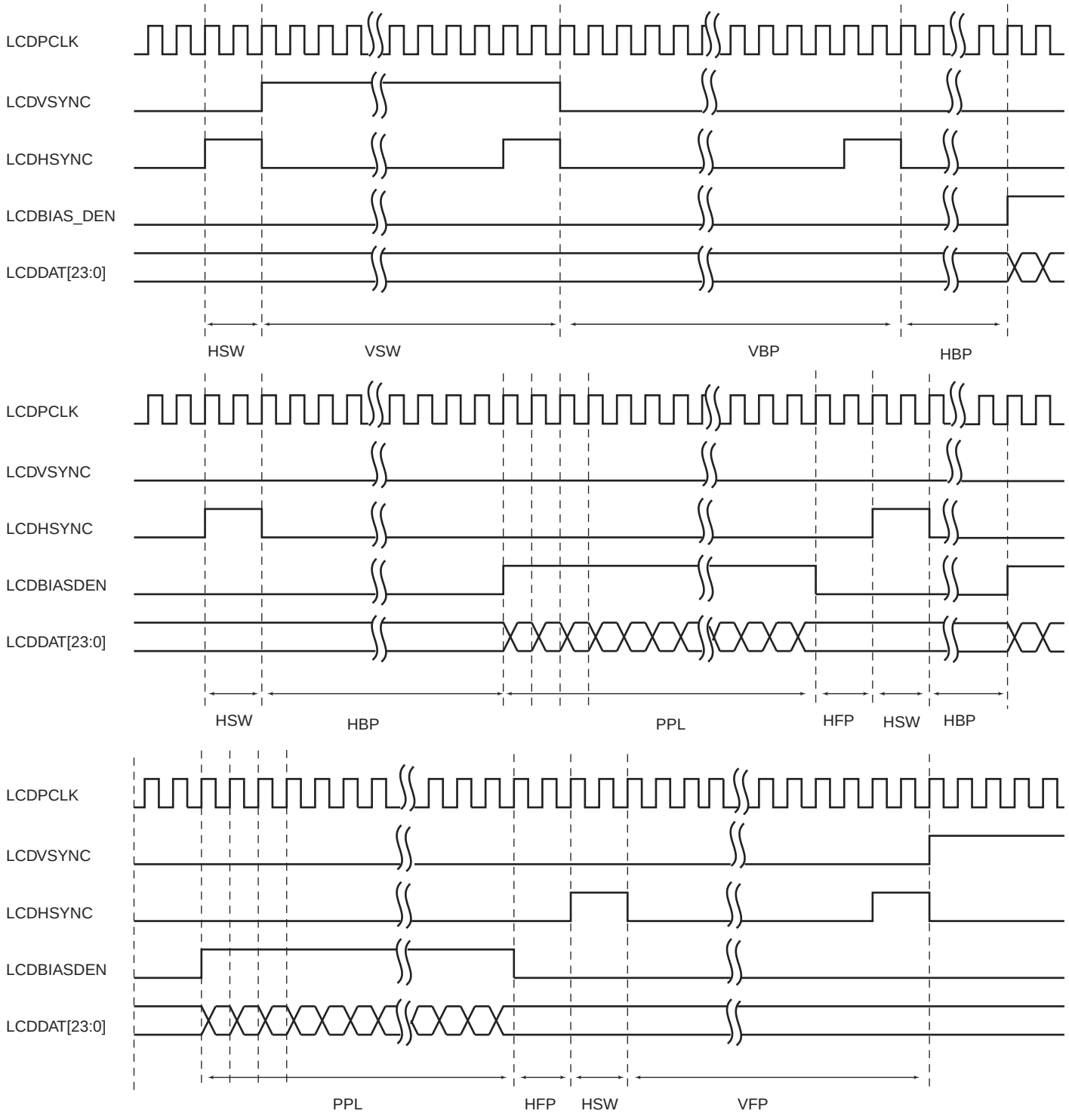
0: Overflow condition has not occurred.

1: Overflow condition has occurred at least once. (This information is only relevant for peripheral synchronized transfers.)

39.6.16 Output Timing Generation

39.6.16.1 Active Display Timing Mode

Figure 39-14: Active Display Timing



39.7.97 High-End Overlay Configuration Register 2

Name: LCDC_HEOCFG2

Address: 0xF0000394

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	YPOS		

23	22	21	20	19	18	17	16
YPOS							

15	14	13	12	11	10	9	8
–	–	–	–	–	XPOS		

7	6	5	4	3	2	1	0
XPOS							

XPOS: Horizontal Window Position

High-End Overlay Horizontal window position.

YPOS: Vertical Window Position

High-End Overlay Vertical window position.

40.8.106 GMAC Received LPI Transitions

Name: GMAC_RXLPI

Address: 0xF8008270

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
COUNT							

7	6	5	4	3	2	1	0
COUNT							

COUNT: Count of RX LPI transitions (cleared on read)

A count of the number of times there is a transition from receiving normal idle to receiving low power idle.

40.8.124 GMAC Screening Type 2 Compare Word 1 Register x

Name: GMAC_ST2CW1x[x=0..23]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	OFFSSTRT

7	6	5	4	3	2	1	0
OFFSSTRT	OFFSVAL						

OFFSVAL: Offset Value in Bytes

The value of OFFSVAL ranges from 0 to 127 bytes, and is counted from either the start of the frame, the byte after the EtherType field (last EtherType in the header if the frame is VLAN tagged), the byte after the IP header (IPv4 or IPv6) or the byte after the TCP/UDP header.

OFFSSTRT: Ethernet Frame Offset Start

Value	Name	Description
0	FRAMESTART	Offset from the start of the frame
1	ETHERTYPE	Offset from the byte after the EtherType field
2	IP	Offset from the byte after the IP header field
3	TCP_UDP	Offset from the byte after the TCP/UDP header field

45.5 SSC Application Examples

The SSC can support several serial communication modes used in audio or high speed serial links. Some standard applications are shown in the following figures. All serial link applications supported by the SSC are not listed here.

Figure 45-3: Audio Application Block Diagram

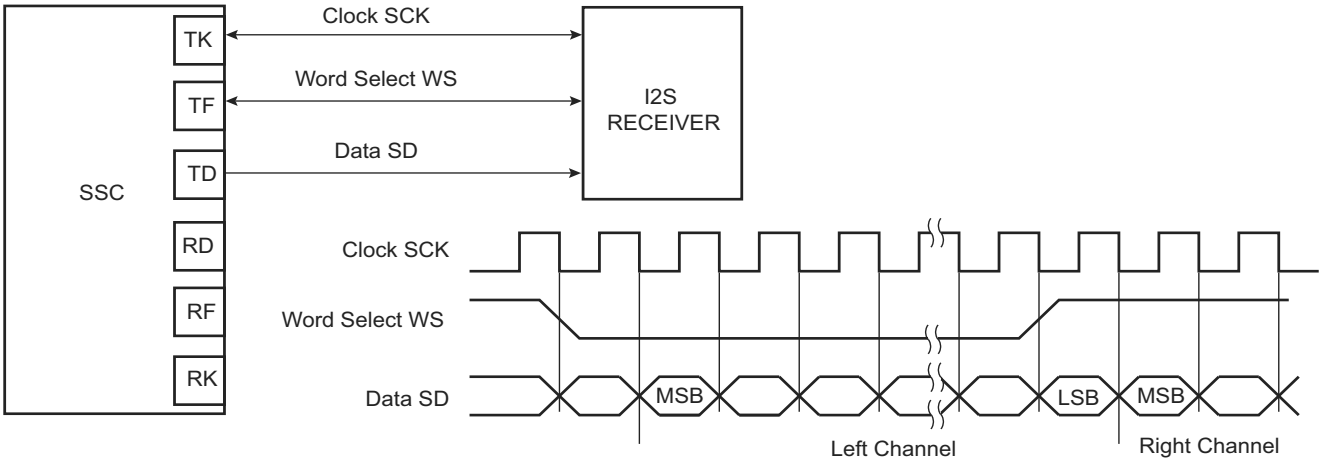


Figure 45-4: Codec Application Block Diagram

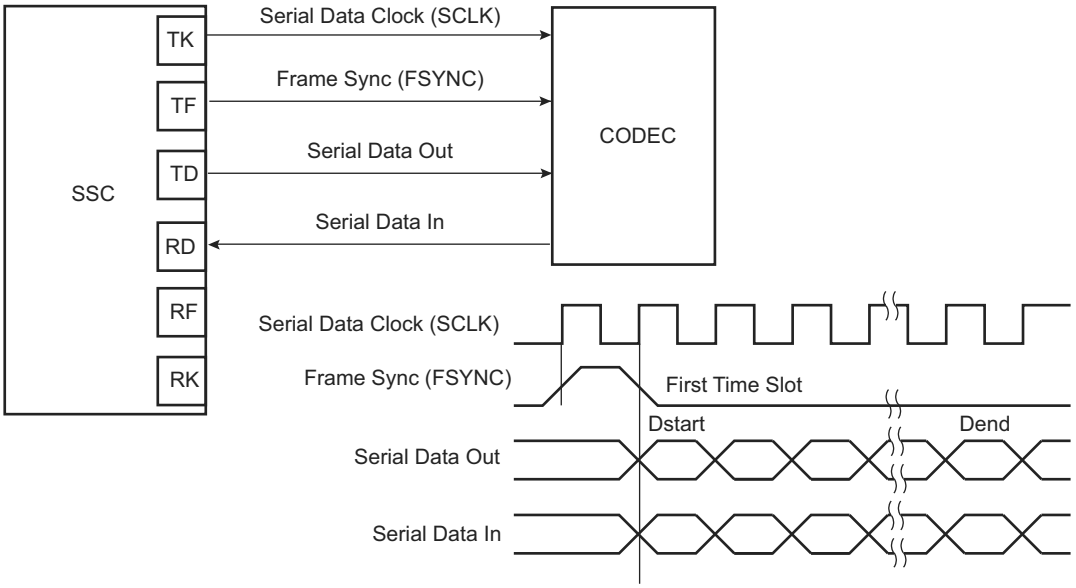
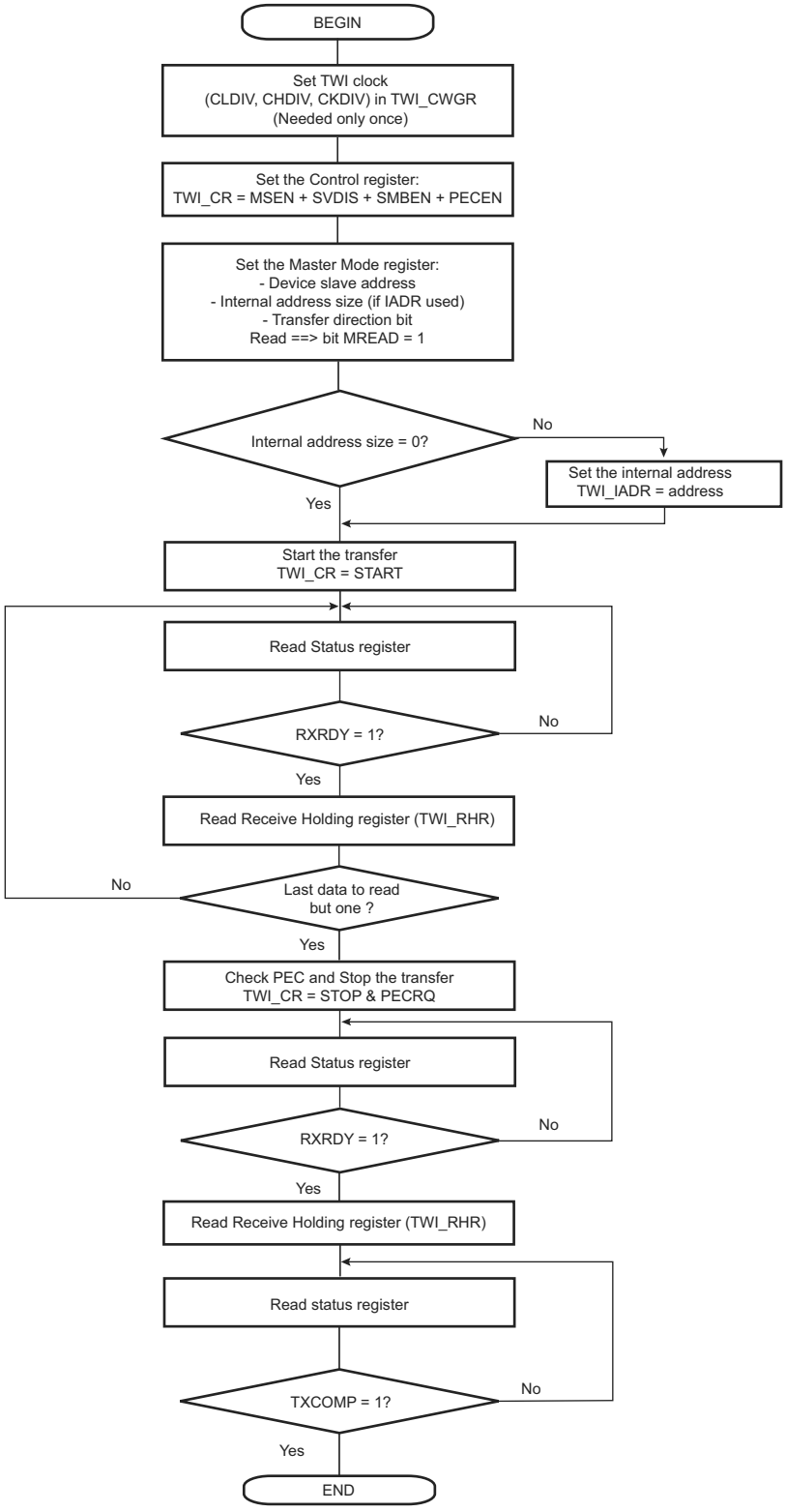


Figure 46-24: TWIHS Read Operation with Multiple Data Bytes with or without Internal Address with PEC



Similarly, for a Receive FIFO containing six data, the options are:

- Perform six TWIHS_RHR-byte read accesses.
- Perform three TWIHS_RHR-halfword read accesses.
- Perform one TWIHS_RHR-word read access and one TWIHS_RHR-halfword read access.

This mode can minimize the number of accesses by concatenating the data to send/read in one access.

- TXRDY and RXRDY Configuration

In Multiple Data mode, the TXRDYM and RXRDYM fields in the TWIHS_FMR become useful.

As in Multiple Data mode, it is possible to write several data in the same access it might be useful to configure TXRDY flag behavior to indicate if 1, 2 or 4 data can be written in the FIFO depending on the access to perform on TWIHS_THR.

If for instance four data are written each time in the TWIHS_THR it might be useful to configure TXRDYM field to 0x2 value so that TXRDY flag will be at ‘1’ only when at least four data can be written in the Transmit FIFO.

In the same way if four data are read each time in the TWIHS_RHR it might be useful to configure RXRDYM field to 0x2 value so that RXRDY flag will be at ‘1’ only when at least four unread data are in the Receive FIFO.

- DMAC

If DMAC transfer is used it is mandatory to configure TXRDYM/RXRDYM to the right value depending on the DMAC channel size (byte, halfword or word).

- Transmit FIFO Lock

If a frame is terminated early due to a not-acknowledge error (NACK flag), SMBus timeout error (TOUT flag) or master code acknowledge error (MACK flag), a lock is set on the Transmit FIFO preventing any new frame from being sent until it is cleared. This allows clearing the FIFO if needed, reset DMAC channels, etc., without any risk.

The LOCK bit in the TWIHS_SR is used to check the state of the Transmit FIFO lock.

The Transmit FIFO lock can be cleared setting the TXFLCLR bit to ‘1’ in the TWIHS_CR.

- FIFO Pointer Error

In some specific cases, it is possible to generate a FIFO pointer error.

- Transmit FIFO:

If the Transmit FIFO is full and a write access is performed on the TWIHS_THR, it will generate a Transmit FIFO pointer error and set the TXFPTEF flag in TWIHS_FSR.

In Multiple Data mode, if the number of data written in the TWIHS_THR (according to the register access size) is bigger than the Transmit FIFO free space, it will generate a Transmit FIFO pointer error and set the TXFPTEF flag in TWIHS_FSR.

- Receive FIFO:

In Multiple Data mode, if the number of data read in the TWIHS_RHR (according to the register access size) is bigger than the number of unread data in the Receive FIFO, it will generate a Receive FIFO pointer error and set the RXFPTEF flag in TWIHS_FSR.

Pointer error should not happen if FIFO state is checked before writing/reading in TWIHS_THR/TWIHS_RHR. FIFO state can be checked either with TXRDY, RXRDY, TXFL or RXFL. When a pointer error occurs, other FIFO flags might not behave as expected; their state should be ignored.

If a Transmit or Receive pointer error occurs, a software reset must be performed using the SWRST bit in the TWIHS_CR. Note that issuing a software while transmitting might leave a slave in an unknown state holding the TWD line. In such case, a Bus Clear Command will allow to make the slave release the TWD line (the first frame sent afterwards might not be received properly by the slave).

- FIFO Thresholds

Each Transmit and Receive FIFO includes a threshold feature used to set a flag and an interrupt when a FIFO threshold is crossed. Thresholds are defined as a number of data in the FIFO, and the FIFO state (TXFL or RXFL) represents the number of data currently in the FIFO.

- Transmit FIFO:

The Transmit FIFO threshold can be set using the TXFTHRES field in TWIHS_FMR. Each time the Transmit FIFO goes from the ‘above threshold’ to the ‘equal or below threshold’ state, the TXFTHF flag in TWIHS_FSR is set. This enables the application to know that the Transmit FIFO reached the defined threshold and to refill it before it becomes empty.

- Receive FIFO:

The Receive FIFO threshold can be set using the RXFTHRES field in TWIHS_FMR. Each time the Receive FIFO goes from the ‘below threshold’ to the ‘equal or above threshold’ state, the RXFTHF flag in TWIHS_FSR is set. This enables the application to know that the Receive FIFO reached the defined threshold and to read some data before it becomes full.

47.10.9 USART Interrupt Enable Register (SPI_MODE)

Name: FLEX_US_IER (SPI_MODE)

Address: 0xF8034208 (0), 0xF8038208 (1), 0xFC010208 (2), 0xFC014208 (3), 0xFC018208 (4)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	CMP	–	–	NSSE	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	UNRE	TXEMPTY	–
7	6	5	4	3	2	1	0
–	–	OVRE	–	–	–	TXRDY	RXRDY

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Enables the corresponding interrupt.

RXRDY: RXRDY Interrupt Enable

TXRDY: TXRDY Interrupt Enable

OVRE: Overrun Error Interrupt Enable

TXEMPTY: TXEMPTY Interrupt Enable

UNRE: SPI Underrun Error Interrupt Enable

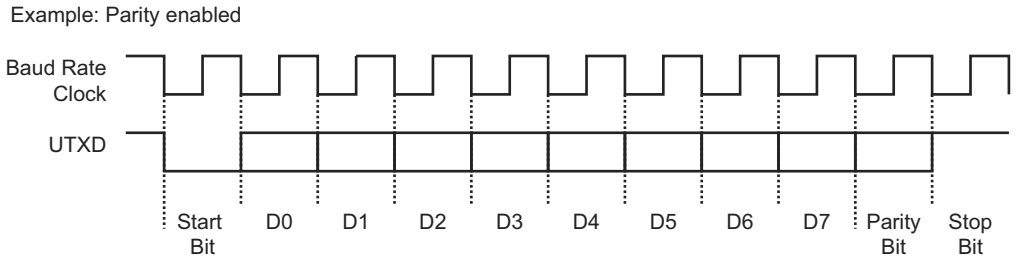
NSSE: NSS Line (Driving CTS Pin) Rising or Falling Edge Event

CMP: Comparison Interrupt Enable

48.5.3.2 Transmit Format

The UART transmitter drives the pin UTXD at the baud rate clock speed. The line is driven depending on the format defined in UART_MR and the data stored in the internal shift register. One start bit at level 0, then the 8 data bits, from the lowest to the highest bit, one optional parity bit and one stop bit at 1 are consecutively shifted out as shown in the following figure. The field PARE in UART_MR defines whether or not a parity bit is shifted out. When a parity bit is enabled, it can be selected between an odd parity, an even parity, or a fixed space or mark bit.

Figure 48-10: Character Transmission

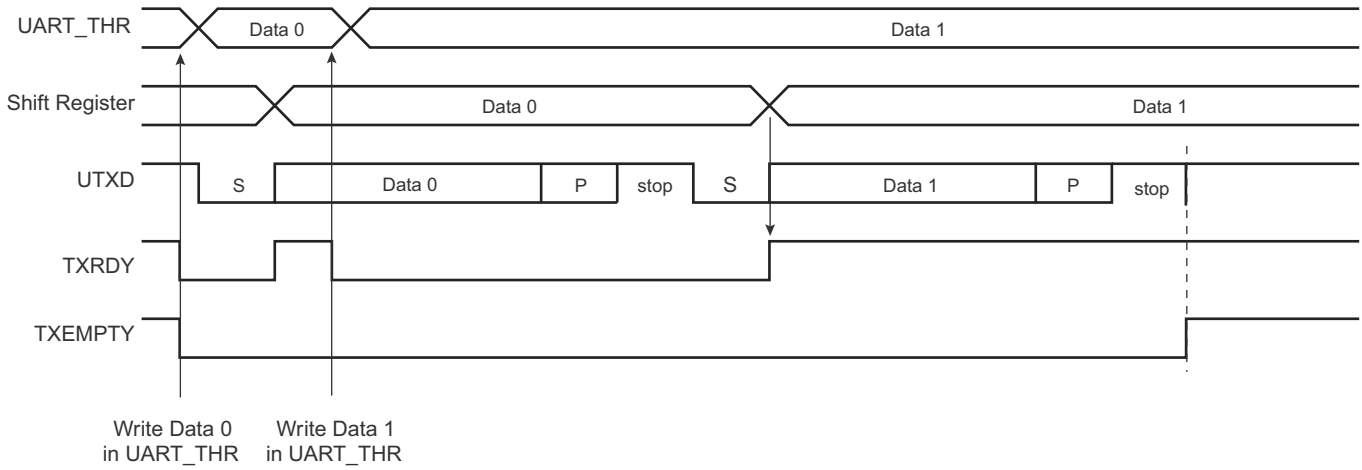


48.5.3.3 Transmitter Control

When the transmitter is enabled, the bit TXRDY (Transmitter Ready) is set in UART_SR. The transmission starts when the programmer writes in the UART_THR, and after the written character is transferred from UART_THR to the internal shift register. The TXRDY bit remains high until a second character is written in UART_THR. As soon as the first character is completed, the last character written in UART_THR is transferred into the internal shift register and TXRDY rises again, showing that the holding register is empty.

When both the internal shift register and UART_THR are empty, i.e., all the characters written in UART_THR have been processed, the TXEMPTY bit rises after the last stop bit has been completed.

Figure 48-11: Transmitter Control



48.5.4 DMA Support

Both the receiver and the transmitter of the UART are connected to a DMA Controller (DMAC) channel.

The DMA Controller channels are programmed via registers that are mapped within the DMAC user interface.

48.5.5 Comparison Function on Received Character

When a comparison is performed on a received character, the result of the comparison is reported on the CMP flag in UART_SR when UART_RHR is loaded with the new received character. The CMP flag is cleared by writing a one to the RSTSTA bit in UART_CR.

UART_CMPR (see Section 48.6.10 “UART Comparison Register”) can be programmed to provide different comparison methods. These are listed below:

- If VAL1 equals VAL2, then the comparison is performed on a single value and the flag is set to 1 if the received character equals

CMDIDX: Command Index Error

This bit is set to 1 if a Command Index error occurs in the command response.

This bit can only be set to 1 if SDMMC_EISTER.CMDIDX is set to 1. An interrupt can only be generated if SDMMC_EISIER.CMDIDX is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

DATTEO: Data Timeout Error

This bit is set to 1 when detecting one of following timeout conditions.

- Busy timeout for R1b, R5b response type (see “Physical Layer Simplified Specification V3.01” and “SDIO Simplified Specification V3.00”).
- Busy timeout after Write CRC status.
- Write CRC Status timeout.
- Read data timeout

This bit can only be set to 1 if SDMMC_EISTER.DATTEO is set to 1. An interrupt can only be generated if SDMMC_EISIER.DATTEO is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

DATCRC: Data CRC error

This bit is set to 1 when detecting a CRC error when transferring read data which uses the DAT line or when detecting that the Write CRC Status has a value other than “010”.

This bit can only be set to 1 if SDMMC_EISTER.DATCRC is set to 1. An interrupt can only be generated if SDMMC_EISIER.DATCRC is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

DATEND: Data End Bit Error

This bit is set to 1 either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status.

This bit can only be set to 1 if SDMMC_EISTER.DATEND is set to 1. An interrupt can only be generated if SDMMC_EISIER.DATEND is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

CURLIM: Current Limit Error

By setting SD Bus Power (SDBPWR) in SDMMC_PCR, the SDMMC is requested to supply power for the SD Bus. The SDMMC is protected from an illegal card by stopping power supply to the card, in which case this bit indicates a failure status. Reading 1 means the SDMMC is not supplying power to the card due to some failure. Reading 0 means that the SDMMC is supplying power and no error has occurred. The SDMMC may require some sampling time to detect the current limit.

This bit can only be set to 1 if SDMMC_EISTER.CURLIM is set to 1. An interrupt can only be generated if SDMMC_EISIER.CURLIM is set to 1.

Writing this bit to 1 clears this bit.

0: No error.

1: Error.

51.13.35 SDMMC Capabilities 1 Register

Name: SDMMC_CA1R

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
CLKMULT							
15	14	13	12	11	10	9	8
RTMOD		TSDR50	–	TCNTRT			
7	6	5	4	3	2	1	0
–	DRVDSUP	DRVCSUP	DRVASUP	–	DDR50SUP	SDR104SUP	SDR50SUP

Note: The Capabilities 1 Register is not supposed to be written by the user. However, the user can modify preset values only if Capabilities Write Enable (CAPWREN) is set to 1 in SDMMC_CACR.

SDR50SUP: SDR50 Support

0: SDR50 mode is not supported.

1: SDR50 mode is supported.

SDR104SUP: SDR104 Support

0: SDR104 mode is not supported.

1: SDR104 mode is supported.

DDR50SUP: DDR50 Support

0: DDR50 mode is not supported.

1: DDR50 mode is supported.

DRVASUP: Driver Type A Support

0: Driver type A is not supported.

1: Driver type A is supported.

DRVCSUP: Driver Type C Support

0: Driver type C is not supported.

1: Driver type C is supported.

DRVDSUP: Driver Type D Support

0: Driver type D is not supported.

1: Driver type D is supported.

TCNTRT: Timer Count For Retuning

This field indicates an initial value of the Retuning Timer for Retuning Mode (RTMOD) 1 to 3. Reading this field at 0 means that the Retuning Timer is disabled. The Retuning Timer initial value ranges from 0 to 1024 seconds.

$t_{TIMER} = 2^{(TCNTRT - 1)}$Seconds

TSDR50: Use Tuning for SDR50

If this bit is set to 1, the SDMMC requires tuning to operate SDR50 (tuning is always required to operate SDR104).

0: SDR50 does not require tuning.

1: SDR50 requires tuning.

51.13.55 SDMMC Retuning Status Slots Register

Name: SDMMC_RTSSR

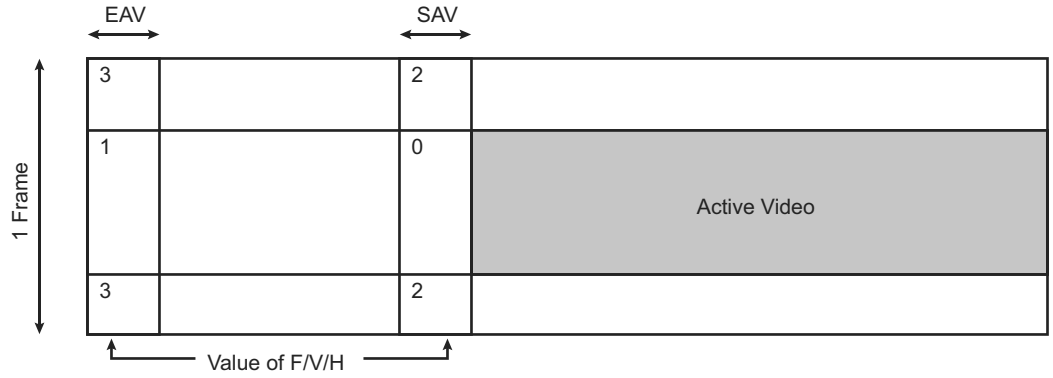
Access: Read-only

7	6	5	4	3	2	1	0
–	–	–	–	–	–	TEVTSLOT	

TEVTSLOT: Retuning Timer Event Slots

These status bits indicate the TEVT status for each SDMMC instance in the product (TEVTSLOT[x] corresponds to SDMMCx instance in the product).

Figure 52-13: Frame Timing Relationship for Progressive Systems



52.5.4 Parallel Interface External Sensor Connections

52.5.4.1 YCbCr, 10-bit CCIR656 with Embedded Synchronization

This mode is activated when fields ISC_PFE_CFG0.CCIR656 and ISC_PFE_CFG0.CCIR10_8N are both set.

Interface Bit	First Word	Second Word	Third Word	Fourth Word
isc_data[11](MSB)	1	0	0	1
isc_data[10]	1	0	0	F
isc_data[9]	1	0	0	V
isc_data[8]	1	0	0	H
isc_data[7]	1	0	0	P3
isc_data[6]	1	0	0	P2
isc_data[5]	1	0	0	P1
isc_data[4]	1	0	0	P0
isc_data[3]	1	0	0	0
isc_data[2]	1	0	0	0
isc_data[1]	not used	not used	not used	not used
isc_data[0]	not used	not used	not used	not used

52.5.4.2 YCbCr, 8-bit CCIR656 with Embedded Synchronization

This mode is activated when field ISC_PFE_CFG0.CCIR656 is set and field ISC_PFE_CFG0.CCIR10_8N is cleared.

Interface Bit	First Word	Second Word	Third Word	Fourth Word
isc_data[11](MSB)	1	0	0	1
isc_data[10]	1	0	0	F
isc_data[9]	1	0	0	V
isc_data[8]	1	0	0	H
isc_data[7]	1	0	0	P3
isc_data[6]	1	0	0	P2
isc_data[5]	1	0	0	P1
isc_data[4]	1	0	0	P0

52.6.43 ISC Contrast And Brightness, Brightness Register

Name: ISC_CBC_BRIGHT

Address: 0xF00083BC

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	BRIGHT		

7	6	5	4	3	2	1	0
BRIGHT							

BRIGHT: Brightness Control (signed 11 bits 1:10:0)

57.5 Secure Fuse Controller (SFC) User Interface

Table 57-1: Register Mapping

Offset	Register	Name	Access	Reset
0x00	SFC Key Register	SFC_KR	Write-only	–
0x04	SFC Mode Register	SFC_MR	Read/Write	0x0
0x08–0x0C	Reserved	–	–	–
0x10	SFC Interrupt Enable Register	SFC_IER	Write-only	–
0x14	SFC Interrupt Disable Register	SFC_IDR	Write-only	–
0x18	SFC Interrupt Mask Register	SFC_IMR	Read-only	0x0
0x1C	SFC Status Register	SFC_SR	Read-only	0x0
0x20	SFC Data Register 0	SFC_DR0	Read/Write	0x0
0x24	SFC Data Register 1	SFC_DR1	Read/Write	0x0
...	...	...	...	...
0x7C	SFC Data Register 23	SFC_DR23	Read/Write	0x0
0x80–0xFC	Reserved	–	–	–

Value	Name	Description
0x2	–	Reserved
0x3	–	Reserved
0x4	CTR	Counter mode (16-bit internal counter)

Values which are not listed in the table must be considered as “reserved”.

For CBC-MAC operating mode, configure OPMOD to 0x1 (CBC) and set LOD to 1.

Note: If the OPMODE field is set to 0x4 and AAHB = 1, there is no compliance with the standard CTR mode of operation.

LOD: Last Output Data Mode

0: No effect.

After each end of encryption/decryption, the output data will be available either on the output data registers (Manual and Auto modes).

In Manual and Auto modes, the AESB_ISR.DATRDY bit is cleared when at least one of the Output Data registers is read.

1: The AESB_ISR.DATRDY bit is cleared when at least one of the Input Data Registers is written.

No more Output Data Register reads are necessary between consecutive encryptions/decryptions (refer to Section 59.3.4 “Last Output Data Mode”).

CKEY: Key

Value	Name	Description
0xE	PASSWD	This field must be written with 0xE the first time that AESB_MR is programmed. For subsequent programming of the AESB_MR register, any value can be written, including that of 0xE.Always reads as 0.