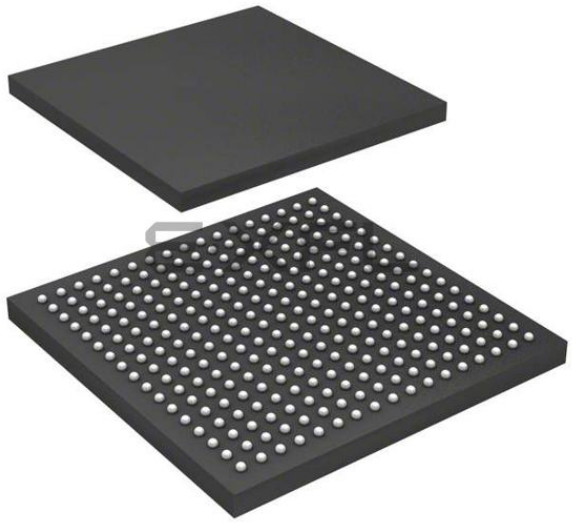


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26a-cn

26.5.6.2 UTC Mode

The update of the UTC time field must be synchronized on a second periodic event by either polling the RTC_SR.SEC status bit or by enabling the SECEN interrupt in the RTC_IER.

Once the second event occurs, the user must stop the RTC by setting the UPDTIM field in the Control Register (RTC_CR).

The ACKUPD bit must then be read to 1 by either polling the RTC_SR or by enabling the ACKUPD interrupt in the RTC_IER. Once ACKUPD is read to 1, it is mandatory to clear this flag by writing the corresponding bit in the RTC_SCCR, after which the user can write to the Time Register.

Once the update is finished, the user must write UPDTIM to 0 in the RTC_CR.

The timing sequence of the UTC time update is described in Figure 26-4 ”UTC Time Update Timing Diagram”.

In successive update operations, the user must wait for at least one second after resetting the UPDTIM bit in the RTC_CR before setting this bit again. This is done by waiting for the SEC flag in the RTC_SR before setting UPDTIM bit. After resetting UPDTIM, the SEC flag must also be cleared.

Figure 26-4: UTC Time Update Timing Diagram

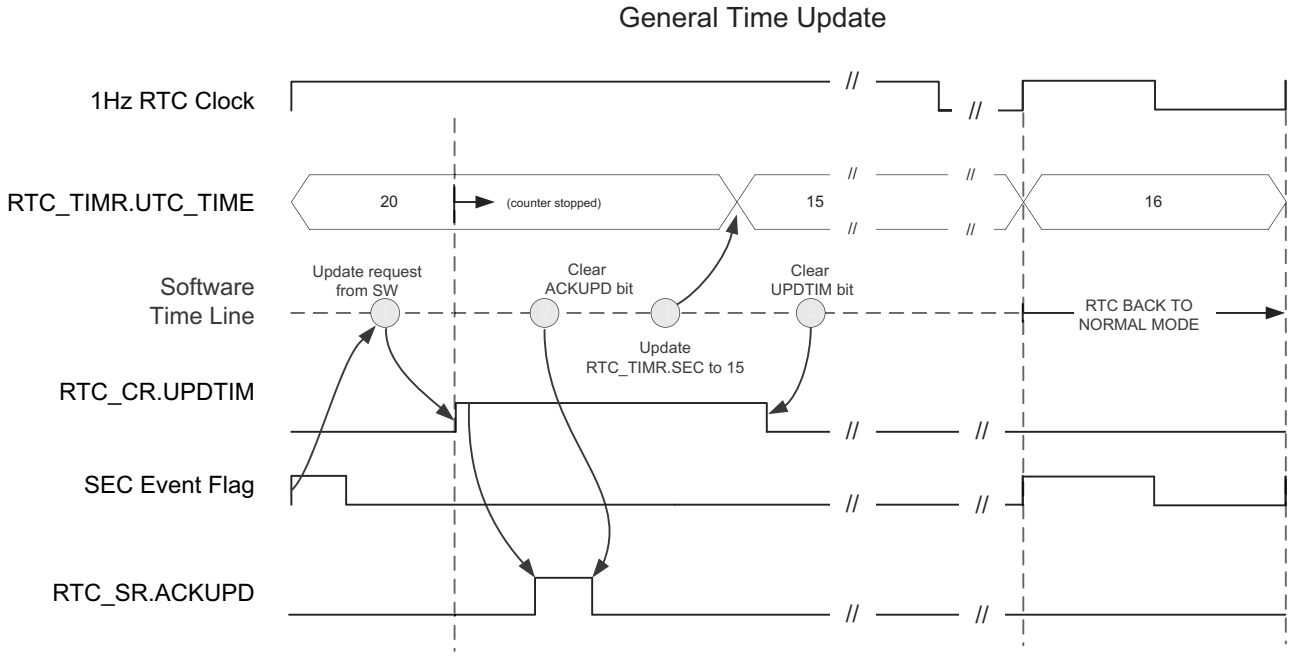
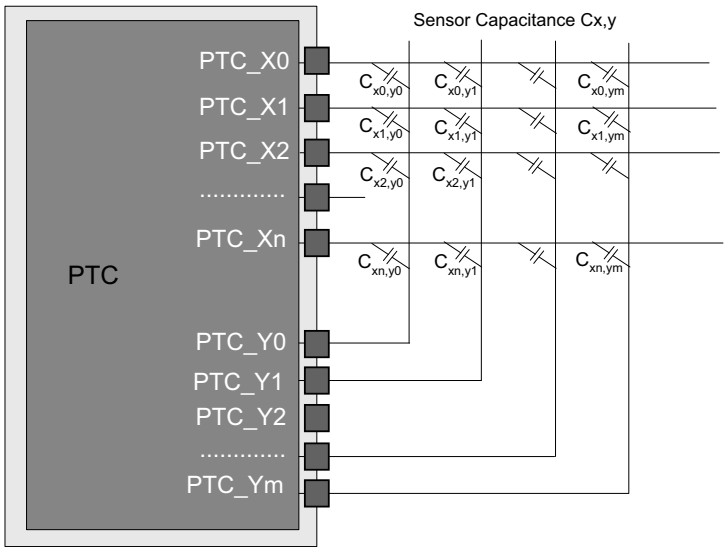


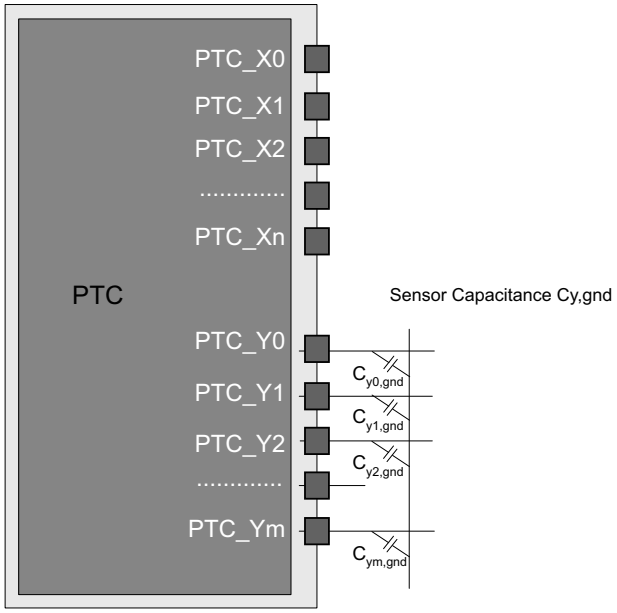
Figure 29-6: Mutual Capacitance Sensor Arrangement



29.6.6 Operations in Self-capacitance

The self-capacitance sensor is connected to a single pin on the PTC through the PTC_Ym electrodes to receive the signal. The sensor electrode capacitance is measured by the PTC.

Figure 29-7: Self-capacitance Sensor Arrangement



34.7 Parallel Input/Output Controller (PIO) User Interface

Each I/O line controlled by the PIO Controller is associated with a bit in each of the PIO Controller User Interface registers. Each register is 32 bits wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero.

Table 34-4: Register Mapping

Offset[3][4]	Register	Name	Access	Reset
0x000 + (io_group * 0x40) + 0x00	PIO Mask Register	PIO_MSKR	Read/Write	0x00000000
0x000 + (io_group * 0x40) + 0x04	PIO Configuration Register	PIO_CFGR	Read/Write	0x00000200
0x000 + (io_group * 0x40) + 0x08	PIO Pin Data Status Register	PIO_PDSR	Read-only	[1]
0x000 + (io_group * 0x40) + 0x0C	PIO Lock Status Register	PIO_LOCKSR	Read-only	0x00000000
0x000 + (io_group * 0x40) + 0x10	PIO Set Output Data Register	PIO_SODR	Write-only	–
0x000 + (io_group * 0x40) + 0x14	PIO Clear Output Data Register	PIO_CODR	Write-only	–
0x000 + (io_group * 0x40) + 0x18	PIO Output Data Status Register	PIO_ODSR	Read/Write	0x00000000
0x000 + (io_group * 0x40) + 0x1C	Reserved	–	–	–
0x000 + (io_group * 0x40) + 0x20	PIO Interrupt Enable Register	PIO_IER	Write-only	–
0x000 + (io_group * 0x40) + 0x24	PIO Interrupt Disable Register	PIO_IDR	Write-only	–
0x000 + (io_group * 0x40) + 0x28	PIO Interrupt Mask Register	PIO_IMR	Read-only	0x00000000
0x000 + (io_group * 0x40) + 0x2C	PIO Interrupt Status Register[2]	PIO_ISR	Read-only	0x00000000
0x000 + (io_group * 0x40) + 0x30	Reserved	–	–	–
0x000 + (io_group * 0x40) + 0x34	Reserved	–	–	–
0x000 + (io_group * 0x40) + 0x38	Reserved	–	–	–
0x000 + (io_group * 0x40) + 0x3C	PIO I/O Freeze Configuration Register	PIO_IOFR	Write-only	–
0x400–0x4FC	Reserved	–	–	–
0x500	Reserved	–	–	–
0x5D0	Reserved	–	–	–
0x5D4	Reserved	–	–	–
0x5E0	PIO Write Protection Mode Register	PIO_WPMR	Read/Write	0x00000000
0x5E4	PIO Write Protection Status Register	PIO_WPSR	Read-only	0x00000000
0x5E8–0x5FC	Reserved	–	–	–
0x1000 + (io_group * 0x40) + 0x00	Secure PIO Mask Register	S_PIO_MSKR	Read/Write	0x00000000

39.7.127 High-End Overlay Configuration Register 32

Name: LCDC_HEOCFG32

Address: 0xF000040C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
XPHI7COEFF4							

XPHI7COEFF4: Horizontal Coefficient for phase 7 tap 4

Coefficient format is 1 sign bit and 7 fractional bits.

39.7.141 Post Processing Interrupt Disable Register

Name: LCDC_PPIDR

Address: 0xF0000550

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	DONE	ADD	DSCR	DMA	–	–

DMA: End of DMA Transfer Interrupt Disable

0: No effect

1: Interrupt source is disabled

DSCR: Descriptor Loaded Interrupt Disable

0: No effect

1: Interrupt source is disabled

ADD: Head Descriptor Loaded Interrupt Disable

0: No effect

1: Interrupt source is disabled

DONE: End of List Interrupt Disable

0: No effect

1: Interrupt source is disabled

42.7.17 EHCI: REG04

Name: UHPHS_INSNREG04

Access: Read/Write

31	30	29	28	27	26	25	24
–							
23	22	21	20	19	18	17	16
–							
15	14	13	12	11	10	9	8
–							
7	6	5	4	3	2	1	0
–		EN_AutoFunc	NAK_RF	–	SDPE_TIME	HCCPARAMS_BW	HCSPARAMS_W

Bits [2:0] are used for debug purposes. Bits [(5+UHC2_N_PORTS):4] are functional bits where UHC2_N_PORTS indicates the number of physical USB ports.

HCSPARAMS_W: HCSPARAMS Write

When set, the HCSPARAMS register becomes writable. Upon system reset, this bit is 0.

HCCPARAMS_BW: HCCPARAMS Bits Write

When set, the HCCPARAMS register's bits 17, 15:4, and 2:0 become writable. Upon system reset, these bits are 0.

SDPE_TIME: Scales Down Port Enumeration Time

When set, Scales Down Port Enumeration Time is enabled. Reset value is 1’b0.

Note: This bit can be used for both RTL and Gate level simulations.

NAK_RF: NAK Reload Fix (Read/Write)

0: Enables this function.

1: Disables this function

Incorrect NAK reload transition at the end of a microframe for backward compatibility with Release 2.40c. For more information, see the *USB 2.0 Host-AHB Release Notes*. Reset value is 1’b0.

EN_AutoFunc: Enable Automatic Feature

0: Enables the automatic feature.

The Suspend signal is deasserted (logic level 1'b1) when run/stop is reset by software, but the hchalted bit is not set yet.

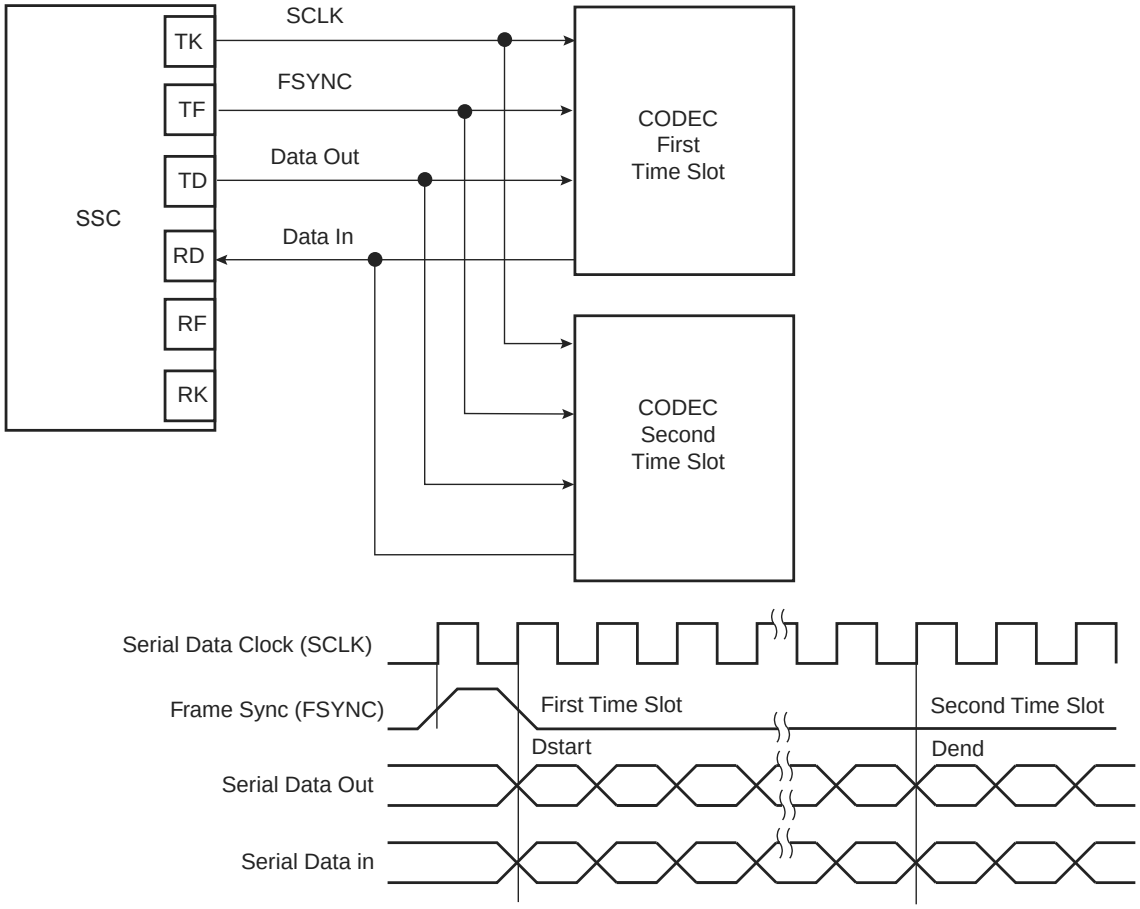
1: Disables the automatic feature, which takes all ports out of suspend when software clears the run/stop bit. This is for backward compatibility.

Bit [5] has an added functionality in release 2.80a and later. For systems where the host is halted without waking up all ports out of suspend, the port can remain suspended because the PHYCLK is not running when the halt is programmed. To avoid this, the DWC H20AHB host core automatically pulls ports out of suspend when the host is halted by software.

This bit is used to disable this automatic function.

Reset value is 0.

Figure 45-5: Time Slot Application Block Diagram



45.6 Pin Name List

Table 45-1: I/O Lines Description

Pin Name	Pin Description	Type
RF	Receive Frame Synchronization	Input/Output
RK	Receive Clock	Input/Output
RD	Receive Data	Input
TF	Transmit Frame Synchronization	Input/Output
TK	Transmit Clock	Input/Output
TD	Transmit Data	Output

START: Receive Start Selection

Value	Name	Description
0	CONTINUOUS	Continuous, as soon as the receiver is enabled, and immediately after the end of transfer of the previous data.
1	TRANSMIT	Transmit start
2	RF_LOW	Detection of a low level on RF signal
3	RF_HIGH	Detection of a high level on RF signal
4	RF_FALLING	Detection of a falling edge on RF signal
5	RF_RISING	Detection of a rising edge on RF signal
6	RF_LEVEL	Detection of any level change on RF signal
7	RF_EDGE	Detection of any edge on RF signal
8	CMP_0	Compare 0

STOP: Receive Stop Selection

0: After completion of a data transfer when starting with a Compare 0, the receiver stops the data transfer and waits for a new compare 0.

1: After starting a receive with a Compare 0, the receiver operates in a continuous mode until a Compare 1 is detected.

STTDLY: Receive Start Delay

If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the current start of reception. When the receiver is programmed to start synchronously with the transmitter, the delay is also applied.

Note: It is very important that STTDLY be set carefully. If STTDLY must be set, it should be done in relation to TAG (Receive Sync Data) reception.

PERIOD: Receive Period Divider Selection

This field selects the divider to apply to the selected Receive Clock in order to generate a new Frame Sync signal. If 0, no PERIOD signal is generated. If not 0, a PERIOD signal is generated each 2 x (PERIOD + 1) Receive Clock.

47.10.49 SPI Transmit Data Register (FIFO Multiple Data, 8- to 16-bit)

Name: FLEX_SPI_TDR (FIFO_MULTI_DATA)

Address: 0xF803440C (0), 0xF803840C (1), 0xFC01040C (2), 0xFC01440C (3), 0xFC01840C (4)

Access: Write-only

31	30	29	28	27	26	25	24
TD1							
23	22	21	20	19	18	17	16
TD1							
15	14	13	12	11	10	9	8
TD0							
7	6	5	4	3	2	1	0
TD0							

Note: If FIFO is enabled (FLEX_SPI_CR.FIFOEN) and FLEX_SPI_FMR.TXRDYM > 0, see Section 47.8.7.7 “SPI Multiple Data Mode” for details.

TDx: Transmit Data

Next data to write in the Transmit FIFO. Information to be transmitted must be written to this register in a right-justified format.

47.10.60 TWI Control Register

Name: FLEX_TWI_CR

Address: 0xF8034600 (0), 0xF8038600 (1), 0xFC010600 (2), 0xFC014600 (3), 0xFC018600 (4)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	FIFODIS	FIFOEN	–	LOCKCLR	–	THRCLR
23	22	21	20	19	18	17	16
–	–	–	–	–	–	ACMDIS	ACMEN
15	14	13	12	11	10	9	8
CLEAR	PECRQ	PECDIS	PECEN	SMBDIS	SMBEN	HSDIS	HSEN
7	6	5	4	3	2	1	0
SWRST	QUICK	SVDIS	SVEN	MSDIS	MSEN	STOP	START

START: Send a START Condition

0: No effect.

1: A frame beginning with a START bit is transmitted according to the features defined in the TWI Master Mode Register (FLEX_TWI_MMR).

This action is necessary when the TWI peripheral needs to read data from a slave. When configured in Master mode with a write operation, a frame is sent as soon as the user writes a character in the Transmit Holding Register (FLEX_TWI_THR).

STOP: Send a STOP Condition

0: No effect.

1: STOP condition is sent just after completing the current byte transmission in Master Read mode.

- In single data byte master read, both START and STOP must be set.
- In multiple data bytes master read, the STOP must be set after the last data received but one.
- In Master Read mode, if a NACK bit is received, the STOP is automatically performed.
- In master data write operation, a STOP condition will be sent after the transmission of the current data is finished.

MSEN: TWI Master Mode Enabled

0: No effect.

1: Enables the Master mode (MSDIS must be written to 0).

Note: Switching from Slave to Master mode is only permitted when TXCOMP = 1.

MSDIS: TWI Master Mode Disabled

0: No effect.

1: The Master mode is disabled, all pending data is transmitted. The shifter and holding characters (if it contains data) are transmitted in case of write operation. In read operation, the character being transferred must be completely received before disabling.

50.7.15 QSPI Write Protection Mode Register

Name: QSPI_WPMR

Address: 0xF00200E4 (0), 0xF00240E4 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
WPKEY							
23	22	21	20	19	18	17	16
WPKEY							
15	14	13	12	11	10	9	8
WPKEY							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPEN

WPEN: Write Protection Enable

0: Disables the write protection if WPKEY corresponds to 0x515350 (QSP in ASCII)

1: Enables the write protection if WPKEY corresponds to 0x515350 (QSP in ASCII)

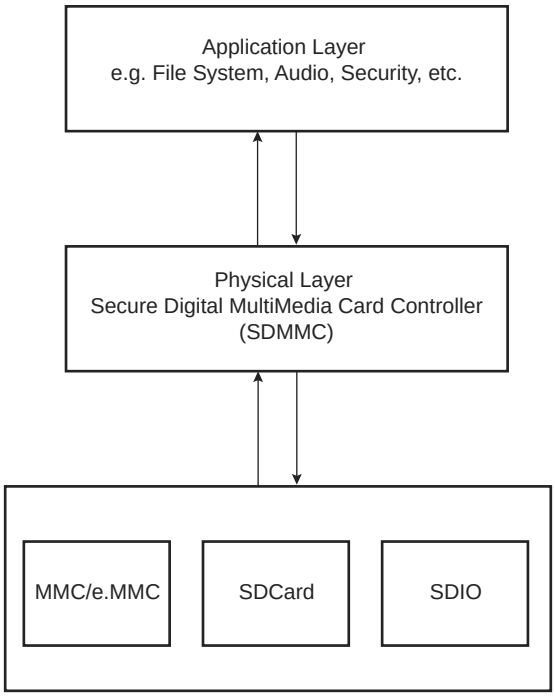
See Section 50.6.7 “Register Write Protection” for the list of registers that can be protected.

WPKEY: Write Protection Key

Value	Name	Description
0x515350	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

51.6 Application Block Diagram

Figure 51-2: Application Block Diagram



51.7 Pin Name List

Table 51-2: I/O Lines Description for 8-bit Configuration

Pin Name[1]	Pin Description	Type
SDMMC_CD	SDCard / SDIO / e.MMC Card Detect	Input
SDMMC_CMD	SDCard / SDIO / e.MMC Command/Response Line	I/O
SDMMC_WP	SDCard Connector Write Protect Signal	Input
SDMMC_RSTN	e.MMC Reset Signal	Output
SDMMC_1V8SEL	SDCard Signal Voltage Selection	Output
SDMMC_CK	SDCard / SDIO / e.MMC Clock Signal	Output
SDMMC_DAT[7..0]	SDCard / SDIO / e.MMC Data Lines	I/O

Note 1: When several SDMMCs are embedded in a product, SDMMC_CK refers to SDMMCx_CK, SDMMC_CMD to SDMMCx_CMD, SDMMC_DATy to SDMMCx_DATy, SDMMC_WP to SDMMCx_WP, SDMMC_1V8SEL to SDMMCx_1V8SEL, SDMMC_CD to SDMMCx_CD and SDMMC_RSTN to SDMMCx_RSTN.

51.13.16 SDMMC Clock Control Register

Name: SDMMC_CCR

Access: Read/Write

15	14	13	12	11	10	9	8
SDCLKFSEL							
7	6	5	4	3	2	1	0
USDCLKFSEL		CLKGSEL	–	–	SDCLKEN	INTCLKS	INTCLKEN

INTCLKEN: Internal Clock Enable

This bit is set to 0 when the SDMMC is not used or is awaiting a wakeup interrupt. In this case, its internal clock is stopped to reach a very low power state. Registers are still able to be read and written. The clock starts to oscillate when this bit is set to 1. Once the clock oscillation is stable, the SDMMC sets Internal Clock Stable (INTCLKS) in this register to 1.

This bit does not affect card detection.

0: The internal clock stops.

1: The internal clock oscillates.

INTCLKS: Internal Clock Stable

This bit is set to 1 when the SD clock is stable after setting SDMMC_CCR.INTCLKEN (Internal Clock Enable) to 1. The user must wait to set SD Clock Enable (SDCLKEN) until this bit is set to 1.

0: Internal clock not ready.

1: Internal clock ready.

SDCLKEN: SD Clock Enable

The SDMMC stops the SD Clock when writing this bit to 0. SDCLK Frequency Select (SDCLKFSEL) can be changed when this bit is 0. Then, the SDMMC maintains the same clock frequency until SDCLK is stopped (Stop at SDCLK = 0). If Card Inserted (CARDINS) in SDMMC_PSR is cleared, this bit is also cleared.

0: SD Clock disabled

1: SD Clock enabled

CLKGSEL: Clock Generator Select

This bit is used to select the clock generator mode in the SDCLK Frequency Select field. If the Programmable mode is not supported (SDMMC_CA1R.CLKMULT (Clock Multiplier) set to 0), then this bit cannot be written and is always read at 0.

This bit depends on the setting of Preset Value Enable (PVALEN) in SDMMC_HC2R.

If PVALEN = 0, this bit is set by the user.

If PVALEN = 1, this bit is automatically set to a value specified in one of the SDMMC_PVRx.

0: Divided Clock mode (BASECLK is used to generate SDCLK).

1: Programmable Clock mode (MULTCLK is used to generate SDCLK).

USDCLKFSEL: Upper Bits of SDCLK Frequency Select

These bits expand the SDCLK Frequency Select (SDCLKFSEL) to 10 bits. These two bits are assigned to bit 09-08 of the clock divider as described in SDCLKFSEL.

52.6.5 ISC Parallel Front End Configuration 1 Register

Name: ISC_PFE_CFG1

Address: 0xF0008010

Access: Read/Write

31	30	29	28	27	26	25	24
COLMAX							

23	22	21	20	19	18	17	16
COLMAX							

15	14	13	12	11	10	9	8
COLMIN							

7	6	5	4	3	2	1	0
COLMIN							

COLMIN: Column Minimum Limit

Horizontal starting position of the cropping area

COLMAX: Column Maximum Limit

Horizontal ending position of the cropping area

52.6.31 ISC Gamma Correction Blue Entry Register

Name: ISC_GAM_BENTRYx[x=0...63]

Address: 0xF0008098

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	BCONSTANT	

23	22	21	20	19	18	17	16
BCONSTANT							

15	14	13	12	11	10	9	8
–	–	–	–	–	–	BSLOPE	

7	6	5	4	3	2	1	0
BSLOPE							

BSLOPE: Blue Color Slope for Piecewise Interpolation (signed 10 bits 1:3:6)

BCONSTANT: Blue Color Constant for Piecewise Interpolation (unsigned 10 bits 0:10:0)

56.7.13 PWM Sync Channels Update Period Update Register

Name: PWM_SCUPUPD

Address: 0xF802C030

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	UPRUPD			

This register acts as a double buffer for the UPR value. This prevents an unexpected automatic trigger of the update of synchronous channels.

UPRUPD: Update Period Update

Defines the wanted time between each update of the synchronous channels if automatic trigger of the update is activated (UPDM = 1 or UPDM = 2 in PWM Sync Channels Mode Register). This time is equal to UPR+1 periods of the synchronous channels.

56.7.43 PWM Channel Period Register

Name: PWM_CPRDx [x=0..3]

Address: 0xF802C20C [0], 0xF802C22C [1], 0xF802C24C [2], 0xF802C26C [3]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
CPRD							

15	14	13	12	11	10	9	8
CPRD							

7	6	5	4	3	2	1	0
CPRD							

This register can only be written if bits WPSWS3 and WPHWS3 are cleared in the PWM Write Protection Status Register.

Only the first 16 bits (channel counter size) are significant.

CPRD: Channel Period

If the waveform is left-aligned, then the output waveform period depends on the channel counter source clock and can be calculated:

– By using the PWM peripheral clock divided by a given prescaler value “X” (where $X = 2^{PREA}$ is 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula is:

$$\frac{(X \times CPRD)}{f_{peripheral\ clock}}$$

– By using the PWM peripheral clock divided by a given prescaler value “X” (see above) and by either the DIVA or the DIVB divider. The formula becomes, respectively:

$$\frac{(X \times CPRD \times DIVA)}{f_{peripheral\ clock}} \ or \ \frac{(X \times CPRD \times DIVB)}{f_{peripheral\ clock}}$$

If the waveform is center-aligned, then the output waveform period depends on the channel counter source clock and can be calculated:

– By using the PWM peripheral clock divided by a given prescaler value “X” (where $X = 2^{PREA}$ is 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula is:

$$\frac{(2 \times X \times CPRD)}{f_{peripheral\ clock}}$$

– By using the PWM peripheral clock divided by a given prescaler value “X” (see above) and by either the DIVA or the DIVB divider. The formula becomes, respectively:

$$\frac{(2 \times X \times CPRD \times DIVA)}{f_{peripheral\ clock}} \ \text{or} \ \frac{(2 \times X \times CPRD \times DIVB)}{f_{peripheral\ clock}}$$

56.7.46 PWM Channel Dead Time Register

Name: PWM_DTx [x=0..3]

Address: 0xF802C218 [0], 0xF802C238 [1], 0xF802C258 [2], 0xF802C278 [3]

Access: Read/Write

31	30	29	28	27	26	25	24
DTL							

23	22	21	20	19	18	17	16
DTL							

15	14	13	12	11	10	9	8
DTH							

7	6	5	4	3	2	1	0
DTH							

This register can only be written if bits WPSWS4 and WPHWS4 are cleared in the PWM Write Protection Status Register.

Only the first 16 bits (dead-time counter size) of fields DTH and DTL are significant.

DTH: Dead-Time Value for PWMHx Output

Defines the dead-time value for PWMHx output. This value must be defined between 0 and the value (CPRD – CDTY) (PWM_CPRDx and PWM_CDTYx).

DTL: Dead-Time Value for PWMLx Output

Defines the dead-time value for PWMLx output. This value must be defined between 0 and CDTY (PWM_CDTYx).

60.5.18 AES Byte Counter Register

Name: AES_BCNT

Address: 0xF002C0B4

Access: Read/Write

31	30	29	28	27	26	25	24
BCNT							
23	22	21	20	19	18	17	16
BCNT							
15	14	13	12	11	10	9	8
BCNT							
7	6	5	4	3	2	1	0
BCNT							

BCNT: Auto Padding Byte Counter

Auto padding byte counter value. BCNT must be greater than 0.

Table 72-2: SAMA5D2 Datasheet DS60001476 Rev. A Revision History

Issue Date	Changes
Mar-2017	Section 40. “Ethernet MAC (GMAC)” Section 40.2 “Embedded Characteristics”: deleted queue sizes (now found in Table 40-6 “Queue Size”). Table 40.6.3.9 “Priority Queueing in the DMA”: added Table 40-6 “Queue Size” and updated queue sizes. Section 40.6.15 “Timestamp Unit”: changed pin reference from “TIOB11/PD22” to “TIOA11/PD21”. Added Section 40.6.18 “Energy-efficient Ethernet Support” Updated Section 40.6.19 “802.1Qav Support - Credit-based Shaping”: added definitions of portTransmitRate and IdleSlope; updated content on queue priority management. Added Section 40.6.20 “LPI Operation in the GMAC”. Table 40-18 “Register Mapping”: added registers at offsets 0x270 to 0x27C. Section 40.8.1 “GMAC Network Control Register”: added bit 19: TXLPIEN: Enable LPI Transmission (was ‘reserved’). Added bit description. Changed description of SRTSM bit. Section 40.8.3 “GMAC Network Status Register”: added bit 7: RXLPIS: LPI Indication (was ‘reserved’). Added bit description. Added bit 27: RXLPISBC: Receive LPI indication Status Bit Change and bit description and added bit 29: TSUTIMCOMP: TSU timer comparison interrupt and bit description in: - Section 40.8.10 “GMAC Interrupt Status Register” - Section 40.8.11 “GMAC Interrupt Enable Register” - Section 40.8.12 “GMAC Interrupt Disable Register” - Section 40.8.13 “GMAC Interrupt Mask Register” Section 40.8.13 “GMAC Interrupt Mask Register”: added bit 26, SRI, and bit 28, WOL, and bit descriptions. Added following sections: - Section 40.8.106 “GMAC Received LPI Transitions” - Section 40.8.107 “GMAC Received LPI Time” - Section 40.8.108 “GMAC Transmit LPI Transitions” - Section 40.8.109 “GMAC Transmit LPI Time” Section 40.8.115 “GMAC Credit-Based Shaping IdleSlope Register for Queue A” and Section 40.8.116 “GMAC Credit-Based Shaping IdleSlope Register for Queue B”: updated example for calculation of IdleSlope.
	Section 41. “USB High Speed Device Port (UDPHS)” Table 41-6 “Register Mapping”: offsets 0xD0 to 0xDC now ‘reserved’. Deleted internal registers: - UDPHS Test SOF Counter Register - UDPHS Test A Counter Register - UDPHS Test B Counter Register - UDPHS Test Mode Register
	Section 43. “Audio Class D Amplifier (CLASSD)” Section 43.6.6 “Application Schematics For Use Case Examples”: for Use Case 1, added information on external MOSFET selection.

cont’d on next page