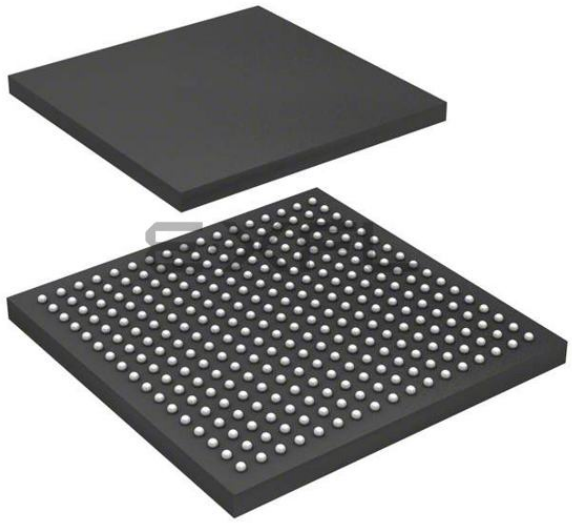

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26a-cnr

14.5.18 L2CC Invalidate Way Register

Name: L2CC_IWR

Address: 0x00A0077C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
WAY7	WAY6	WAY5	WAY4	WAY3	WAY2	WAY1	WAY0

WAYx: Invalidate Way Number x

0: The corresponding way is totally invalidated.

1: Invalidates the way. This bit is read as ‘1’ as long as invalidation of the way is in progress.

18. Matrix (H64MX/H32MX)

18.1 Description

In order to reduce power consumption without loss in performance, the system embeds three matrixes: one based on the AXI protocol (AXIMX) and two based on the AHB protocol (H64MX and H32MX). This section describes the implementation of the 64-bit AHB Matrix (H64MX) and the 32-bit AHB Matrix (H32MX).

For details on the matrix based on the AXI protocol, refer to Section 17. “AXI Matrix (AXIMX)”.

Each AHB Matrix implements a multilayer AHB, based on the AHB-Lite protocol, which enables parallel access paths between multiple AHB masters and slaves in a system, thus increasing the overall bandwidth. The normal latency to connect a master to a slave is one cycle, except for the default master of the accessed slave which is connected directly (zero cycle latency).

Note: When a master and a slave are on different bus matrixes (AXIMX, H64MX, or H32MX), both matrixes (H64MX and H32MX) and the bridge between the bus matrixes must be configured accordingly.

18.2 Embedded Characteristics

- 32-bit or 64-bit Data Bus
- 64-bit AHB Matrix (H64MX) Providing 12 Masters and 15 Slaves
- 32-bit AHB Matrix (H32MX) Providing 8 Masters and 6 Slaves
- One Address Decoder for Each Master
- Support for Long Bursts of Length 32, 64, 128 and Up to the Limit of 256-bit Burst Beats of Words
- Enhanced Programmable Mixed Arbitration for Each Slave:
  - Round-robin
  - Fixed priority
  - Latency quality of service
- Programmable Default Master for Each Slave:
  - No default master
  - Last accessed default master
  - Fixed default master
- Deterministic Maximum Access Latency for Masters
- Zero or One Cycle Arbitration Latency for the First Access of a Burst
- Bus Lock Forwarding to Slaves
- One Special Function Register for Each Slave (not dedicated)
- Register Write Protection
- ARM TrustZone Technology Extension to AHB and APB

20. Special Function Registers Backup (SFRBU)

20.1 Description

Special Function Registers Backup (SFRBU) manages specific aspects of the integrated memory, bridge implementations, processor and other functionality not controlled elsewhere.

20.2 Embedded Characteristics

- 32-bit Special Function Registers Backup controls specific behavior of the product.

24.7.3 Shutdown Status Register

Name: SHDW_SR

Address: 0xF8048018

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	WKUPIS9	WKUPIS8
23	22	21	20	19	18	17	16
WKUPIS7	WKUPIS6	WKUPIS5	WKUPIS4	WKUPIS3	WKUPIS2	WKUPIS1	WKUPIS0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXLPWK	ACCWK	RTCWK	–	–	–	–	WKUPS

WKUPS: PIOBU, WKUP Wakeup Status

0 (NO): No wakeup due to the assertion of the PIOBU, WKUP pins has occurred since the last read of SHDW_SR.

1 (PRESENT): At least one wakeup due to the assertion of the PIOBU, WKUP pins has occurred since the last read of SHDW_SR.

Note: WKUPIS1 reports the status of the Security Module event.

ACCWK: Analog Comparator Controller Wakeup

0: No wakeup alarm from the ACC occurred since the last read of SHDW_SR.

1: At least one wakeup alarm from the ACC occurred since the last read of SHDW_SR.

RXLPWK: Debug Unit Wakeup

0: No wakeup alarm from the Backup RX UART Comparison unit (RXLP) occurred since the last read of SHDW_SR.

1: At least one wakeup alarm from the Backup RX UART Comparison unit (RXLP) occurred since the last read of SHDW_SR.

WKUPIS0–WKUPIS9: Wakeup 0 to 9 Input Status

0 (DISABLE): The corresponding wakeup input is disabled, or was inactive at the time the debouncer triggered a wakeup event.

1 (ENABLE): The corresponding wakeup input was active at the time the debouncer triggered a wakeup event.

The value obtained must be rounded to the nearest integer prior to being programmed into CORRECTION field.

If HIGHPPM = 1, then the clock frequency correction range is from 30.5 ppm up to 1950 ppm. The RTC accuracy is less than 1 ppm for a range correction from 30.5 ppm up to 90 ppm.

The correction field must be programmed according to the required correction in ppm; the formula is as follows:

$$\text{CORRECTION} = \frac{3906}{\text{ppm}} - 1$$

The value obtained must be rounded to the nearest integer prior to be programmed into CORRECTION field.

If NEGPPM is set to 1, the ppm correction is negative (used to correct crystals that are faster than the nominal 32.768 kHz).

OUT0: All ADC Channel Trigger Event Source Selection

Value	Name	Description
0	NO_WAVE	No waveform, stuck at ‘0’
1	FREQ1HZ	1 Hz square wave
2	FREQ32HZ	32 Hz square wave
3	FREQ64HZ	64 Hz square wave
4	FREQ512HZ	512 Hz square wave
5	ALARM_TOGGLE	Output toggles when alarm flag rises
6	ALARM_FLAG	Output is a copy of the alarm flag
7	PROG_PULSE	Duty cycle programmable pulse

OUT1: ADC Last Channel Trigger Event Source Selection

Value	Name	Description
0	NO_WAVE	No waveform, stuck at ‘0’
1	FREQ1HZ	1 Hz square wave
2	FREQ32HZ	32 Hz square wave
3	FREQ64HZ	64 Hz square wave
4	FREQ512HZ	512 Hz square wave
5	ALARM_TOGGLE	Output toggles when alarm flag rises
6	ALARM_FLAG	Output is a copy of the alarm flag
7	PROG_PULSE	Duty cycle programmable pulse

THIGH: High Duration of the Output Pulse

Value	Name	Description
0	H_31MS	31.2 ms
1	H_16MS	15.6 ms
2	H_4MS	3.91 ms
3	H_976US	976 µs
4	H_488US	488 µs

34.7.4 PIO Lock Status Register

Name: PIO_LOCKSRx [x=0..3]

Address: 0xFC03800C [0], 0xFC03804C [1], 0xFC03808C [2], 0xFC0380CC [3]

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0–P31: Lock Status

0: The I/O line of the I/O group x is not locked.

1: The I/O line of the I/O group x is locked.

36.7.14 MPDDRC OCMS KEY1 Register

Name: MPDDRC_OCMS_KEY1

Address: 0xF000C03C

Access: Write once

31	30	29	28	27	26	25	24
KEY1							

23	22	21	20	19	18	17	16
KEY1							

15	14	13	12	11	10	9	8
KEY1							

7	6	5	4	3	2	1	0
KEY1							

This register can only be written if the WPEN bit is cleared in the MPDDRC Write Protection Mode Register.

KEY1: Off-chip Memory Scrambling (OCMS) Key Part 1

When Off-chip Memory Scrambling is enabled, the data scrambling depends on KEY1 and KEY2 values.

37.9 Connection to External Devices

37.9.1 Data Bus Width

A data bus width of 8 or 16 bits can be selected for each chip select. This option is controlled by the bit DBW in the SMC Mode Register (HSMC_MODE) for the corresponding chip select.

Figure 37-4 shows how to connect a 512 KB x 8-bit memory on NCS2. Figure 37-5 shows how to connect a 512 KB x 16-bit memory on NCS2.

Figure 37-4: Memory Connection for an 8-bit Data Bus

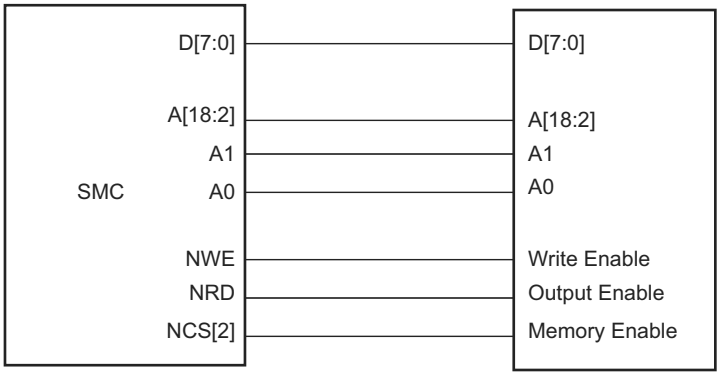
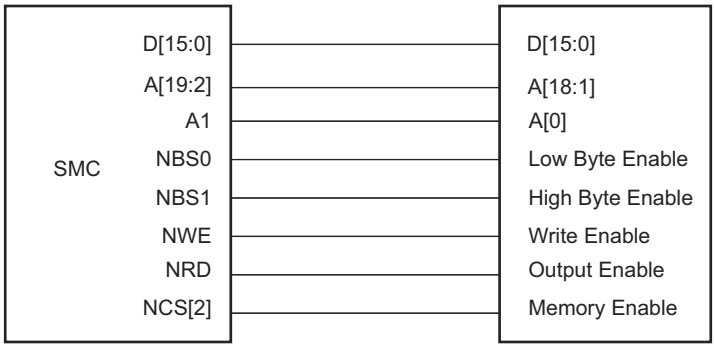


Figure 37-5: Memory Connection for a 16-bit Data Bus



37.9.2 Byte Write or Byte Select Access

Each chip select with a 16-bit data bus can operate with one of two different types of write access: Byte Write or Byte Select. This is controlled by the BAT bit of the HSMC_MODE register for the corresponding chip select.

37.9.2.1 Byte Write Access

Byte Write Access is used to connect 2 x 8-bit devices as a 16-bit memory, and supports one write signal per byte of the data bus and a single read signal.

Note that the SMC does not allow boot in Byte Write Access mode.

For 16-bit devices, the SMC provides NWR0 and NWR1 write signals for respectively Byte0 (lower byte) and Byte1 (upper byte) of a 16-bit bus. One single read signal (NRD) is provided.

37.9.2.2 Byte Select Access

Byte Select Access is used to connect one 16-bit device. In this mode, read/write operations can be enabled/disabled at Byte level. One Byte-select line per byte of the data bus is provided. One NRD and one NWE signal control read and write.

For 16-bit devices, the SMC provides NBS0 and NBS1 selection signals for respectively Byte0 (lower byte) and Byte1 (upper byte) of a 16-bit bus.

40.8.79 GMAC 1519 to Maximum Byte Frames Received Register

Name: GMAC_TMXBFR

Address: 0xF8008180

Access: Read-only

31	30	29	28	27	26	25	24
NFRX							

23	22	21	20	19	18	17	16
NFRX							

15	14	13	12	11	10	9	8
NFRX							

7	6	5	4	3	2	1	0
NFRX							

NFRX: 1519 to Maximum Byte Frames Received without Error

This register counts the number of 1519 byte or above frames successfully received without error. Maximum frame size is determined by the Network Configuration Register bit 8 (1536 maximum frame size) or bit 3 (jumbo frame size). Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory. See Section 40.8.2 ”GMAC Network Configuration Register”.

40.8.118 GMAC Screening Type 2 Register x Priority Queue

Name: GMAC_ST2RPQx[x=0..7]

Address: 0xF8008540

Access: Read/Write

31	30	29	28	27	26	25	24
–	COMPCE	COMPC					COMPBE

23	22	21	20	19	18	17	16
COMPB					COMPAE	COMPA	

15	14	13	12	11	10	9	8
COMPA			ETHE	I2ETH			VLANE

7	6	5	4	3	2	1	0
–	VLANP			–	QNB		

Screening type 2 registers are used to allocate up to 3 priority queues to received frames based on the VLAN priority field of received ethernet frames.

QNB: Queue Number (0–2)

If a match is successful, then the queue value programmed in QNB is allocated to the frame.

VLANP: VLAN Priority

When VLAN match enable is set (bit 8), the VLAN priority field of the received frame is matched against bits 7:4 of this register.

VLANE: VLAN Enable

0: VLAN match is disabled.

1: VLAN match is enabled.

I2ETH: Index of Screening Type 2 EtherType register x

When ETHE is set (bit 12), the field EtherType (last EtherType in the header if the frame is VLAN tagged) is compared with bits 15:0 in the register designated by the value of I2ETH.

ETHE: EtherType Enable

0: EtherType match with bits 15:0 in the register designated by the value of I2ETH is disabled.

1: EtherType match with bits 15:0 in the register designated by the value of I2ETH is enabled.

COMPA: Index of Screening Type 2 Compare Word 0/Word 1 register x

COMPA is a pointer to the compare registers GMAC_ST2CW0x and GMAC_ST2CW1x. When COMPAE is set, the compare is true if the data at the frame offset ANDed with the value MASKVAL is equal to the value of COMPVAL ANDed with the value of MASKVAL.

COMPAE: Compare A Enable

0: Comparison via the register designated by index COMPA is disabled.

1: Comparison via the register designated by index COMPA is enabled.

41. USB High Speed Device Port (UDPHS)

41.1 Description

The USB High Speed Device Port (UDPHS) is compliant with the Universal Serial Bus (USB), rev 2.0 High Speed device specification.

Each endpoint can be configured in one of several USB transfer types. It can be associated with one, two or three banks of a Dual-port RAM used to store the current data payload. If two or three banks are used, one DPR bank is read or written by the processor, while the other is read or written by the USB device peripheral. This feature is mandatory for isochronous endpoints.

41.2 Embedded Characteristics

- 1 High-speed Device
- 1 UTMI Transceiver shared between Host and Device
- USB v2.0 High Speed (480 Mbits/s) Compliant
- 16 Endpoints up to 1024 bytes
- Embedded Dual-port RAM for Endpoints
- Suspend/Resume Logic (Command of UTMI)
- Up to Three Memory Banks for Endpoints (Not for Control Endpoint)
- 8 Kbytes of DPRAM

41.7.7 UDPHS Test Register

Name: UDPHS_TST

Address: 0xFC02C0E0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	OPMODE2	TST_PKT	TST_K	TST_J	SPEED_CFG	

SPEED_CFG: Speed Configuration

Value	Name	Description
0	NORMAL	Normal mode: The macro is in Full Speed mode, ready to make a High Speed identification, if the host supports it and then to automatically switch to High Speed mode.
1	–	Reserved
2	HIGH_SPEED	Force High Speed: Set this value to force the hardware to work in High Speed mode. Only for debug or test purpose.
3	FULL_SPEED	Force Full Speed: Set this value to force the hardware to work only in Full Speed mode. In this configuration, the macro will not respond to a High Speed reset handshake.

TST_J: Test J Mode

0: No effect.

1: Set to send the J state on the UDPHS line. This enables the testing of the high output drive level on the D+ line.

TST_K: Test K Mode

0: No effect.

1: Set to send the K state on the UDPHS line. This enables the testing of the high output drive level on the D- line.

TST_PKT: Test Packet Mode

0: No effect.

1: Set to repetitively transmit the packet stored in the current bank. This enables the testing of rise and fall times, eye patterns, jitter, and any other dynamic waveform specifications.

OPMODE2: OpMode2

0: No effect.

1: Set to force the OpMode signal (UTMI interface) to “10”, to disable the bit-stuffing and the NRZI encoding.

Note: For the Test mode, Test_SE0_NAK (refer to Universal Serial Bus Specification, Revision 2.0: 7.1.20, Test Mode Support). Force the device in High Speed mode, and configure a bulk-type endpoint. Do not fill this endpoint for sending NAK to the host. Upon command, a port’s transceiver must enter the High Speed Receive mode and remain in that mode until the exit action is taken. This enables the testing of output impedance, low level output voltage and loading characteristics. In addition, while in this mode, upstream facing ports (and only upstream facing ports) must respond to any IN token packet with a NAK handshake (only if the packet CRC is determined to be correct) within the normal allowed device response time. This enables testing of the device squelch level circuitry and, additionally, provides a general purpose stimulus/response test for basic functional testing.

47.10.35 USART FIFO Mode Register

Name: FLEX_US_FMR

Address: 0xF80342A0 (0), 0xF80382A0 (1), 0xFC0102A0 (2), 0xFC0142A0 (3), 0xFC0182A0 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	RXFTHRES2					
23	22	21	20	19	18	17	16
–	–	RXFTHRES					
15	14	13	12	11	10	9	8
–	–	TXFTHRES					
7	6	5	4	3	2	1	0
FRTSC	–	RXRDYM		–	–	TXRDYM	

TXRDYM: Transmitter Ready Mode

If FIFOs are enabled, the FLEX_US_CSR.TXRDY flag behaves as follows.

Value	Name	Description
0	ONE_DATA	TXRDY will be at level ‘1’ when at least one data can be written in the Transmit FIFO
1	TWO_DATA	TXRDY will be at level ‘1’ when at least two data can be written in the Transmit FIFO
2	FOUR_DATA	TXRDY will be at level ‘1’ when at least four data can be written in the Transmit FIFO

RXRDYM: Receiver Ready Mode

If FIFOs are enabled, the FLEX_US_CSR.RXRDY flag behaves as follows.

Value	Name	Description
0	ONE_DATA	RXRDY will be at level ‘1’ when at least one unread data is in the Receive FIFO
1	TWO_DATA	RXRDY will be at level ‘1’ when at least two unread data are in the Receive FIFO
2	FOUR_DATA	RXRDY will be at level ‘1’ when at least four unread data are in the Receive FIFO

FRTSC: FIFO RTS Pin Control enable (Hardware Handshaking mode only)

0: RTS pin is not controlled by Receive FIFO thresholds.

1: RTS pin is controlled by Receive FIFO thresholds.

See Section 47.7.3.15 ”Hardware Handshaking” for details.

TXFTHRES: Transmit FIFO Threshold

0–32: Defines the Transmit FIFO threshold value (number of data). The FLEX_US_FESR.TXFTHF flag will be set when Transmit FIFO goes from “above” threshold state to “equal or below” threshold state.

RXFTHRES: Receive FIFO Threshold

0–32: Defines the Receive FIFO threshold value (number of data). The FLEX_US_FESR.RXFTHF flag will be set when Receive FIFO goes from “below” threshold state to “equal to or above” threshold state.

RXFTHRES2: Receive FIFO Threshold 2

0–32: Defines the Receive FIFO threshold 2 value (number of data). The FLEX_US_FESR.RXFTHF2 flag will be set when Receive FIFO goes from “above” threshold state to “equal or below” threshold state.

Figure 48-3: Start Bit Detection

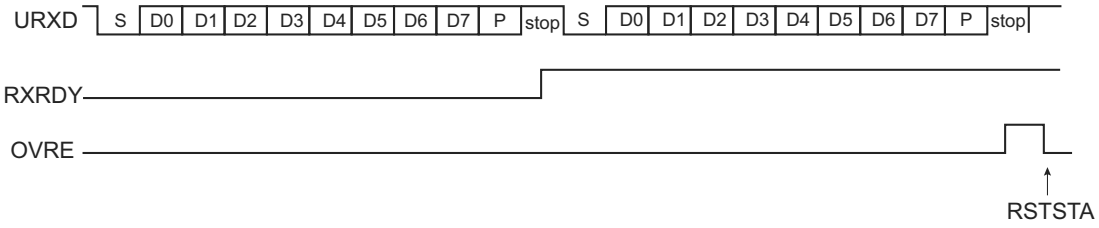
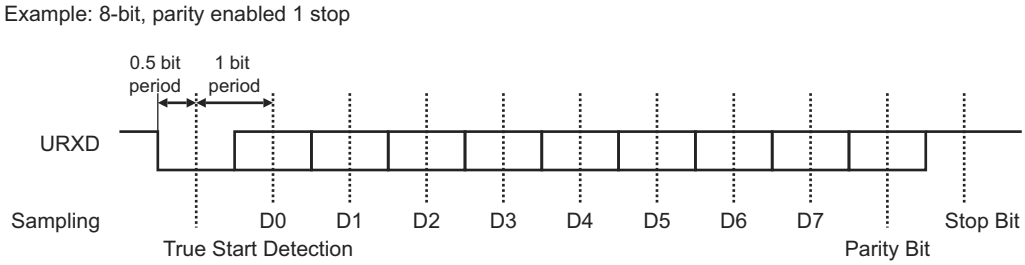


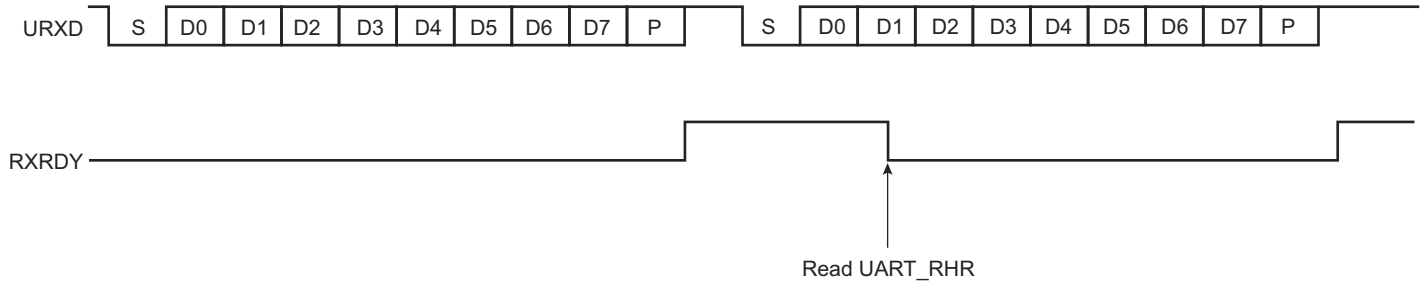
Figure 48-4: Character Reception



48.5.2.3 Receiver Ready

When a complete character is received, it is transferred to the Receive Holding Register (UART_RHR) and the RXRDY status bit in the Status Register (UART_SR) is set. The bit RXRDY is automatically cleared when UART_RHR is read.

Figure 48-5: Receiver Ready



48.5.2.4 Receiver Overrun

The OVRE status bit in UART_SR is set if UART_RHR has not been read by the software (or the DMA Controller) since the last transfer, the RXRDY bit is still set and a new character is received. OVRE is cleared when the software writes a 1 to the bit RSTSTA (Reset Status) in UART_CR.

Figure 48-6: Receiver Overrun

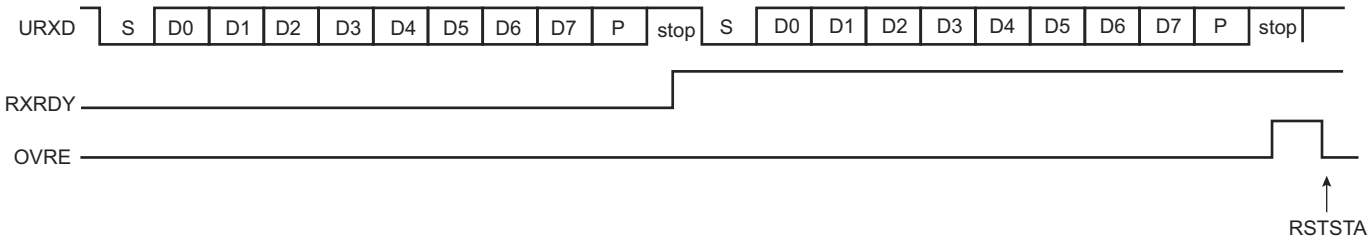
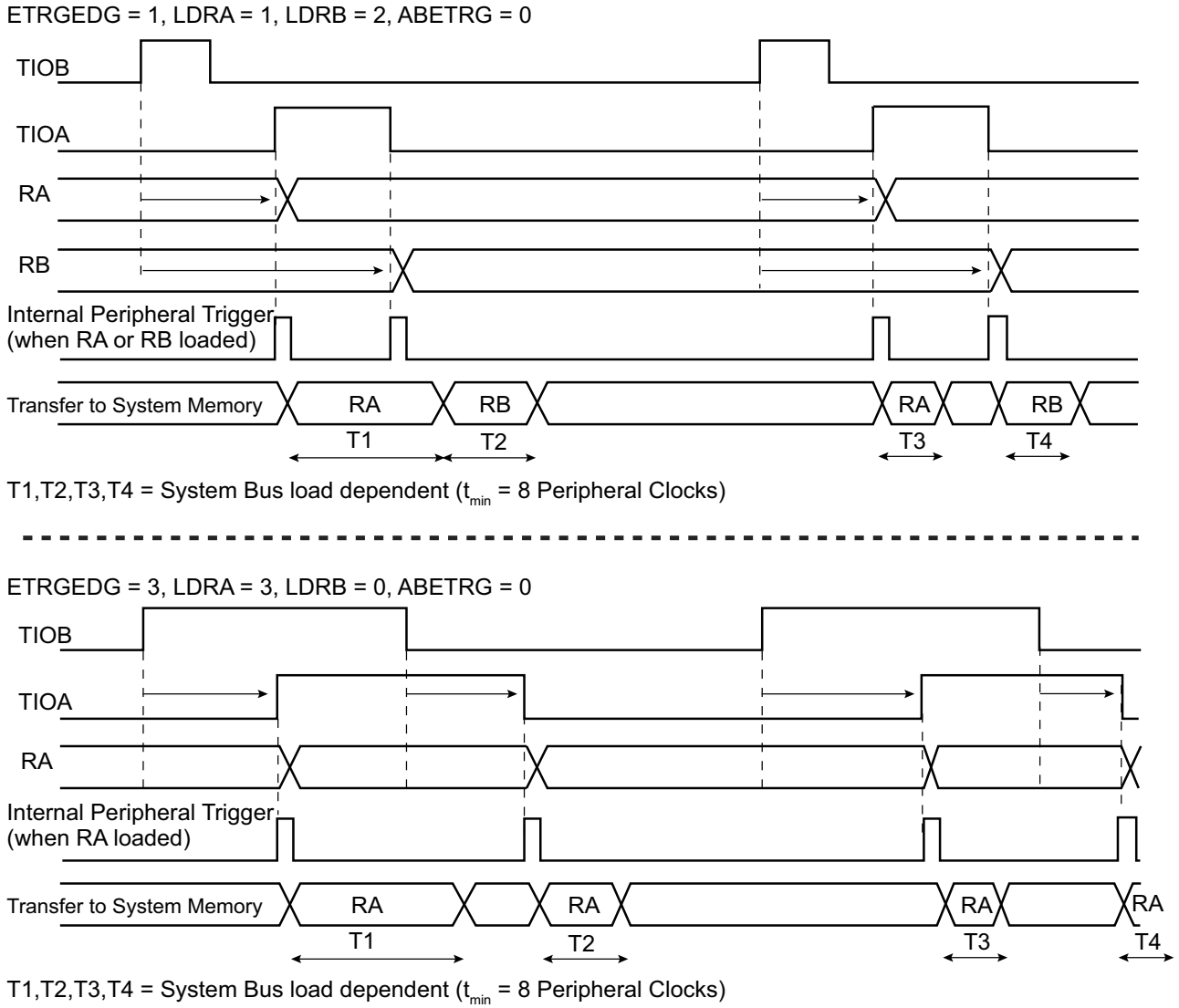


Figure 54-5: Example of Transfer with DMAC in Capture Mode



54.6.10 Trigger Conditions

In addition to the SYNC signal, the software trigger and the RC compare trigger, an external trigger can be defined.

TC_CMRx.ABETRG selects TIOAx or TIOBx input signal as an external trigger or the trigger signal from the output comparator of the PWM module. The External Trigger Edge Selection parameter (TC_CMR.ETRGEDG) defines the edge (rising, falling, or both) detected to generate an external trigger. If TC_CMRx.ETRGEDG = 0 (none), the external trigger is disabled.

56.7.8 PWM Interrupt Status Register 1

Name: PWM_ISR1

Address: 0xF802C01C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	FCHID3	FCHID2	FCHID1	FCHID0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

CHIDx: Counter Event on Channel x

0: No new counter event has occurred since the last read of PWM_ISR1.

1: At least one counter event has occurred since the last read of PWM_ISR1.

FCHIDx: Fault Protection Trigger on Channel x

0: No new trigger of the fault protection since the last read of PWM_ISR1.

1: At least one trigger of the fault protection since the last read of PWM_ISR1.

Note: Reading PWM_ISR1 automatically clears CHIDx and FCHIDx flags.

60.5.3 AES Interrupt Enable Register

Name: AES_IER

Address: 0xF002C010

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	PLENERR	EOPAD	TAGRDY
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	URAD
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

DATRDY: Data Ready Interrupt Enable

URAD: Unspecified Register Access Detection Interrupt Enable

TAGRDY: GCM Tag Ready Interrupt Enable

EOPAD: End of Padding Interrupt Enable

PLENERR: Padding Length Error Interrupt Enable

61.5.7 SHA Message Size Register

Name: SHA_MSR

Address: 0xF0028020

Access: Read/Write

31	30	29	28	27	26	25	24
MSGSIZE							

23	22	21	20	19	18	17	16
MSGSIZE							

15	14	13	12	11	10	9	8
MSGSIZE							

7	6	5	4	3	2	1	0
MSGSIZE							

MSGSIZE: Message Size

The size in bytes of the message. When MSGSIZE differs from 0, the SHA appends the corresponding value converted in bits after the padding section, as described in the FIPS180-2 specification.

To disable automatic padding, MSGSIZE field must be written to 0.

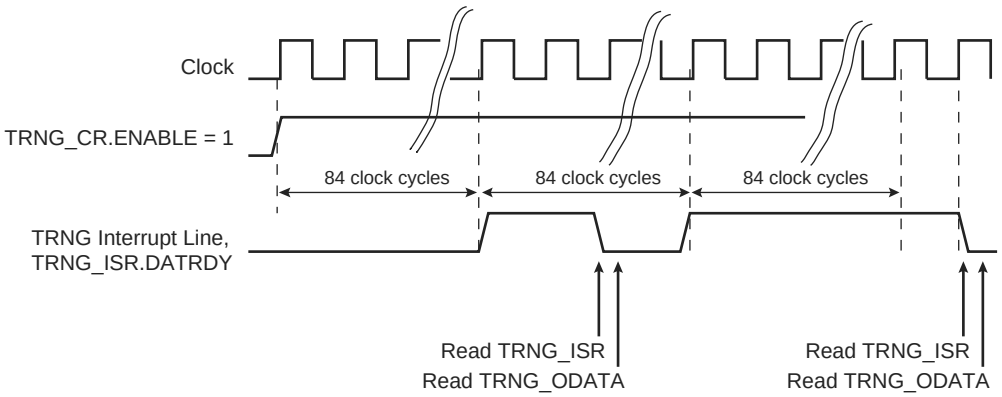
63.5 Functional Description

As soon as the TRNG is enabled in the Control register (TRNG_CR), the generator provides one 32-bit random value every 84 clock cycles.

The TRNG interrupt line can be enabled in the Interrupt Enable register (TRNG_IER), and disabled in the Interrupt Disable register (TRNG_IDR). This interrupt is set when a new random value is available and the interrupt is cleared when the Status register (TRNG_ISR) is read. The flag TRNG_ISR.DATRDY is set when the random data is ready to be read out on the 32-bit Output Data register (TRNG_ODATA).

The normal operating mode checks that the TRNG_ISR.DATRDY flag equals '1' before reading TRNG_ODATA when a 32-bit random value is required by the software application.

Figure 63-2: TRNG Data Generation Sequence



If JTAG IOSET 4 is selected by the user as JTAG debug port in the Boot Configuration Word, and if the ROM Code boots, or tries to boot, on any of the external memory interfaces stated above, the JTAG clock pin (TCK) is reset at its default mode (PIO) at the end of the ROM Code execution.

This occurs as soon as EXT_MEM_BOOT_ENABLE is set.

Workaround: Do not select, or disable, external memory boot interface SDMMC1, SPI1 IOSET 2 or QSPI0 IOSET 3. However, if using one of these boot interfaces is required, reconfigure the PA22 pin in JTAG TCK IOSET 4 mode in the bootstrap or application.

71.3 Errata - SAMA5D2 MRL A Parts

This section describes errata relevant to the devices listed in Table 71-3.

Table 71-3: SAMA5D2 MRL A Parts

Device Name
ATSAMA5D22A
ATSAMA5D24A
ATSAMA5D27A
ATSAMA5D28A

71.3.1 GMAC Timestamps and PTP packets

Issue: Issue: Bad association of timestamps and the PTP packets

An issue in the association mechanism between event registers and queued PTP packets may lead to timestamps incorrectly associated with these packets.

Even if it is highly unlikely to queue consecutive packets of the same type, there is no way to know to which frame the content of the PTP event registers refers.

Workaround: None

71.3.2 ROM Code: Main External Clock Frequency Support for SAM-BA Monitor

Issue: ROM code v1.1 supports ONLY a 12 and 16 MHz external clock frequency to allow USB connection to be used for SAM-BA Monitor

Workaround: None

71.3.3 ROM Code: Watchdog after SAM-BA Monitor Connection

Issue: Watchdog reset occurs when reenabling the watchdog

When no bootable program is found in an external memory, the Watchdog is disabled just before the ROM Code runs SAM-BA Monitor. The ROM code sets the Watchdog Timer Mode register (WDT_MR) to the value 0x00008000 and then clears the counter value. If a program loaded and executed using the SAM-BA Monitor Go command reenables the watchdog, a watchdog reset is immediately executed whatever the value of the watchdog counter.