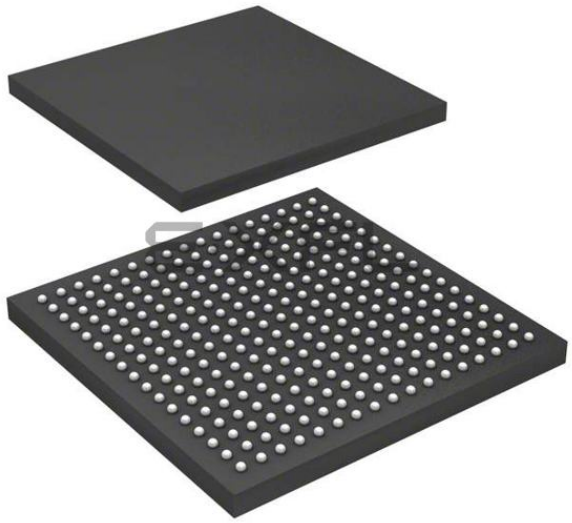

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26a-cu

13. ARM Cortex-A5

13.1 Description

The ARM Cortex-A5 processor is a high-performance, low-power, ARM macrocell with an L1 cache subsystem that provides full virtual memory capabilities. The Cortex-A5 processor implements the ARMv7 architecture and runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java™ byte codes in Jazelle® state.

The Cortex-A5 NEON Media Processing Engine (MPE) extends the Cortex-A5 functionality to provide support for the ARM v7 Advanced SIMD v2 and *Vector Floating-Point v4* (VFPv4) instruction sets. The Cortex-A5 NEON MPE provides flexible and powerful acceleration for signal processing algorithms including multimedia such as image processing, video decode/encode, 2D/3D graphics, and audio. See the *Cortex-A5 NEON Media Processing Engine Technical Reference Manual*.

The Cortex-A5 processor includes TrustZone® technology to enhance security by partitioning the SoC's hardware and software resources in a Secure world for the security subsystem and a Normal world for the rest, enabling a strong security perimeter to be built between the two. See *Security Extensions overview* in the *Cortex-A5 Technical Reference Manual*. See the *ARM Architecture Reference Manual* for details on how TrustZone works in the architecture.

Note: All ARM publications referenced in this datasheet can be found at www.arm.com.

13.1.1 Power Management

The Cortex-A5 design supports the following main levels of power management:

- Run Mode
- Standby Mode

13.1.1.1 Run Mode

Run mode is the normal mode of operation where all of the processor functionality is available. Everything, including core logic and embedded RAM arrays, is clocked and powered up.

13.1.1.2 Standby Mode

Standby mode disables most of the clocks of the processor, while keeping it powered up. This reduces the power drawn to the static leakage current, plus a small clock power overhead required to enable the processor to wake up from Standby mode. The transition from Standby mode to Run mode is caused by one of the following:

- the arrival of an interrupt, either masked or unmasked
- the arrival of an event, if standby mode was initiated by a Wait for Event (WFE) instruction
- a debug request, when either debug is enabled or disabled
- a reset.

30.6.2 RXLP Mode Register

Name: RXLP_MR

Address: 0xF8049004

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	PAR			–
7	6	5	4	3	2	1	0
–	–	–	FILTER	–	–	–	–

FILTER: Receiver Digital Filter

Value	Name	Description
0	DISABLED	RXLP does not filter the receive line.
1	ENABLED	RXLP filters the receive line using a three-sample filter (16x-bit clock) (2 over 3 majority).

PAR: Parity Type

Value	Name	Description
0	EVEN	Even Parity
1	ODD	Odd Parity
2	SPACE	Parity forced to 0
3	MARK	Parity forced to 1
4	NO	No parity

34.7.10 PIO Interrupt Mask Register

Name: PIO_IMRx [x=0..3]

Address: 0xFC038028 [0], 0xFC038068 [1], 0xFC0380A8 [2], 0xFC0380E8 [3]

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0–P31: Input Change Interrupt Mask

0: Input Change interrupt is disabled on the I/O line of the I/O group x.

1: Input Change interrupt is enabled on the I/O line of the I/O group x.

39.7.54 Overlay 1 Configuration Register 9

Name: LCDC_OVR1CFG9

Address: 0xF0000190

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
GA							

15	14	13	12	11	10	9	8
–	–	–	–	–	DSTKEY	REP	DMA

7	6	5	4	3	2	1	0
OVR	LAEN	GAEN	REVALPHA	ITER	ITER2BL	INV	CRKEY

CRKEY: Blender Chroma Key Enable

0: Chroma key matching is disabled.

1: Chroma key matching is enabled.

INV: Blender Inverted Blender Output Enable

0: Iterated pixel is the blended pixel.

1: Iterated pixel is the inverted pixel.

ITER2BL: Blender Iterated Color Enable

0: Final adder stage operand is set to 0.

1: Final adder stage operand is set to the iterated pixel value.

ITER: Blender Use Iterated Color

0: Pixel difference is set to 0.

1: Pixel difference is set to the iterated pixel value.

REVALPHA: Blender Reverse Alpha

0: Pixel difference is multiplied by alpha.

1: Pixel difference is multiplied by 1 - alpha.

GAEN: Blender Global Alpha Enable

0: Global alpha blending coefficient is disabled.

1: Global alpha blending coefficient is enabled.

LAEN: Blender Local Alpha Enable

0: Local alpha blending coefficient is disabled.

1: Local alpha blending coefficient is enabled.

OVR: Blender Overlay Layer Enable

0: Overlay pixel color is set to the default overlay pixel color.

1: Overlay pixel color is set to the DMA channel pixel color.

DMA: Blender DMA Layer Enable

0: The default color is used on the Overlay 1 Layer.

1: The DMA channel retrieves the pixels stream from the memory.

39.7.105 High-End Overlay Configuration Register 10

Name: LCDC_HEOCFG10

Address: 0xF00003B4

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
RKEY							

15	14	13	12	11	10	9	8
GKEY							

7	6	5	4	3	2	1	0
BKEY							

RKEY: Red Color Component Chroma Key

Reference Red chroma key used to match the Red color of the current overlay.

GKEY: Green Color Component Chroma Key

Reference Green chroma key used to match the Green color of the current overlay.

BKEY: Blue Color Component Chroma Key

Reference Blue chroma key used to match the Blue color of the current overlay.

39.7.107 High-End Overlay Configuration Register 12

Name: LCDC_HEOCFG12

Address: 0xF00003BC

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
GA							

15	14	13	12	11	10	9	8
–	–	–	VIDPRI	–	DSTKEY	REP	DMA

7	6	5	4	3	2	1	0
OVR	LAEN	GAEN	REVALPHA	ITER	ITER2BL	INV	CRKEY

CRKEY: Blender Chroma Key Enable

0: Chroma key matching is disabled.

1: Chroma key matching is enabled.

INV: Blender Inverted Blender Output Enable

0: Iterated pixel is the blended pixel.

1: Iterated pixel is the inverted pixel.

ITER2BL: Blender Iterated Color Enable

0: Final adder stage operand is set to 0.

1: Final adder stage operand is set to the iterated pixel value.

ITER: Blender Use Iterated Color

0: Pixel difference is set to 0.

1: Pixel difference is set to the iterated pixel value.

REVALPHA: Blender Reverse Alpha

0: Pixel difference is multiplied by alpha.

1: Pixel difference is multiplied by 1 - alpha.

GAEN: Blender Global Alpha Enable

0: Global alpha blending coefficient is disabled.

1: Global alpha blending coefficient is enabled.

LAEN: Blender Local Alpha Enable

0: Local alpha blending coefficient is disabled.

1: Local alpha blending coefficient is enabled.

OVR: Blender Overlay Layer Enable

0: Overlay pixel color is set to the default overlay pixel color.

1: Overlay pixel color is set to the DMA channel pixel color.

DMA: Blender DMA Layer Enable

0: The default color is used on the Overlay 1 Layer.

1: The DMA channel retrieves the pixels stream from the memory.

TXPBMS: Transmitter Packet Buffer Memory Size Select

Having this bit at zero halves the amount of memory used for the transmit packet buffer. This reduces the amount of memory used by the GMAC. It is important to set this bit to one if the full configured physical memory is available. The value in brackets below represents the size that would result for the default maximum configured memory size of 4 Kbytes.

0: Do not use top address bit (2 Kbytes).

1: Use full configured addressable space (4 Kbytes).

TXCOEN: Transmitter Checksum Generation Offload Enable

Transmitter IP, TCP and UDP checksum generation offload enable. When set, the transmitter checksum generation engine is enabled to calculate and substitute checksums for transmit frames. When clear, frame data is unaffected.

DRBS: DMA Receive Buffer Size

DMA receive buffer size in AHB system memory. The value defined by these bits determines the size of buffer to use in main AHB system memory when writing received data.

The value is defined in multiples of 64 bytes, thus a value of 0x01 corresponds to buffers of 64 bytes, 0x02 corresponds to 128 bytes etc.

For example:

– 0x02: 128 bytes

– 0x18: 1536 bytes (1 × max length frame/buffer)

– 0xA0: 10240 bytes (1 × 10K jumbo frame/buffer)

Note that this value should never be written as zero.

DDRP: DMA Discard Receive Packets

When set, the GMAC DMA will automatically discard receive packets from the receiver packet buffer memory when no AHB resource is available.

When low, the received packets will remain to be stored in the SRAM based packet buffer until AHB buffer resource next becomes available.

A write to this bit is ignored if the DMA is not configured in the packet buffer full store and forward mode.

40.8.10 GMAC Interrupt Status Register

Name: GMAC_ISR

Address: 0xF8008024

Access: Read-only

31	30	29	28	27	26	25	24
–	–	TSUTIMCOMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
23	22	21	20	19	18	17	16
PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR	–	–
15	14	13	12	11	10	9	8
–	PFTR	PTZ	PFNZ	HRESP	ROVR	–	–
7	6	5	4	3	2	1	0
TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS

This register indicates the source of the interrupt. In order that the bits of this register read 1, the corresponding interrupt source must be enabled in the mask register. If any bit is set in this register, the GMAC interrupt signal will be asserted in the system.

MFS: Management Frame Sent

The PHY Maintenance Register has completed its operation. Cleared on read.

RCOMP: Receive Complete

A frame has been stored in memory. Cleared on read.

RXUBR: RX Used Bit Read

Set when a receive buffer descriptor is read with its used bit set. Cleared on read.

TXUBR: TX Used Bit Read

Set when a transmit buffer descriptor is read with its used bit set. Cleared on read.

TUR: Transmit Underrun

This interrupt is set if the transmitter was forced to terminate a frame that it has already began transmitting due to further data being unavailable.

This interrupt is set if a transmitter status write back has not completed when another status write back is attempted.

This interrupt is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB not OK response was returned, or because the used bit was read.

RLEX: Retry Limit Exceeded

Transmit error. Cleared on read.

TFC: Transmit Frame Corruption Due to AHB Error

Transmit frame corruption due to AHB error. Set if an error occurs while midway through reading transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame.

TCOMP: Transmit Complete

Set when a frame has been transmitted. Cleared on read.

ROVR: Receive Overrun

Set when the receive overrun status bit is set. Cleared on read.

HRESP: HRESP Not OK

Set when the DMA block sees HRESP not OK. Cleared on read.

PFNZ: Pause Frame with Non-zero Pause Quantum Received

40.8.53 GMAC 64 Byte Frames Transmitted Register

Name: GMAC_BFT64

Address: 0xF8008118

Access: Read-only

31	30	29	28	27	26	25	24
NFTX							

23	22	21	20	19	18	17	16
NFTX							

15	14	13	12	11	10	9	8
NFTX							

7	6	5	4	3	2	1	0
NFTX							

NFTX: 64 Byte Frames Transmitted without Error

This register counts the number of 64 byte frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

42.7.14 EHCI: REG01 - Programmable Packet Buffer OUT/IN Thresholds

Name: UHPHS_INSNREG01

Access: Read/Write

31	30	29	28	27	26	25	24
Out_Threshold							
23	22	21	20	19	18	17	16
Out_Threshold							
15	14	13	12	11	10	9	8
In_Threshold							
7	6	5	4	3	2	1	0
In_Threshold							

Programmable Packet Buffer OUT/IN thresholds (in CONFIG1 mode only, not applicable in Config2 mode).

The value specified here is the number of DWORDs (32-bit entries).

In_Threshold: Amount of Data Available in the IN Packet Buffer

The IN threshold is used to start the memory transfer as soon as the IN threshold amount of data is available in the Packet Buffer. It is also used to disconnect the data write, if the threshold amount of data is not available in the Packet Buffer.

Out_Threshold: Amount of Data Available in the OUT Packet Buffer

The OUT threshold is used to start the USB transfer as soon as the OUT threshold amount of data is fetched from system memory. It is also used to disconnect the data fetch, if the threshold amount of space is not available in the Packet Buffer.

The minimum OUT and IN threshold amount that can be programmed through INSN registers is 16 bytes.

For INCRX configurations, the minimum threshold amount that can be programmed is the highest possible INCRX burst value. For example, if the value of the strap signals {ss_ena_incr16_i, ss_ena_incr8_i, ss_ena_incr4_i} is 3'b011 (for example, INCR16 burst is disabled, INCR8/INCR4 bursts are enabled), then the minimum OUT and IN threshold values should be 32 bytes (8 DWords).

OUT and IN threshold values can be equal to the packet buffer depth only when one of the following conditions is met:

- The packet buffer depth is equal to 512 bytes and isochronous/interrupt transactions are not initiated by the host controller.
- The packet buffer depth is equal to 1024 bytes.

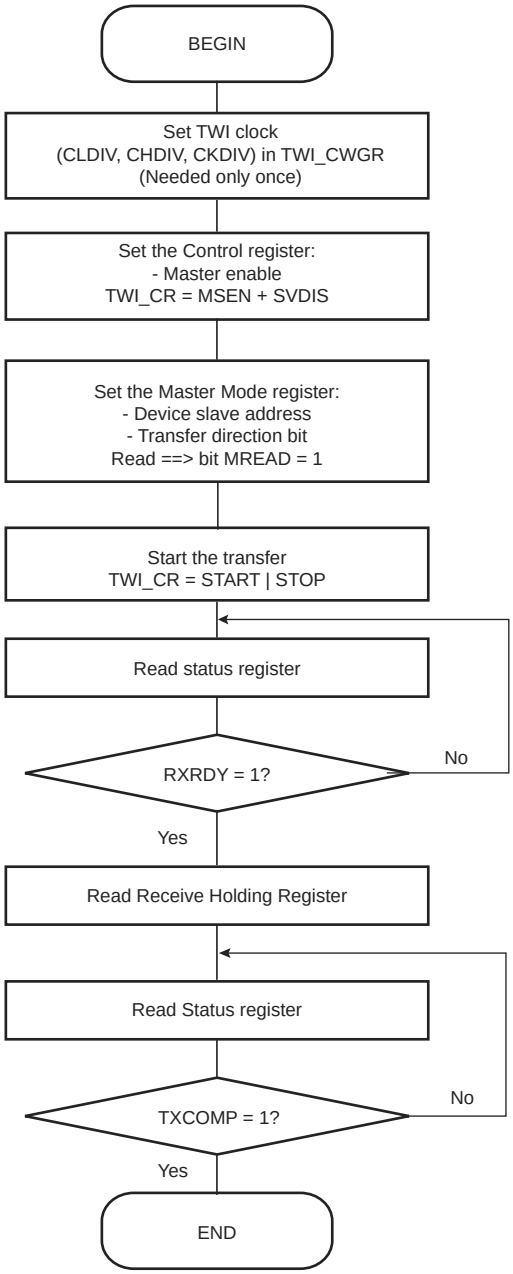
The threshold default value depends on one of the following packet buffer configurations:

- 1024 bytes depth, 256 bytes IN and OUT thresholds
- 512 bytes depth, 128 bytes IN and OUT thresholds
- 256 bytes depth, 64 bytes IN and OUT thresholds
- 128 bytes depth, 64 bytes IN and OUT thresholds
- 64 bytes depth, 60 bytes IN and OUT thresholds

For INCRX configurations, the Break Memory Transfer bit is always enabled.

Depending on the different packet buffer settings, not all MSB bits are used.

Figure 46-21: TWIHS Read Operation with Single Data Byte without Internal Address



46.7.25 TWIHS FIFO Interrupt Mask Register

Name: TWIHS_FIMR

Address: 0xF802806C (0), 0xFC02806C (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXFPTEF	TXFPTEF	RXFTHF	RXFFF	RXFEF	TXFTHF	TXFFF	TXFEF

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

TXFEF: TXFEF Interrupt Mask

TXFFF: TXFFF Interrupt Mask

TXFTHF: TXFTHF Interrupt Mask

RXFEF: RXFEF Interrupt Mask

RXFFF: RXFFF Interrupt Mask

RXFTHF: RXFTHF Interrupt Mask

TXFPTEF: TXFPTEF Interrupt Mask

RXFPTEF: RXFPTEF Interrupt Mask

Table 47-18: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x630	TWI Receive Holding Register	FLEX_TWI_RHR	Read-only	0x00000000
0x634	TWI Transmit Holding Register	FLEX_TWI_THR	Write-only	–
0x638	TWI SMBus Timing Register	FLEX_TWI_SMBTR	Read/Write	0x00000000
0x63C	Reserved	–	–	–
0x640	TWI Alternative Command Register	FLEX_TWI_ACR	Read/Write	0x0
0x644	TWI Filter Register	FLEX_TWI_FILTR	Read/Write	0x00000000
0x648	Reserved	–	–	–
0x64C	TWI SleepWalking Matching Register	FLEX_TWI_SWMR	Read/Write	0x00000000
0x650	TWI FIFO Mode Register	FLEX_TWI_FMR	Read/Write	0x0
0x654	TWI FIFO Level Register	FLEX_TWI_FLR	Read-only	0x0
0x658–0x65C	Reserved	–	–	–
0x660	TWI FIFO Status Register	FLEX_TWI_FSR	Read-only	0x0
0x664	TWI FIFO Interrupt Enable Register	FLEX_TWI_FIER	Write-only	–
0x668	TWI FIFO Interrupt Disable Register	FLEX_TWI_FIDR	Write-only	–
0x66C	TWI FIFO Interrupt Mask Register	FLEX_TWI_FIMR	Read-only	0x0
0x670–0x6CC	Reserved	–	–	–
0x6D0	Reserved	–	–	–
0x6D4–0x6E0	Reserved	–	–	–
0x6E4	TWI Write Protection Mode Register	FLEX_TWI_WPMR	Read/Write	0x00000000
0x6E8	TWI Write Protection Status Register	FLEX_TWI_WPSR	Read-only	0x00000000
0x6EC–0x6FC	Reserved	–	–	–
0x700–0x7FC	Reserved	–	–	–

Note 1: Write is possible only in LIN master node configuration.

ACMDIS: Alternative Command Mode Disable

0: No effect.

1: Alternative Command mode disabled.

THRCLR: Transmit Holding Register Clear

0: No effect.

1: Clear the Transmit Holding Register and set TXRDY, TXCOMP flags.

LOCKCLR: Lock Clear

0: No effect.

1: Clear the TWI FSM lock.

FIFOEN: FIFO Enable

0: No effect.

1: Enable the Transmit and Receive FIFOs

FIFODIS: FIFO Disable

0: No effect.

1: Disable the Transmit and Receive FIFOs

50.7.1 QSPI Control Register

Name: QSPI_CR

Address: 0xF0020000 (0), 0xF0024000 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	LASTXFER
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	–	–	QSPIDIS	QSPIEN

QSPIEN: QSPI Enable

0: No effect.

1: Enables the QSPI to transfer and receive data.

QSPIDIS: QSPI Disable

0: No effect.

1: Disables the QSPI.

As soon as QSPIDIS is set, the QSPI finishes its transfer.

All pins are set in Input mode and no data is received or transmitted.

If a transfer is in progress, the transfer is finished before the QSPI is disabled.

If both QSPIEN and QSPIDIS are equal to one when QSPI_CR is written, the QSPI is disabled.

SWRST: QSPI Software Reset

0: No effect.

1: Reset the QSPI. A software-triggered hardware reset of the QSPI interface is performed.

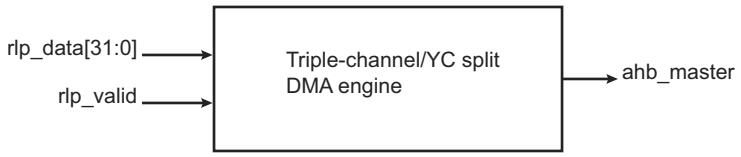
DMA channels are not affected by software reset.

LASTXFER: Last Transfer

0: No effect.

1: The chip select is deasserted after the character written in QSPI_TDR.TD has been transferred.

Figure 52-34: DMA Engine Block Diagram



ISC_DCFG.IMODE	DMA Engine Input Data
PACKED8	rlp_data[7:0]
PACKED16	rlp_data[15:0]
PACKED32	rlp_data[31:0]
YC422SP	rlp_data[31:0]
YC422P	rlp_data[31:0]
YC420SP	rlp_data[31:0]
YC420P	rlp_data[31:0]

When a bus error is detected, an interrupt flag is set. If the error occurs on a write operation, ISC_INTSR.WERR is asserted. If the error occurs on a read operation, ISC_INTSR.RERR is asserted. The ISC_INTSR.WERRID field gives details on the first error channel identifier.

52.5.15.1 Descriptor Memory Address Mapping

ISC_DCFG.IMODE	ISC_DAD0.AD0	ISC_DAD1.AD1	ISC_DAD2.AD2
PACKED8, PACKED16, PACKED32	data address	not used	not used
YC422SP	Y address	CbCr address	not used
YC422P	Y address	Cb address	Cr address
YC420SP	Y address	CbCr address	not used
YC420P	Y address	Cb address	Cr address

52.5.15.2 Descriptor Memory Mapping

Three descriptor views are available. Descriptor view 0 is used when the pixel or data stream is packed. Descriptor view 1 is used for YCbCr semi-planar pixel stream. Descriptor view 2 is used for YCbCr planar pixel stream.

Table 52-5: ISC_DCTRL.DVIEW = 0

Address	Register
ISC_DNDA+0x00	ISC_DCTRL
ISC_DNDA+0x04	ISC_DNDA
ISC_DNDA+0x08	ISC_DAD0
ISC_DNDA+0x0C	ISC_DST0

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the MCAN's transmit output CANTX through the transceiver to the receive input CANRX plus the transmitter delay compensation offset as configured by MCAN_TDCR.TDCO. The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (e.g. half of the bit time in the data phase). The position of the secondary sample point is rounded down to the next integer number of CAN core clock periods.

MCAN_PSR.TDCV shows the actual transmitter delay compensation value. MCAN_PSR.TDCV is cleared when MCAN_CCCR.INIT is set and is updated at each transmission of an FD frame while MCAN_DBTP.TDC is set.

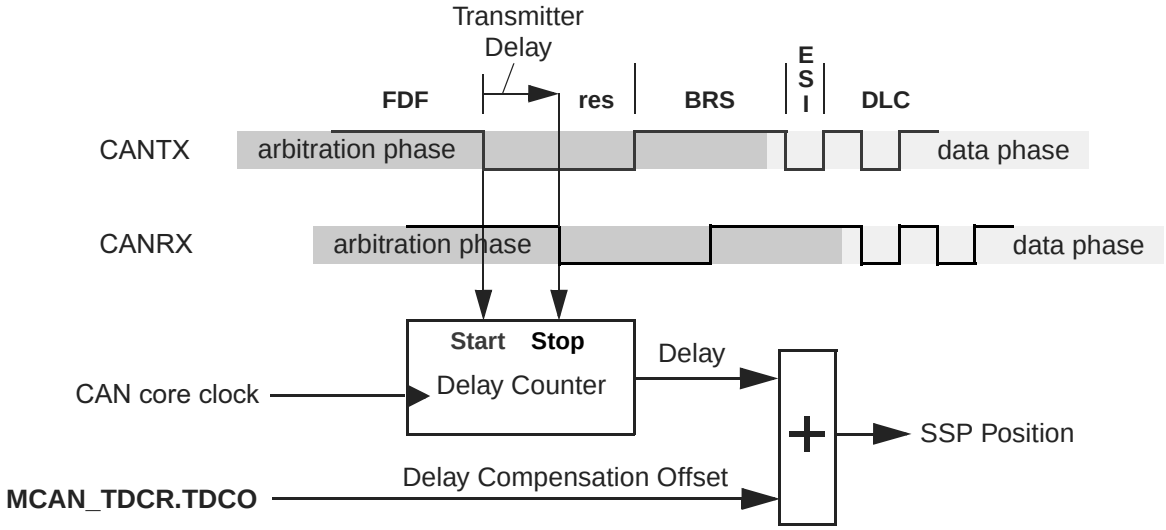
The following boundary conditions have to be considered for the delay compensation implemented in the MCAN:

- The sum of the measured delay from CANTX to CANRX and the configured delay compensation offset MCAN_TDCR.TDCO has to be less than 6 bit times in the data phase.
- The sum of the measured delay from CANTX to CANRX and the configured delay compensation offset MCAN_TDCR.TDCO has to be less or equal 127 CAN core clock periods. In case this sum exceeds 127 CAN core clock periods, the maximum value of 127 CAN core clock periods is used for delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs.
- Transmitter Delay Measurement

If transmitter delay compensation is enabled by programming MCAN_DBTP.TDC = '1', the measurement is started within each transmitted CAN FD frame at the falling edge of bit FDF to bit res. The measurement is stopped when this edge is seen at the receive input CANRX of the transmitter.

The resolution of this measurement is one mtq.

Figure 53-2: Transmitter Delay Measurement



To avoid that a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in a to early SSP position, the use of a transmitter delay compensation filter window can be enabled by programming MCAN_TDCR.TDCF.

This defines a minimum value for the SSP position. Dominant edges on CANRX, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR.TDCF AND CANRX is low.

53.5.1.5 Restricted Operation Mode

In Restricted Operation mode, the node is able to receive data and remote frames and to give acknowledge to valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The error counters are not incremented. The processor can set the MCAN into Restricted Operation mode by setting bit MCAN_CCCR.ASM. The bit can only be set by the processor when both MCAN_CCCR.CCE and MCAN_CCCR.INIT are set to '1'. The bit can be reset by the processor at any time.

Restricted Operation mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation mode, the processor has to reset MCAN_CCCR.ASM.

Table 54-4: I/O Lines (Continued)

TC1	TCLK4	PC11	D
TC1	TCLK5	PA8	D
TC1	TCLK5	PB30	D
TC1	TIOA3	PB9	A
TC1	TIOA3	PB19	D
TC1	TIOA3	PD29	D
TC1	TIOA4	PA9	D
TC1	TIOA4	PC9	D
TC1	TIOA5	PA6	D
TC1	TIOA5	PB28	D
TC1	TIOB3	PB10	A
TC1	TIOB3	PB20	D
TC1	TIOB3	PD30	D
TC1	TIOB4	PA10	D
TC1	TIOB4	PC10	D
TC1	TIOB5	PA7	D
TC1	TIOB5	PB29	D

54.5.2 Power Management

The TC is clocked through the Power Management Controller (PMC), thus the programmer must first configure the PMC to enable the Timer Counter clock.

54.5.3 Interrupt Sources

The TC has an interrupt line connected to the interrupt controller. Handling the TC interrupt requires programming the interrupt controller before configuring the TC.

Table 54-5: Peripheral IDs

Instance	ID
TC0	35
TC1	36

54.5.4 Synchronization Inputs from PWM

The TC has trigger/capture inputs internally connected to the PWM. Refer to Section 54.6.14 “Synchronization with PWM” and to the implementation of the Pulse Width Modulation (PWM) in this product.

54.5.5 Fault Output

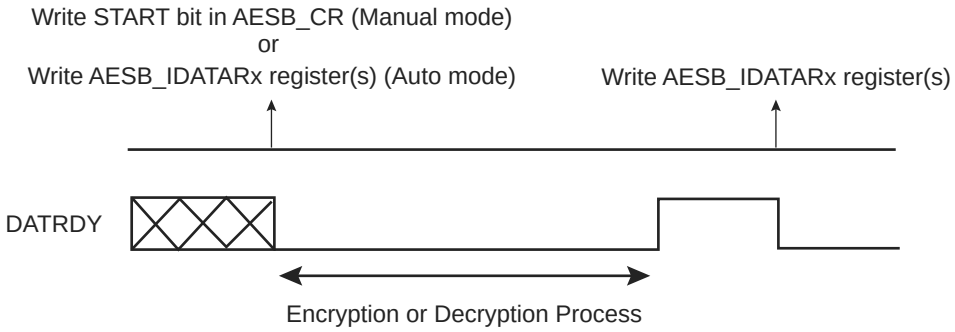
The TC has the FAULT output internally connected to the fault input of PWM. Refer to Section 54.6.18 “Fault Mode” and to the implementation of the Pulse Width Modulation (PWM) in this product.

54.6 Functional Description

54.6.1 Description

All channels of the Timer Counter are independent and identical in operation except when the QDEC is enabled. The registers for channel programming are listed in Table 54-6 “Register Mapping”.

Figure 59-2: Manual and Auto Modes with AESB_MR.LOD = 1



59.3.6 Automatic Bridge Mode

59.3.6.1 Description

The Automatic Bridge mode, when the AESB block is connected between the system bus and a DDR port and the QSPI, provides automatic encryption/decryption without any action on the part of the user. For Automatic Bridge mode, the OPMODE field must be configured to 0x4 in AESB_MR (refer to Section 59.4.2 “AESB Mode Register”). If bit AESB_MR.AAHB is set and field AESB_MR.OPMODE = 0x4, there is no compliance with the standard CTR mode of operation.

In case of write transfer, this mode automatically encrypts the data before writing it to the final slave destination. In case of read transfer, this mode automatically decrypts the data read from the target slave before putting it on the system bus.

Therefore, this mode does not work if the automatically encrypted data is moved at another address outside of the AESB IP scope. This means that for a given data, the encrypted value is not the same if written at different addresses.

59.3.6.2 Configuration

The Automatic Bridge mode can be enabled by setting bit AESB_MR.AAHB.

The IV (Initialization Vector) field of the AESB Initialization Vector Register x (AESB_IVRx) can be used to add a nonce in the encryption process in order to bring even more security (ignored if not filled). In this case, any value encrypted with a given nonce can only be decrypted with this nonce. If another nonce is set for the IV field, any value encrypted with the previous nonce cannot be decrypted anymore (refer to Section 59.4.10 “AESB Initialization Vector Register x”).

Dual buffer usage (write a 1 to bit AESB_MR.DUALBUFF) is recommended for improved performance.

59.3.7 Security Features

59.3.7.1 Unspecified Register Access Detection

When an unspecified register access occurs, the URAD bit in AESB_ISR raises. Its source is then reported in the Unspecified Register Access Type (URAT) field. Only the last unspecified register access is available through the URAT field.

Several kinds of unspecified register accesses can occur:

- Input Data Register written during the data processing when SMOD = IDATAR0_START
- Output Data Register read during data processing
- Mode Register written during data processing
- Output Data Register read during sub-keys generation
- Mode Register written during sub-keys generation
- Write-only register read access

The URAD bit and the URAT field can only be reset by AESB_CR.SWRST.

64.6.9 SECUMOD RAM Access Rights Register

Name: SECUMOD_RAMACC

Address: 0xFC040074

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	RW5		RW4	

7	6	5	4	3	2	1	0
RW3		RW2		RW1		RW0	

The following configuration values are valid for all listed bit names of this register:

00: No access allowed

01: Only write access allowed

10: Only read access allowed

11: Read and write accesses allowed

Accessing a forbidden area causes an interrupt (SECURAM ID).

RW0: Access right for RAM region [0; 1 Kbyte]

RW1: Access right for RAM region [1 Kbyte; 2 Kbytes]

RW2: Access right for RAM region [2 Kbytes; 3 Kbytes]

RW3: Access right for RAM region [3 Kbytes; 4 Kbytes]

RW4: Access right for RAM region [4 Kbytes; 5 Kbytes]

RW5: Access right for RAM region [5 Kbytes; 6 Kbytes] (register bank BUREG256b)