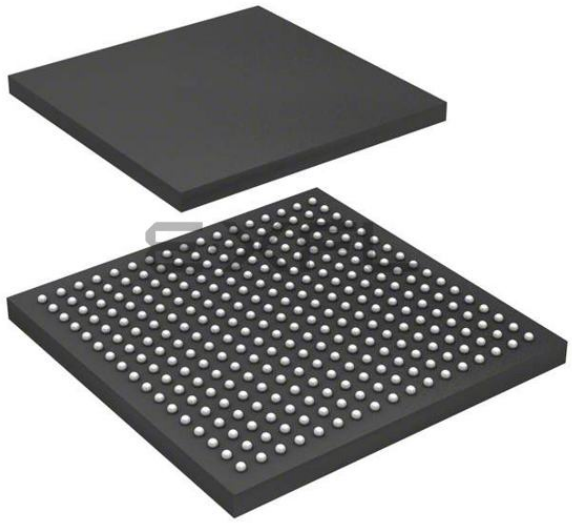


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26b-cn

Figure 7-1: Recommended Powerup Sequence

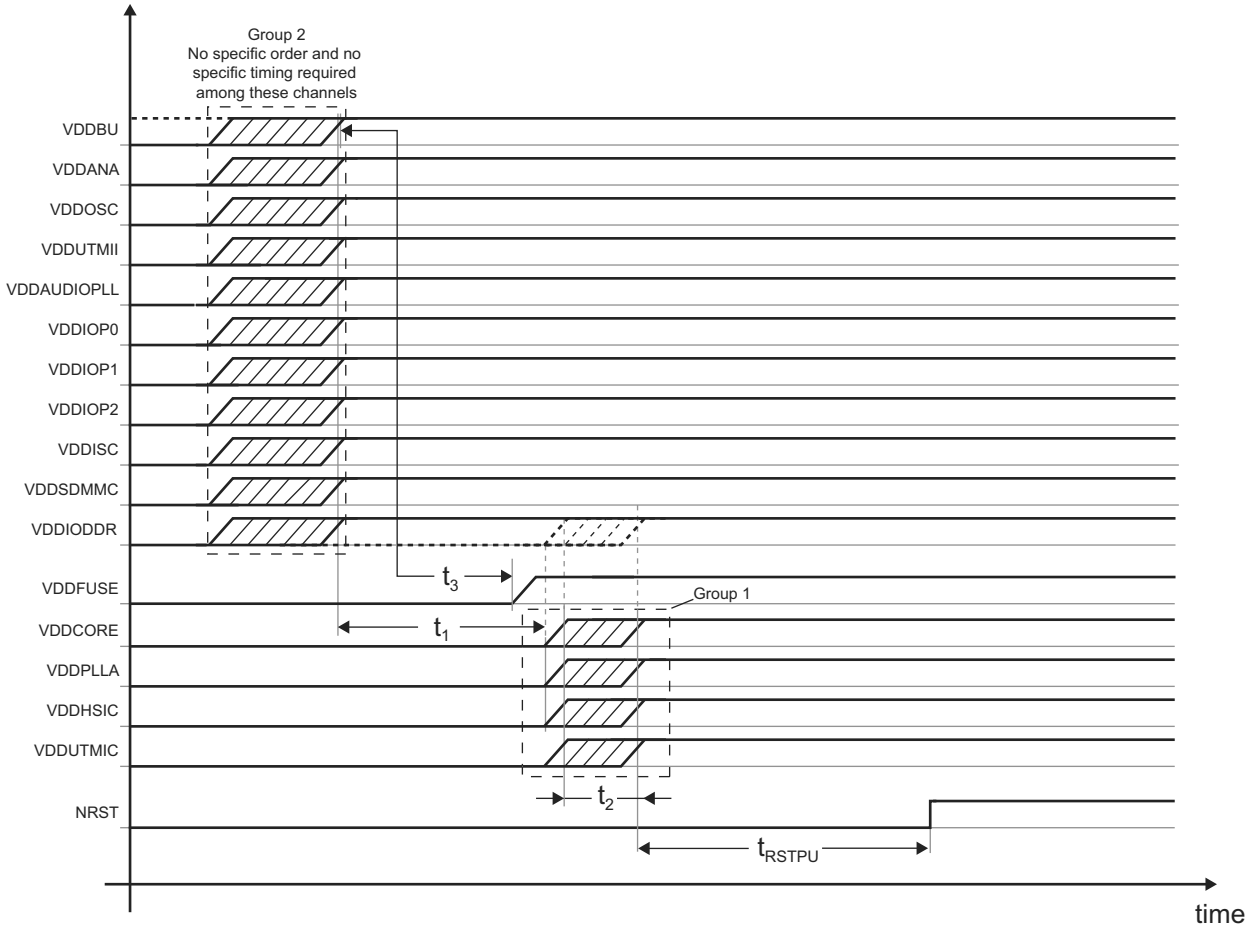


Table 7-2: Powerup Timing Specification

Symbol	Parameter	Conditions	Min	Max	Unit
t_1	Group 2 to Group 1 delay	Delay from the last Group 2 established(1) supply to the first Group1 supply turn-on	0	–	ms
t_2	Group 1 delay(2)	Delay from the first group 1 established supply to the last Group 1 established supply	–	1	
t_3	VDDFUSE to VDDBU delay	Delay from VDDBU established to VDDFUSE turn-on	1	–	
t_{RSTPU}	Reset delay at powerup	From the last established supply to NRST high	1	–	

Note 1: An “established” supply refers to a power supply established at 90% of its final value.

2: Also applies to VDDIODDR when considered as part of Group 1.

26.6.17 RTC TimeStamp Time Register 0 (UTC_MODE)

Name: RTC_TSTR0 (UTC_MODE)

Address: 0xF8048160

Access: Read-only

31	30	29	28	27	26	25	24
BACKUP	–	–	–	TEVCNT			
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

RTC_TSTR0 reports the timestamp of the first tamper event.

TEVCNT: Tamper Events Counter (cleared by reading RTC_TSSR0)

Each time a tamper event occurs, this counter is incremented. This counter saturates at 15. Once this value is reached, it is no more possible to know the exact number of tamper events.

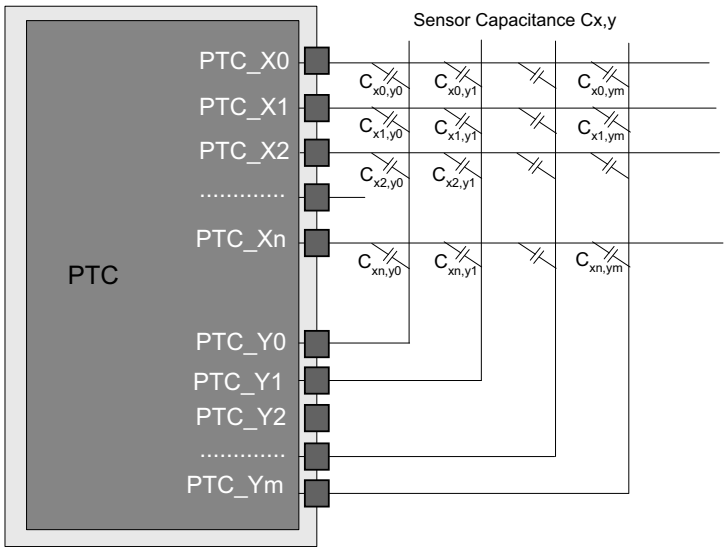
If this field is not null, this implies that at least one tamper event occurs since last register reset and that the values stored in timestamping registers are valid.

BACKUP: System Mode of the Tamper (cleared by reading RTC_TSSR0)

0: The state of the system is different from Backup mode when the tamper event occurs.

1: The system is in Backup mode when the tamper event occurs.

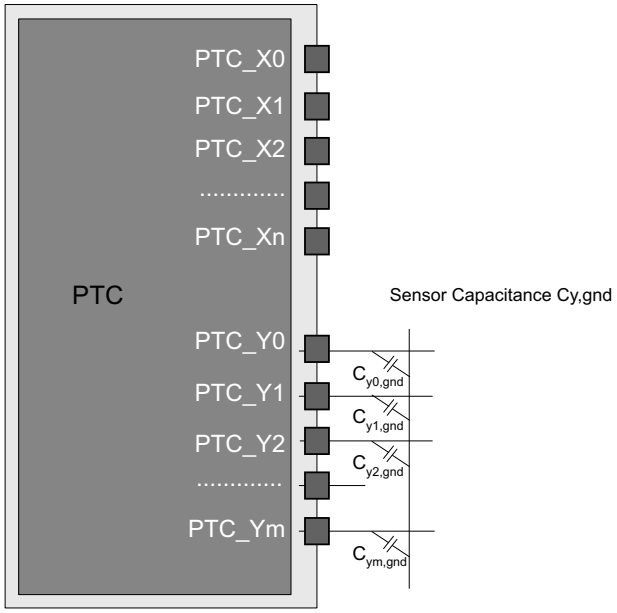
Figure 29-6: Mutual Capacitance Sensor Arrangement



29.6.6 Operations in Self-capacitance

The self-capacitance sensor is connected to a single pin on the PTC through the PTC_Ym electrodes to receive the signal. The sensor electrode capacitance is measured by the PTC.

Figure 29-7: Self-capacitance Sensor Arrangement



31.7.3 ACC Write Protection Mode Register

Name: ACC_WPMR

Address: 0xF804A0E4

Access: Read/Write

31	30	29	28	27	26	25	24
WPKEY							
23	22	21	20	19	18	17	16
WPKEY							
15	14	13	12	11	10	9	8
WPKEY							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPEN

WPEN: Write Protection Enable

0: Disables the write protection if WPKEY corresponds to 0x414343 (“ACC” in ASCII).

1: Enables the write protection if WPKEY corresponds to 0x414343 (“ACC” in ASCII).

Refer to Section 31.6.2 “Register Write Protection” for the list of registers that can be write-protected.

WPKEY: Write Protection Key

Value	Name	Description
0x414343	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

37.20.41 Write Protection Mode Register

Name: HSMC_WPMR

Address: 0xF80147E4

Access: Read/Write

31	30	29	28	27	26	25	24
WPKEY							

23	22	21	20	19	18	17	16
WPKEY							

15	14	13	12	11	10	9	8
WPKEY							

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPEN

WPEN: Write Protection Enable

0: Disables write protection if WPKEY value corresponds to 0x534D43 (“SMC” in ASCII)

1: Enables write protection if WPKEY value corresponds to 0x534D43 (“SMC” in ASCII)

See Section 37.16 “Register Write Protection” for list of write-protected registers.

WPKEY: Write Protection Key

Value	Name	Description
0x534D43	PASSWD	Writing any other value in this field aborts the write operation of bit WPEN. Always reads as 0.

39.7.55 Overlay 2 Channel Enable Register

Name: LCDC_OVR2CHER

Address: 0xF0000240

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	A2QEN	UPDATEEN	CHEN

CHEN: Channel Enable

0: No effect

1: Enables the DMA channel

UPDATEEN: Update Overlay Attributes Enable

0: No effect

1: Updates windows attributes on the next start of frame.

A2QEN: Add To Queue Enable

0: No effect

1: Indicates that a valid descriptor has been written to memory, its memory location should be written to the DMA head pointer. The A2QSR status bit is set to one, and it is reset by hardware as soon as the descriptor pointed to by the DMA head pointer is added to the list.

39.7.76 High-End Overlay Channel Enable Register

Name: LCDC_HEOCHER

Address: 0xF0000340

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	A2QEN	UPDATEEN	CHEN

CHEN: Channel Enable

0: No effect

1: Enables the DMA channel

UPDATEEN: Update Overlay Attributes Enable

0: No effect

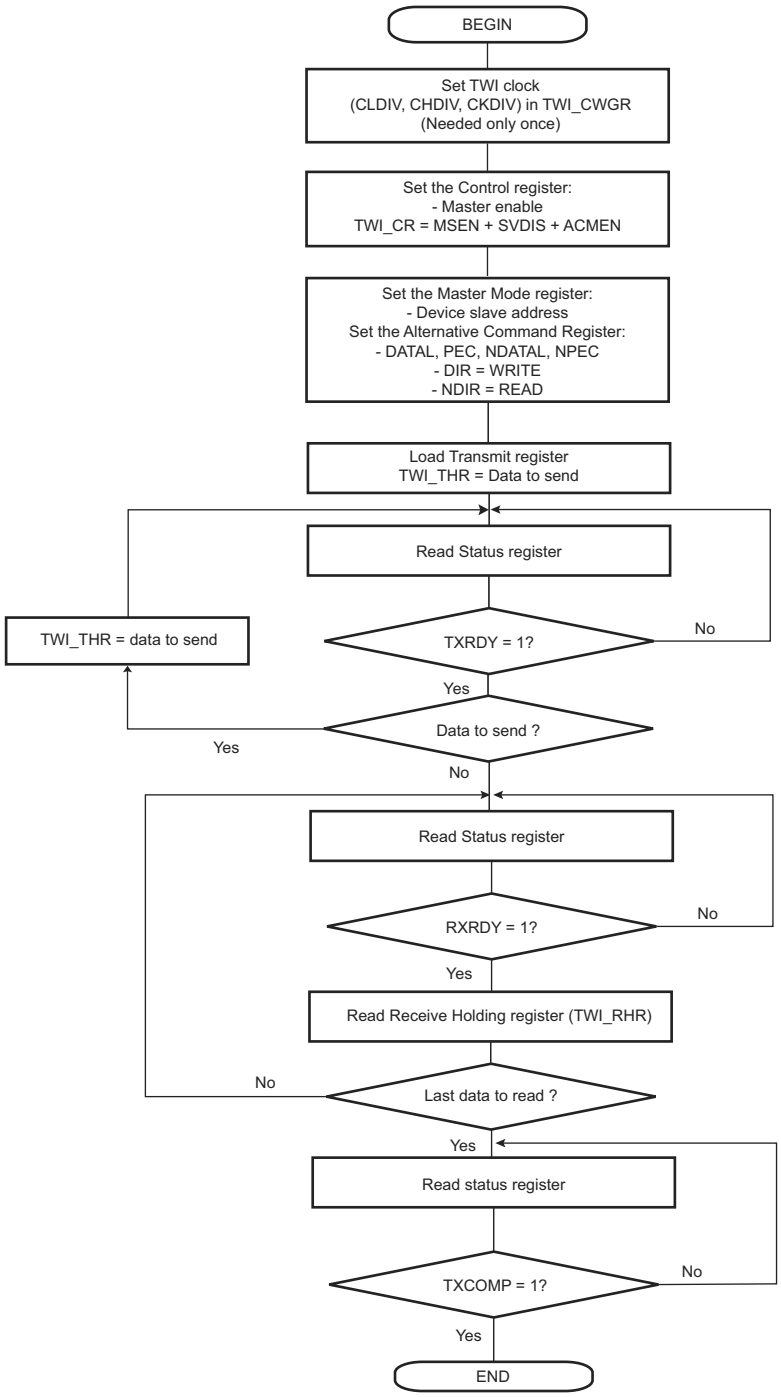
1: Updates windows attributes on the next start of frame.

A2QEN: Add To Queue Enable

0: No effect

1: Indicates that a valid descriptor has been written to memory, its memory location should be written to the DMA head pointer. The A2QSR status bit is set to one, and it is reset by hardware as soon as the descriptor pointed to by the DMA head pointer is added to the list.

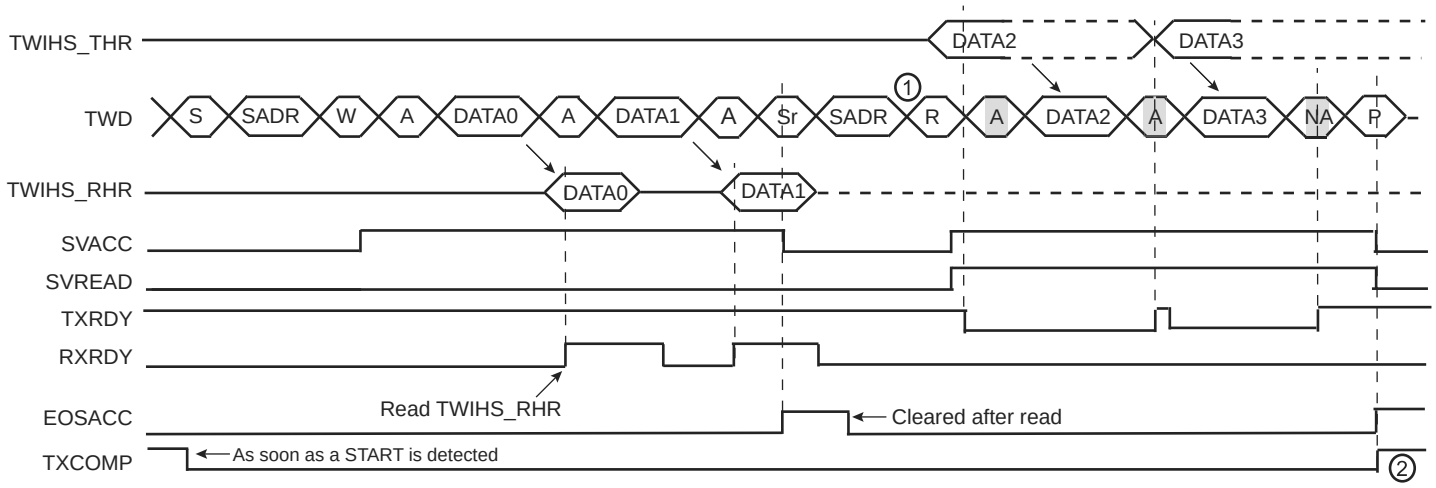
Figure 46-20: TWIHS Write Operation with Multiple Data Bytes + Read Operation and Alternative Command Mode + PEC



Reversal of Write to Read

The master initiates the communication by a write command and finishes it by a read command. Figure 46-42 describes the REPEATED START and the reversal from Write mode to Read mode.

Figure 46-42: Repeated Start and Reversal from Write Mode to Read Mode



Note 1: In this case, if TWIHS_THR has not been written at the end of the read command, the clock is automatically stretched before the ACK.

2: TXCOMP is only set at the end of the transmission. This is because after the REPEATED START, SADR is detected again.

0: No effect.

1: Alternative Command mode disabled.

TXFCLR: Transmit FIFO Clear

0: No effect.

1: Clears the Transmit FIFO, Transmit FIFO will become empty.

RXFCLR: Receive FIFO Clear

0: No effect.

1: Clears the Receive FIFO, Receive FIFO will become empty.

TXFLCLR: Transmit FIFO Lock CLEAR

0: No effect.

1: Clears the Transmit FIFO Lock.

FIFOEN: FIFO Enable

0: No effect.

1: Enables the Transmit and Receive FIFOs

FIFODIS: FIFO Disable

0: No effect.

1: Disables the Transmit and Receive FIFOs

47.10.32 USART LIN Identifier Register

Name: FLEX_US_LINIR

Address: 0xF8034258 (0), 0xF8038258 (1), 0xFC010258 (2), 0xFC014258 (3), 0xFC018258 (4)

Access: Read/Write or Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
IDCHR							

This register is relevant only if USART_MODE = 0xA or 0xB in Section 47.10.6 ”USART Mode Register”.

IDCHR: Identifier Character

If USART_MODE = 0xA (master node configuration):

IDCHR is Read/Write and its value is the identifier character to be transmitted.

If USART_MODE = 0xB (slave node configuration):

IDCHR is Read-only and its value is the last identifier character that has been received.

48. Universal Asynchronous Receiver Transmitter (UART)

48.1 Description

The Universal Asynchronous Receiver Transmitter (UART) features a two-pin UART that can be used for communication and trace purposes and offers an ideal medium for in-situ programming solutions.

Moreover, the association with a DMA controller permits packet handling for these tasks with processor time reduced to a minimum.

48.2 Embedded Characteristics

- Two-pin UART
  - Independent Receiver and Transmitter with a Common Programmable Baud Rate Generator
  - Baud Rate can be Driven by Processor-Independent Generic Source Clock
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Digital Filter on Receive Line
  - Interrupt Generation
  - Support for Two DMA Channels with Connection to Receiver and Transmitter
  - Supports Asynchronous Partial Wakeup on Receive Line Activity (SleepWalking)
  - Comparison Function on Received Character
  - Receiver Timeout
  - Register Write Protection

48.3 Block Diagram

Figure 48-1: UART Block Diagram

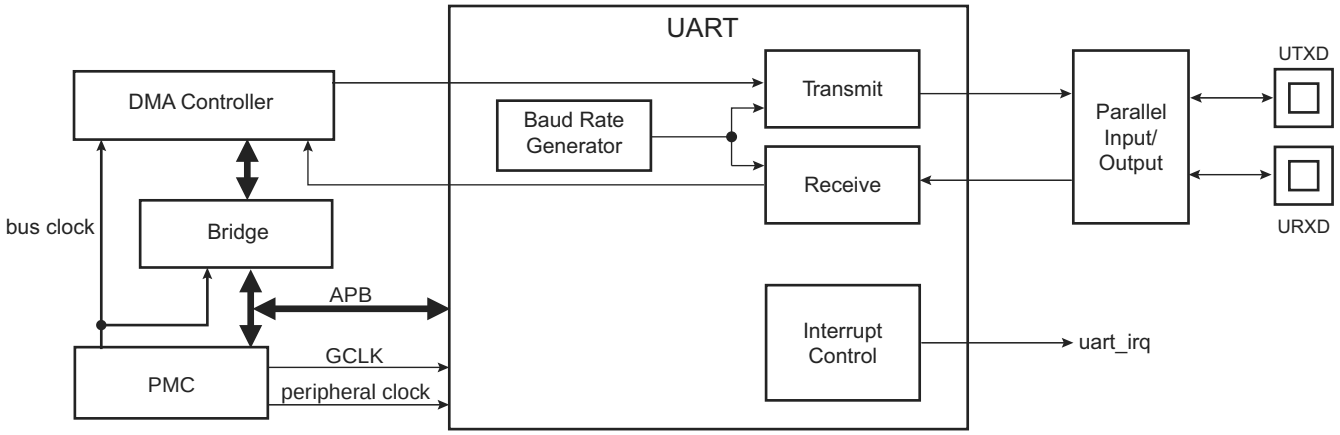


Table 48-1: UART Pin Description

Pin Name	Description	Type
URXD	UART Receive Data	Input
UTXD	UART Transmit Data	Output

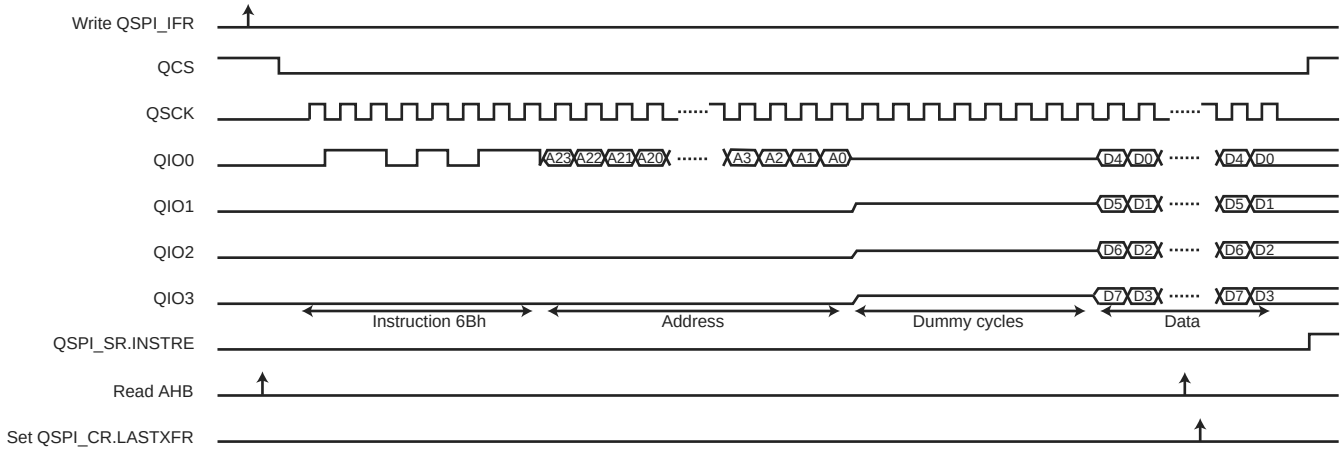
Example 6:

Instruction in Single-bit SPI, with address in Single-bit SPI, without option, with data read in Quad SPI, with eight dummy cycles.

Command: QUAD_OUTPUT READ ARRAY (6Bh)

- Write 0x0000_006B in QSPI_ICR.
- Write 0x0008_10B2 in QSPI_IFR.
- Read QSPI_IR (dummy read) to synchronize system bus accesses.
- Read data in the QSPI system bus memory space (0x9000_00000-0x9800_00000/0XD000_0000--0XD800_0000).
  The address of the first system bus read access is sent in the instruction frame.
  The address of the next system bus read accesses is not used.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 50-16: Instruction Transmission Waveform 6



51.13.53 SDMMC Retuning Interrupt Signal Enable Register

Name: SDMMC_RTISIER

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	TEVT

TEVT: Retuning Timer Event

0 (MASKED): No interrupt is generated when the TEVT status rises in SDMMC_RTISTR.

1 (ENABLED): An interrupt is generated when the TEVT status rises in SDMMC_RTISTR.

RERR: Read Channel Error Interrupt Mask

0: The interrupt is disabled.

1: The interrupt is enabled.

VFPOV: Vertical Front Porch Overflow Interrupt Mask

0: The interrupt is disabled.

1: The interrupt is enabled.

DAOV: Data Overflow Interrupt Mask

0: The interrupt is disabled.

1: The interrupt is enabled.

VDTO: Vertical Synchronization Timeout Interrupt Mask

0: The interrupt is disabled.

1: The interrupt is enabled.

HDTO: Horizontal Synchronization Timeout Interrupt Mask

0: The interrupt is disabled.

1: The interrupt is enabled.

CCIRERR: CCIR Decoder Error Interrupt Mask

0: The interrupt is disabled.

1: The interrupt is enabled.

CAN FD operation is enabled by programming CCCR.FDOE. In case CCCR.FDOE = '1', transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured via bit FDF in the respective Tx Buffer element. With CCCR.FDOE = '0', received frames are interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if bit FDF of a Tx Buffer element is set. CCCR.FDOE and CCCR.BRSE can only be changed while CCCR.INIT and CCCR.CCE are both set.

With MCAN_CCCR.FDOE = 0, the setting of bits FDF and BRS is ignored and frames are transmitted in Classic CAN format. With MCAN_CCCR.FDOE = 1 and MCAN_CCCR.BRSE = 0, only bit FDF of a Tx Buffer element is evaluated. With MCAN_CCCR.FDOE = 1 and MCAN_CCCR.BRSE = 1, transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with bits FDF and BRS set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significant higher than in the CAN FD arbitration phase. In this case disable the CAN FD bit rate switching option for transmissions.
- During system startup all nodes are transmitting according to ISO11898-1 until it is verified that they are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wake-up messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD-capable. Non-CAN FD nodes are held in Silent mode until programming has completed. Then all nodes revert to Classic CAN communication.

In the CAN FD format, the coding of the DLC differs from the standard CAN format. The DLC codes 0 to 8 have the same coding as in standard CAN, the codes 9 to 15, which in standard CAN all code a data field of 8 bytes, are coded according to Table 53-3 below.

Table 53-3: Coding of DLC in CAN FD

DLC	9	10	11	12	13	14	15
Number of Data Bytes	12	16	20	24	32	48	64

In CAN FD frames, the bit timing will be switched inside the frame, after the BRS (Bit Rate Switch) bit, if this bit is recessive. Before the BRS bit, in the CAN FD arbitration phase, the nominal CAN bit timing is used as defined by the Nominal Bit Timing and Prescaler register (MCAN_NBTP). In the following CAN FD data phase, the data phase CAN bit timing is used as defined by the Data Bit Timing and Prescaler register (MCAN_DBTP). The bit timing reverts back from the data phase timing at the CRC delimiter or when an error is detected, whichever occurs first.

The maximum configurable bit rate in the CAN FD data phase depends on the CAN core clock frequency. Example: with a CAN clock frequency of 20 MHz and the shortest configurable bit time of 4 t_q, the bit rate in the data phase is 5 Mbit/s.

In both data frame formats, CAN FD and CAN FD with bit rate switching, the value of the bit ESI (Error Status Indicator) is determined by the transmitter's error state at the start of the transmission. If the transmitter is error passive, ESI is transmitted recessive, else it is transmitted dominant.

53.5.1.4 Transmitter Delay Compensation

During the data phase of a CAN FD transmission only one node is transmitting, all others are receivers. The length of the bus line has no impact. When transmitting via pin CANTX the protocol controller receives the transmitted data from its local CAN transceiver via pin CANRX. The received data is delayed by the transmitter delay. In case this delay is greater than TSEG1 (time segment before sample point), a bit error is detected. In order to enable a data phase bit time that is even shorter than the transmitter delay, the delay compensation is introduced. Without delay compensation, the bit rate in the data phase of a CAN FD frame is limited by the delay.

- Description

The MCAN protocol unit has implemented a delay compensation mechanism to compensate the delay, thereby enabling transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver.

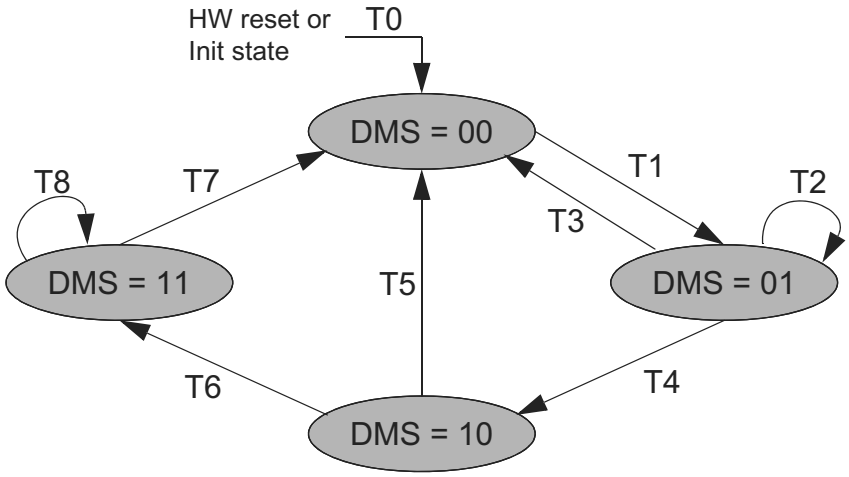
To check for bit errors during the data phase, the delayed transmit data is compared against the received data at the secondary sample point. If a bit error is detected, the transmitter will react to this bit error at the next following regular sample point. During arbitration phase the delay compensation is always disabled.

The transmitter delay compensation enables configurations where the data bit time is shorter than the transmitter delay, it is described in detail in the new ISO11898-1. It is enabled by setting bit MCAN_DBTP.TDC.

The debug message handling state machine ensures that debug messages are stored to three consecutive Rx Buffers in the correct order. If some messages are missing, the process is restarted. The DMA request is activated only when all three debug messages A, B, C have been received in the correct order.

The status of the debug message handling state machine is signalled via MCAN_RXF1S.DMS.

Figure 53-9: Debug Message Handling State Machine



T0: reset m_can_dma_req output, enable reception of debug messages A, B, and C

T1: reception of debug message A

T2: reception of debug message A

T3: reception of debug message C

T4: reception of debug message B

T5: reception of debug messages A, B

T6: reception of debug message C

T7: DMA transfer completed

T8: reception of debug message A,B,C (message rejected)

53.5.5 Tx Handling

The Tx Handler handles transmission requests for the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue. It controls the transfer of transmit messages to the CAN Core, the Put and Get Indices, and the Tx Event FIFO. Up to 32 Tx Buffers can be set up for message transmission. The CAN mode for transmission (Classic CAN or CAN FD) can be configured separately for each Tx Buffer element. The Tx Buffer element is described in Section 53.5.7.3. Table 53-7 describes the possible configurations for frame transmission.

Table 53-7: Possible Configurations for Frame Transmission

MCAN_CCCR		Tx Buffer Element		
BRSE	**FDOE**	**FDF**	**BRS**	**Frame Transmission**
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	FD without bit rate switching
1	1	1	1	FD with bit rate switching

66.9 USB HS Characteristics

66.9.1 Electrical Characteristics

The device conforms to all voltage, power, and timing characteristics and specifications set forth in the USB 2.0 Specification. Refer to the USB 2.0 Specification for more information.

66.9.2 Dynamic Power Consumption

Table 66-27: USB Transceiver Dynamic Power Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BIAS}	Bias Generator Current Consumption	–	–	0.7	0.8	mA
$I_{VDDUTMII}$	HS Transceiver Current Consumption	HS transmission	–	47	60	mA
	HS Transceiver Current Consumption	HS reception	–	18	27	mA
	LS / FS Transceiver Current Consumption	FS transmission 0m cable(1)	–	4	6	mA
	LS / FS Transceiver Current Consumption	FS transmission 5m cable(1)	–	26	30	mA
	LS / FS Transceiver Current Consumption	FS reception(1)	–	3	4.5	mA
$I_{VDDUTMIC}$	Core	–	–	5.5	9	mA

Note: 1. Including 1 mA due to pull-up/pull-down current consumption.

66.10 PTC Characteristics

Table 66-28: PTC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Type
C_C	Compensation Capacitance	Programmable max code 0x3FFF	30	–	–	pF	-
E_{RS}	Error on Serial filtering Resistance	20, 50, 100 kOhm	-20	–	20	%	-
I_{PTCT}	PTC Current Consumption	–	–	–	500	µA	-

66.11 ADC Characteristics

Electrical data are in accordance with an operating temperature range from -40°C to +85°C unless otherwise specified.

ADVREF is the positive reference of the ADC.

66.11.1 ADC Power Supply

66.11.1.1 Power Supply Characteristics

Table 66-29: Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDIN}	Analog Current Consumption	Sleep mode(1) Fast Wakeup mode Normal mode, single sampling	-	2 0.4 2.2	4 0.6 3.0	µA mA mA
$I_{VDDCORE}$	Digital Current Consumption	Sleep mode(1) Normal mode	-	1 80	2 100	µA µA

Note: 1. In Sleep mode, the ADC core, the Sample and Hold and the internal reference operational amplifier are off.

Table 66-66: SPI1 IOSET1 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
Master Mode						
SPI_0	MISO Setup time before SPCK rises	14.6	–	13.1	–	ns
SPI_1	MISO Hold time after SPCK rises	0	–	0	–	ns
SPI_2	SPCK rising to MOSI	0	0.8	0	1.2	ns
SPI_3	MISO Setup time before SPCK falls	15	–	13.7	–	ns
SPI_4	MISO Hold time after SPCK falls	0	–	0	–	ns
SPI_5	SPCK falling to MOSI	0	0.9	0	1.6	ns
Slave Mode						
SPI_6	SPCK falling to MISO	10.3	12.4	8.3	11.2	ns
SPI_7	MOSI Setup time before SPCK rises	3.5	–	3.4	–	ns
SPI_8	MOSI Hold time after SPCK rises	0.8	–	0.7	–	ns
SPI_9	SPCK rising to MISO	9.8	11.8	7.8	10.4	ns
SPI_{10}	MOSI Setup time before SPCK falls	3.5	–	3.4	–	ns
SPI_{11}	MOSI Hold time after SPCK falls	0.8	–	0.7	–	ns
SPI_{12}	NPCS0 setup to SPCK rising	4.9	–	4.8	–	ns
SPI_{13}	NPCS0 hold after SPCK falling	1.1	–	0.9	–	ns
SPI_{14}	NPCS0 setup to SPCK falling	4.4	–	4.4	–	ns
SPI_{15}	NPCS0 hold after SPCK rising	0.5	–	0.3	–	ns
SPI_{16}	NPCS0 falling to MISO valid	14.7	–	13.4	–	ns

Table 72-6: SAMA5D2 Datasheet Rev. 11267B Revision History

Issue Date	Changes
13-Nov-15	“Features” Updated Security features
	Section 3. “Block Diagram” Updated Figure 3-1 “SAMA5D2 Series Block Diagram”.
	Section 5. “Package and Pinout” Updated Table 5-2 “Pin Description (SAMA5D21, SAMA5D22, SAMA5D24, SAMA5D26, SAMA5D27, SAMA5D28A)” Removed Section 4.2 “Input/Output Description” and Section 4-3 “SAMA5D2 I/O Type Description”
	Section 6. “Power Considerations” Updated Table 6-1 “SAMA5D2 Power Supplies” Updated Figure 6-1 “Recommended Powerup Sequence”, Figure 6-2 “Recommended Powerdown Sequence”, Figure 6-3 “Recommended Backup Mode Entry”, Figure 6-4 “Recommended Power Supply Sequencing at Wakeup”
	Section 8. “Event System” Updated Table 8-1 “Real-time Event Mapping List”
	Section 15. “Standard Boot Strategies” Replaced all instances of "GPBR" with "BUREG".
	Section 20. “Special Function Registers (SFR)” Updated Section 20.3.15 “I2S Register”
	Section 20. “Advanced Interrupt Controller (AIC)” Removed Sections “Interrupt Vectoring” and “Fast Interrupt Vectoring” Updated Section 20.8.3.3 “Interrupt Handlers”and Section 20.8.4.3 “Fast Interrupt Handlers”
	Section 29. “Power Management Controller (PMC)” Replaced “generated clock” with “generic clock”, and “GCK” with “GCLK” Updated Section 29.22.8 “PMC Clock Generator Main Oscillator Register”
	Section 37. “Parallel Input/Output Controller (PIO)” Removed all references to programmable I/O delay
	Added Section 32. “External Memories”
	Section 33. “Multi-port DDR-SDRAM Controller (MPDDRC)” Section 33.4.3 “Low-power DDR2-SDRAM Initialization”: added Step 14., Step 15. and Step 21. Section 33.4.5 “Low-power DDR3-SDRAM Initialization”: added Step 14., Step 15. and Step 21. Section 33.7.8 “MPDDRC Memory Device Register”: updated DBW field description; corrected location of fields RL3 and WL
	Section 37. “Ethernet MAC (GMAC)” Updated Section 37.1 “Description” Section 37.5.2 “Power Management”: deleted reference to PMC_PCER Section 37.5.3 “Interrupt Sources”: deleted reference to ‘Advanced Interrupt Controller’. Replaced by ‘Interrupt Controller’. Section 37.6.14 “IEEE 1588 Support”: deleted reference to GMAC_TSSx. Removed reference to ‘output pins’ in 2nd paragraph. Section 37.6.15 “Time Stamp Unit”: added information on GTSUCOMP signal in last paragraph