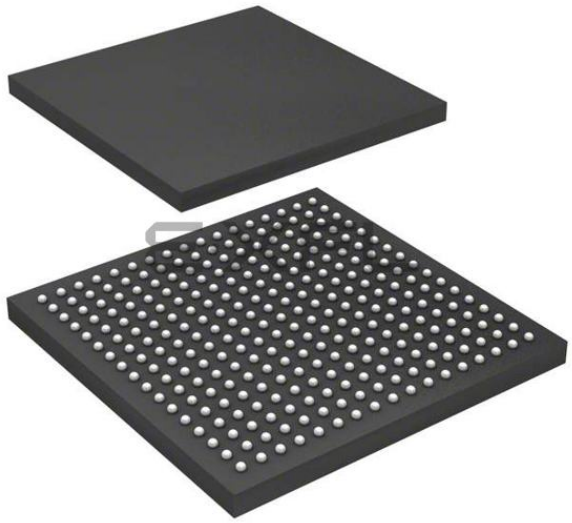


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26b-cnr

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)(1)(2)
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
A6	B6	B5	VDDIOP0	GPIO	PB3	I/O	–	–	A	URXD4	I	1	PIO, I, PU, ST
									B	D8	I/O	1	
									C	IRQ	I	3	
									D	PWMEXTRG1	I	1	
									F	CLASSD_R2	O	1	
B6	A6	A4	VDDIOP0	GPIO	PB4	I/O	–	–	A	UTXD4	O	1	PIO, I, PU, ST
									B	D9	I/O	1	
									C	FIQ	I	4	
									F	CLASSD_R3	O	1	
B7	D7	D6	VDDIOP0	GPIO_QSPI	PB5	I/O	–	–	A	TCLK2	I	1	PIO, I, PU, ST
									B	D10	I/O	1	
									C	PWMH2	O	1	
									D	QSPI1_SCK	O	2	
									F	GTSUCOMP	O	3	
C7	B5	A3	VDDIOP0	GPIO	PB6	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
									B	D11	I/O	1	
									C	PWML2	O	1	
									D	QSPI1_CS	O	2	
									F	GTXER	O	3	
C6	A5	B4	VDDIOP0	GPIO_IO	PB7	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
									B	D12	I/O	1	
									C	PWMH3	O	1	
									D	QSPI1_IO0	I/O	2	
									F	GRXCK	I	3	
A5	E7	A2	VDDIOP0	GPIO_IO	PB8	I/O	–	–	A	TCLK3	I	1	PIO, I, PU, ST
									B	D13	I/O	1	
									C	PWML3	O	1	
									D	QSPI1_IO1	I/O	2	
									F	GCRS	I	3	
A4	F6	B3	VDDIOP0	GPIO_IO	PB9	I/O	–	–	A	TIOA3	I/O	1	PIO, I, PU, ST
									B	D14	I/O	1	
									C	PWMFI1	I	1	
									D	QSPI1_IO2	I/O	2	
									F	GCOL	I	3	

See Section 14.4.1 “Double Linefill Issuing” for details on double linefill functionality.

19.3.3 OHCI Interrupt Status Register

Name: SFR_OHCIISR

Address: 0xF8030014

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	RIS2	RIS1	RIS0

RISx: OHCI Resume Interrupt Status Port x

0: OHCI port resume not detected.

1: OHCI port resume detected.

38.9.2 XDMAC Global Configuration Register

Name: XDMAC_GCFG

Address: 0xF0010004 (0), 0xF0004004 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	BXKBEN
7	6	5	4	3	2	1	0
–	–	–	–	CGDISIF	CGDISFIFO	CGDISPIPE	CGDISREG

CGDISREG: Configuration Registers Clock Gating Disable

0: The automatic clock gating is enabled for the configuration registers.

1: The automatic clock gating is disabled for the configuration registers.

CGDISPIPE: Pipeline Clock Gating Disable

0: The automatic clock gating is enabled for the main pipeline.

1: The automatic clock gating is disabled for the main pipeline.

CGDISFIFO: FIFO Clock Gating Disable

0: The automatic clock gating is enabled for the main FIFO.

1: The automatic clock gating is disabled for the main FIFO.

CGDISIF: Bus Interface Clock Gating Disable

0: The automatic clock gating is enabled for the system bus interface.

1: The automatic clock gating is disabled for the system bus interface.

BXKBEN: Boundary X Kilobyte Enable

0: The 1 Kbyte boundary is used.

1: The controller does not meet the AHB specification.

38.9.13 XDMAC Global Channel Read Write Suspend Register

Name: XDMAC_GRWS

Address: 0xF0010030 (0), 0xF0004030 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
RWS15	RWS14	RWS13	RWS12	RWS11	RWS10	RWS9	RWS8

7	6	5	4	3	2	1	0
RWS7	RWS6	RWS5	RWS4	RWS3	RWS2	RWS1	RWS0

RWSx: XDMAC Channel x Read Write Suspend Bit

0: No effect.

1: Read and write requests are suspended.

39.7.8 LCD Controller Enable Register

Name: LCDC_LCDEN

Address: 0xF0000020

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	PWMEN	DISPEN	SYNCEN	CLKEN

CLKEN: LCD Controller Pixel Clock Enable

0: No effect

1: Pixel clock logical unit is activated.

SYNCEN: LCD Controller Horizontal and Vertical Synchronization Enable

0: No effect

1: Both horizontal and vertical synchronization (LCDVSYNC and LCDHSYNC) signals are generated.

DISPEN: LCD Controller DISP Signal Enable

0: No effect

1: LCDDISP signal is generated.

PWMEN: LCD Controller Pulse Width Modulation Enable

0: No effect

1: PWM is enabled.

39.7.45 Overlay 1 Configuration Register 0

Name: LCDC_OVR1CFG0

Address: 0xF000016C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	LOCKDIS	ROTDIS	–	–	–	DLBO

7	6	5	4	3	2	1	0
–	–	BLEN		–	–	–	SIF

SIF: Source Interface

0: Base Layer data is retrieved through AHB interface 0.

1: Base Layer data is retrieved through AHB interface 1.

BLEN: AHB Burst Length

Value	Name	Description
0	AHB_BLEN_SINGLE	AHB Access is started as soon as there is enough space in the FIFO to store one data. SINGLE, INCR, INCR4, INCR8 and INCR16 bursts are used. INCR is used for a burst of 2 and 3 beats.
1	AHB_BLEN_INCR4	AHB Access is started as soon as there is enough space in the FIFO to store a total amount of 4 data. An AHB INCR4 Burst is used. SINGLE, INCR and INCR4 bursts are used. INCR is used for a burst of 2 and 3 beats.
2	AHB_BLEN_INCR8	AHB Access is started as soon as there is enough space in the FIFO to store a total amount of 8 data. An AHB INCR8 Burst is used. SINGLE, INCR, INCR4 and INCR8 bursts are used. INCR is used for a burst of 2 and 3 beats.
3	AHB_BLEN_INCR16	AHB Access is started as soon as there is enough space in the FIFO to store a total amount of 16 data. An AHB INCR16 Burst is used. SINGLE, INCR, INCR4, INCR8 and INCR16 bursts are used. INCR is used for a burst of 2 and 3 beats.

DLBO: Defined Length Burst Only for Channel Bus Transaction

0: Undefined length INCR burst is used for a burst of 2 and 3 beats.

1: Only Defined Length burst is used (SINGLE, INCR4, INCR8 and INCR16).

ROTDIS: Hardware Rotation Optimization Disable

0: Rotation optimization is enabled.

1: Rotation optimization is disabled.

LOCKDIS: Hardware Rotation Lock Disable

0: AHB lock signal is asserted when a rotation is performed.

1: AHB lock signal is cleared when a rotation is performed.

40.8.69 GMAC Frames Received Register

Name: GMAC_FR

Address: 0xF8008158

Access: Read-only

31	30	29	28	27	26	25	24
FRX							

23	22	21	20	19	18	17	16
FRX							

15	14	13	12	11	10	9	8
FRX							

7	6	5	4	3	2	1	0
FRX							

FRX: Frames Received without Error

Frames received without error. This register counts the number of frames successfully received. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

43.7.10 CLASSD Write Protection Mode Register

Name: CLASSD_WPMR

Address: 0xFC0480E4

Access: Read/Write

31	30	29	28	27	26	25	24
WPKEY							
23	22	21	20	19	18	17	16
WPKEY							
15	14	13	12	11	10	9	8
WPKEY							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPEN

WPEN: Write Protection Enable

0: Disables the write protection if WPKEY corresponds to 0x434C44 (“CLD” in ASCII).

1: Enables the write protection if WPKEY corresponds to 0x434C44 (“CLD” in ASCII).

See Section 43.6.7 “Register Write Protection” for the list of registers that can be write-protected.

WPKEY: Write Protection Key

Value	Name	Description
0x434C44	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

RXFPTEF: Receive FIFO Pointer Error Flag

0: No Receive FIFO pointer occurred

1: Receive FIFO pointer error occurred. Receiver must be reset

See Section 47.7.11.9 ”FIFO Pointer Error” for details.

TXFLOCK: Transmit FIFO Lock

0: The Transmit FIFO is not locked.

1: The Transmit FIFO is locked.

RXFTHF2: Receive FIFO Threshold Flag 2 (cleared by writing the FLEX_US_CR.RSTSTA bit)

0: Number of unread data in Receive FIFO is above RXFTHRES threshold.

1: Number of unread data in Receive FIFO has reached RXFTHRES2 threshold since the last RSTSTA command was issued.

49.8.9 SPI Interrupt Enable Register

Name: SPI_IER

Address: 0xF8000014 (0), 0xFC000014 (1)

Access: Write-only

31	30	29	28	27	26	25	24
RXFPTEF	TXFPTEF	RXFTHF	RXFFF	RXFEF	TXFTHF	TXFFF	TXFEF
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	CMP	UNDES	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
–	–	–	–	OVRES	MODF	TDRE	RDRF

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

RDRF: Receive Data Register Full Interrupt Enable

TDRE: SPI Transmit Data Register Empty Interrupt Enable

MODF: Mode Fault Error Interrupt Enable

OVRES: Overrun Error Interrupt Enable

NSSR: NSS Rising Interrupt Enable

TXEMPTY: Transmission Registers Empty Enable

UNDES: Underrun Error Interrupt Enable

CMP: Comparison Interrupt Enable

TXFEF: TXFEF Interrupt Enable

TXFFF: TXFFF Interrupt Enable

TXFTHF: TXFTHF Interrupt Enable

RXFEF: RXFEF Interrupt Enable

RXFFF: RXFFF Interrupt Enable

RXFTHF: RXFTHF Interrupt Enable

TXFPTEF: TXFPTEF Interrupt Enable

RXFPTEF: RXFPTEF Interrupt Enable

Example 5:

Instruction in Single-bit SPI, with address in Dual SPI, without option, with data write in Dual SPI.

Command: BYTE/PAGE PROGRAM (02h)

- Write 0x0000_0002 in QSPI_ICR.
- Write 0x0000_30B3 in QSPI_IFR.
- Read QSPI_IFR (dummy read) to synchronize system bus accesses.
- Write data in the QSPI system bus memory space (0x9000_00000-0x9800_00000/0XD000_0000--0XD800_0000).
  The address of the first system bus write access is sent in the instruction frame.
  The address of the next system bus write accesses is not used.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 50-15: Instruction Transmission Waveform 5

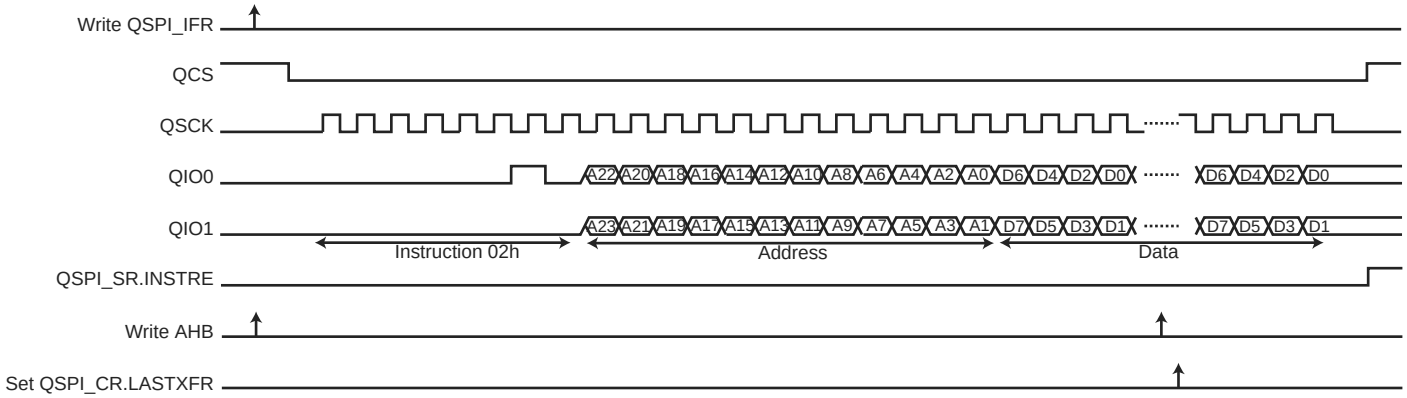


Table 52-18: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x410	Histogram Entry 0	ISC_HIS_ENTRY0	Read-only	0x00000000
...	...	...	...	...
0xBFC	Histogram Entry 511	ISC_HIS_ENTRY511	Read-only	0x00000000

52.6.36 ISC Color Space Conversion YB OY Register

Name: ISC_CSC_YB_OY

Address: 0xF00083A0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	YOFST		

23	22	21	20	19	18	17	16
YOFST							

15	14	13	12	11	10	9	8
–	–	–	–	YBGAIN			

7	6	5	4	3	2	1	0
YBGAIN							

YBGAIN: Blue Gain for Luminance Component (12 bits signed 1:3:8)

YOFST: Luminance Offset (11 bits signed 1:10:0)

FDOE: CAN FD Operation Enable (read/write, write protection)

0 (DISABLED): FD operation disabled.

1 (ENABLED): FD operation enabled.

BRSE: Bit Rate Switching Enable (read/write, write protection)

0 (DISABLED): Bit rate switching for transmissions disabled.

1 (ENABLED): Bit rate switching for transmissions enabled.

PXHD: Protocol Exception Event Handling (read/write, write protection)

0: Protocol exception handling enabled.

1: Protocol exception handling disabled.

EFBI: Edge Filtering during Bus Integration (read/write, write protection)

0: Edge filtering is disabled.

1: Edge filtering is enabled. Two consecutive dominant tq required to detect an edge for hard synchronization.

TXP: Transmit Pause (read/write, write protection)

If this bit is set, the MCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 53.5.5).

0: Transmit pause disabled.

1: Transmit pause enabled.

53.6.44 MCAN Transmit Buffer Cancellation Finished Interrupt Enable

Name: MCAN_TXBCIE

Address: 0xF80540E4 (0), 0xFC0500E4 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
23	22	21	20	19	18	17	16
CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
15	14	13	12	11	10	9	8
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
7	6	5	4	3	2	1	0
CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0

CFIEx: Cancellation Finished Interrupt Enable for Transmit Buffer x

Each Transmit Buffer has its own Cancellation Finished Interrupt Enable bit.

0: Cancellation finished interrupt disabled.

1: Cancellation finished interrupt enabled.

56.7.10 PWM DMA Register

Name: PWM_DMAR

Address: 0xF802C024

Access: Write- only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
DMADUTY							

15	14	13	12	11	10	9	8
DMADUTY							

7	6	5	4	3	2	1	0
DMADUTY							

Only the first 16 bits (channel counter size) are significant.

DMADUTY: Duty-Cycle Holding Register for DMA Access

Each write access to PWM_DMAR sequentially updates the CDTY field of PWM_CDTYx with DMADUTY (only for channel configured as synchronous). See “Method 3: Automatic write of duty-cycle values and automatic trigger of the update” .

5. Write the data to be encrypted/decrypted in the authorized Input Data Registers (refer to Table 59-2).

Table 59-2: Authorized Input Data Registers

Operating Mode	Input Data Registers to Write
ECB	All
CBC	All
CTR	All

6. Set the START bit in the AESB Control Register (AESB_CR) to begin the encryption or decryption process.
7. When processing is complete, the DATRDY bit in the AESB Interrupt Status Register (AESB_ISR) raises. If an interrupt has been enabled by setting the DATRDY bit in AESB_IER, the interrupt line of the AESB is activated.
8. When the software reads one of the Output Data Registers (AESB_ODATARx), the AESB_ISR.DATRDY bit is automatically cleared.

59.3.3.2 Auto Mode

Auto mode is similar to Manual mode, except that in Auto mode, as soon as the correct number of Input Data registers is written, processing starts automatically without any action in the Control Register.

59.3.4 Last Output Data Mode

Last Output Data mode is used to generate cryptographic checksums on data (MAC) by means of a cipher block chaining encryption algorithm (the CBC-MAC algorithm for example).

After each end of encryption/decryption, the output data are available on the output data registers for Manual and Auto modes.

The Last Output Data (LOD) bit in AESB_MR allows retrieval of only the last data of several encryption/decryption processes.

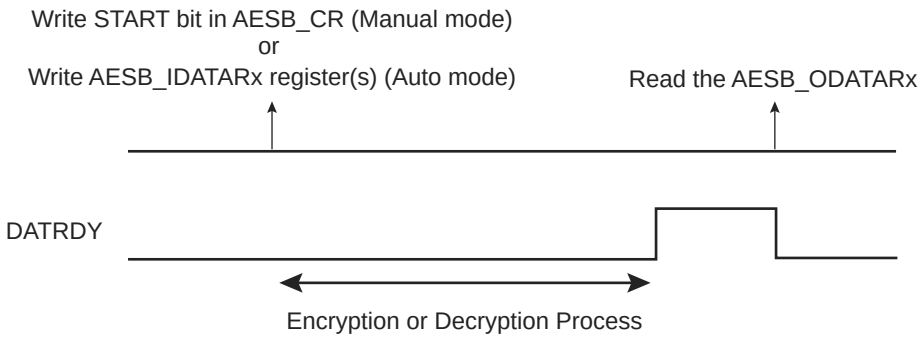
Those data are only available on the Output Data Registers (AESB_ODATARx).

59.3.5 Manual and Auto Modes

59.3.5.1 If AESB_MR.LOD = 0

The AESB_ISR.DATRDY bit is cleared when at least one of the Output Data Registers is read (refer to Figure 59-1).

Figure 59-1: Manual and Auto Modes with AESB_MR.LOD = 0



If the user does not want to read the output data registers between each encryption/decryption, the AESB_ISR.DATRDY bit will not be cleared. If the AESB_ISR.DATRDY bit is not cleared, the user cannot know the end of the following encryptions/decryptions.

59.3.5.2 If AESB_MR.LOD = 1

The AESB_ISR.DATRDY bit is cleared when at least one Input Data Register is written, so before the start of a new transfer (refer to Figure 59-2). No more Output Data Register reads are necessary between consecutive encryptions/decryptions.

60.5.18 AES Byte Counter Register

Name: AES_BCNT

Address: 0xF002C0B4

Access: Read/Write

31	30	29	28	27	26	25	24
BCNT							
23	22	21	20	19	18	17	16
BCNT							
15	14	13	12	11	10	9	8
BCNT							
7	6	5	4	3	2	1	0
BCNT							

BCNT: Auto Padding Byte Counter

Auto padding byte counter value. BCNT must be greater than 0.

Table 68-1: Power Supply Connections (Continued)

Signal Name	Recommended Pin Connection	Description
VDDFUSE	2.25V to 2.75V Decoupling capacitor (100 nF)(1)(2)	Powers the fuse box for programming. VDDFUSE must not be left floating.
VDDAUDIOPLL	3.0V to 3.6V Decoupling capacitor (100 nF)(1)(2)	Powers the Audio PLL.
GNDCORE	Core Chip ground	GNDCORE pins are common to VDDCORE pins. GNDCORE pins should be connected as shortly as possible to the system ground plane.
GNDPLLA	PLLA cell ground	GNDPLL pin is provided for VDDPLLA pins. GNDPLL pin should be connected as shortly as possible to the system ground plane.
GNDIODDR	DDR2/LPDDR1/LPDDR2/DDR3/LPDDR3 interface I/O lines ground	GNDIODDR pins should be connected as shortly as possible to the system ground plane.
GNDISC	VDDISC ground	GNDISC pins are common to VDDISC pins. GNDISC pins should be connected as shortly as possible to the system ground plane.
GNDIOP0,1,2	Peripherals and ISC I/O lines ground	GNDIOPx pins are common to VDDIOPx pins. GNDIOP pins should be connected as shortly as possible to the system ground plane.
GNDBU	Backup ground	GNDBU pin is provided for VDDBU pins. GNDBU pin should be connected as shortly as possible to the system ground plane.
GNDUTMIC	VDDUTMIC and VDDHSIC ground	GNDUTMIC pins are common to VDDUTMIC and VDDHSIC pins. GNDUTMIC pins should be connected as shortly as possible to the system ground plane.
GNDUTMII	UDPHS and UHPHS UTMI+ Core and Interface, and PLL UTMI ground	GNDUTMII pins are common to VDDUTMII and VDDUTMIC pins. GNDUTMII pins should be connected as shortly as possible to the system ground plane.
GNDOSC	Oscillator ground	GNDOSC pin is provided for VDDOSC pins. GNDOSC pin should be connected as shortly as possible to the system ground plane.
GNDSDMMC	SDMMC ground	SDMMC pins are common to VDDSDMMC pins. GNDSDMMC pins should be connected as shortly as possible to the system ground plane.
GNDANA	Analog ground	GNDANA pins are common to VDDANA pins. GNDANA pins should be connected as shortly as possible to the system ground plane.
GNDFUSE	Fuse box ground	GNDFUSE pins are common to VDDFUSE pins. GNDFUSE pins should be connected as shortly as possible to the system ground plane.