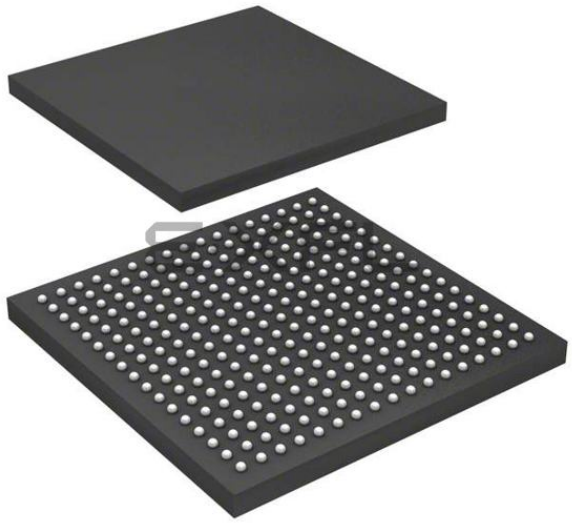

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26b-cu

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)(1)(2)
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
G5	–	–	VDDISC	GPIO	PC23	I/O	–	–	A	LCDDAT19	O	2	PIO, I, PU, ST
									B	GCOL	I	1	
									C	ISC_HSYNC	I	1	
									F	A12	O	2	
H1	–	–	VDDISC	GPIO_CLK	PC24	I/O	–	–	A	LCDDAT20	O	2	PIO, I, PU, ST
									B	GRX2	I	1	
									C	ISC_MCK	O	1	
									F	A13	O	2	
H5	–	–	VDDISC	GPIO	PC25	I/O	–	–	A	LCDDAT21	O	2	PIO, I, PU, ST
									B	GRX3	I	1	
									C	ISC_FIELD	I	1	
									F	A14	O	2	
J9	–	–	VDDIOP2	GPIO	PC26	I/O	–	–	A	LCDDAT22	O	2	PIO, I, PU, ST
									B	GTX2	O	1	
									D	CANTX1	O	1	
									F	A15	O	2	
H9	–	–	VDDIOP2	GPIO	PC27	I/O	–	–	A	LCDDAT23	O	2	PIO, I, PU, ST
									B	GTX3	O	1	
									C	PCK1	O	2	
									D	CANRX1	I	1	
									E	TWD0	I/O	2	
									F	A16	O	2	
E8	–	–	VDDIOP2	GPIO	PC28	I/O	–	–	A	LCDPWM	O	2	PIO, I, PU, ST
									B	FLEXCOM4_IO0	I/O	1	
									C	PCK2	O	1	
									E	TWCK0	I/O	2	
									F	A17	O	2	
G8	–	–	VDDIOP2	GPIO	PC29	I/O	–	–	A	LCDDISP	O	2	PIO, I, PU, ST
									B	FLEXCOM4_IO1	I/O	1	
									F	A18	O	2	
F8	–	–	VDDIOP2	GPIO	PC30	I/O	–	–	A	LCDVSYNC	O	2	PIO, I, PU, ST
									B	FLEXCOM4_IO2	I/O	1	
									F	A19	O	2	
D8	–	–	VDDIOP2	GPIO	PC31	I/O	–	–	A	LCDHSYNC	O	2	PIO, I, PU, ST
									B	FLEXCOM4_IO3	O	1	
									C	URXD3	I	2	
									F	A20	O	2	

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)(1)(2)
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
G10	E9	–	VDDIOP2	GPIO_CLK	PD0	I/O	–	–	A	LCDPCK	O	2	PIO, I, PU, ST
									B	FLEXCOM4_IO4	O	1	
									C	UTXD3	O	2	
									D	GTSUCOMP	O	2	
									F	A23	O	2	
E10	F8	–	VDDIOP2	GPIO	PD1	I/O	–	–	A	LCDDEN	O	2	PIO, I, PU, ST
									D	GRXCK	I	2	
									F	A24	O	2	
G9	F9	–	VDDIOP2	GPIO_CLK	PD2	I/O	–	–	A	URXD1	I	1	PIO, I, PU, ST
									D	GTXER	O	2	
									E	ISC_MCK	O	2	
									F	A25	O	2	
K1	J4	–	VDDANA	GPIO_AD	PD3	I/O	PTC_X0	–	A	UTXD1	O	1	PIO, I, PU, ST
									B	FIQ	I	2	
									D	GCRS	I	2	
									E	ISC_D11	I	2	
									F	NWAIT	I	2	
J6	H6	–	VDDANA	GPIO_AD	PD4	I/O	PTC_X1	–	A	TWD1	I/O	2	PIO, I, PU, ST
									B	URXD2	I	1	
									D	GCOL	I	2	
									E	ISC_D10	I	2	
									F	NCS0	O	2	
J4	H1	–	VDDANA	GPIO_AD	PD5	I/O	PTC_X2	–	A	TWCK1	I/O	2	PIO, I, PU, ST
									B	UTXD2	O	1	
									D	GRX2	I	2	
									E	ISC_D9	I	2	
									F	NCS1	O	2	
J2	G4	–	VDDANA	GPIO_AD	PD6	I/O	PTC_X3	–	A	TCK	I	2	PIO, I, PU, ST
									B	PCK1	O	1	
									D	GRX3	I	2	
									E	ISC_D8	I	2	
									F	NCS2	O	2	
J7	H5	F5	VDDANA	GPIO_AD	PD7	I/O	PTC_X4	–	A	TDI	I	2	PIO, I, PU, ST
									C	UTMI_RXVAL	O	1	
									D	GTX2	O	2	
									E	ISC_D0	I	2	
									F	NWR1/NBS1	O	2	

19.3.15 QSPI Clock Pad Supply Select Register

Name: QSPICLK_REG

Address: 0xF8030094

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SUP_SEL

SUP_SEL: Supply Selection

0: 1.8V supply selected.

1: 3.3V supply selected.

24.4 I/O Lines Description

Table 24-1: I/O Lines Description

Name	Description	Type
WKUP0	Wakeup inputs	Input
PIOBU 0-7	Wakeup inputs, WKUP(2-9)	Input
SHDN	Shutdown output	Output

24.5 Product Dependencies

24.5.1 Power Management

The Shutdown Controller is continuously clocked by the Slow Clock (SLCK). The Power Management Controller has no effect on the behavior of the Shutdown Controller.

24.6 Functional Description

The Shutdown Controller manages the main power supply. To do so, it is supplied with VDDBU and manages wakeup input pins and one output pin, SHDN.

A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies of the system, and especially VDDCORE and/or VDDIO. The wakeup inputs (WKUPn) connect to any push-buttons or signal that wake up the system.

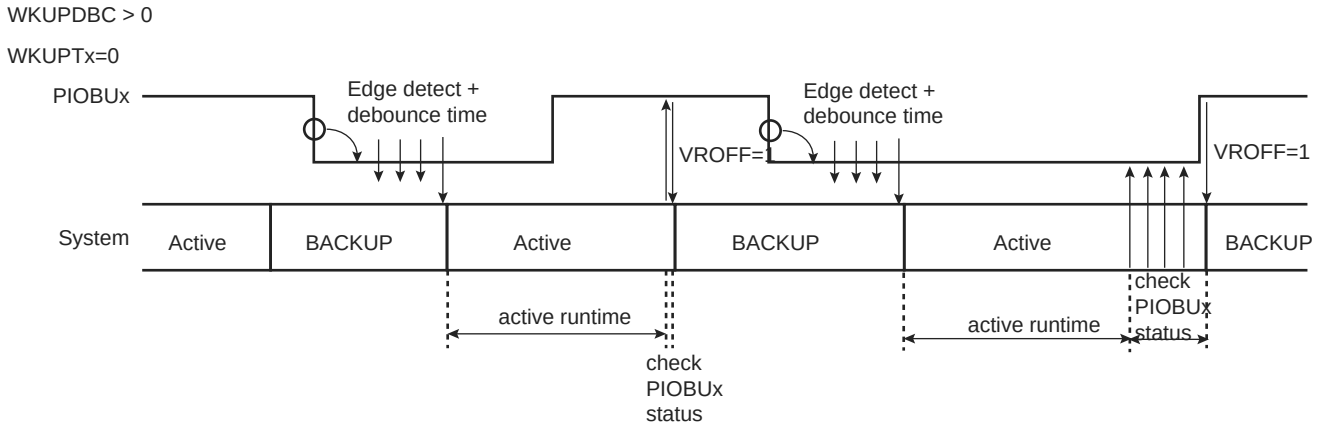
The software is able to control the pin SHDN by writing the Shutdown Control Register (SHDW_CR) with the bit SHDW at 1. The shutdown is taken into account only two slow clock cycles after the write of SHDW_CR. This register is password-protected and so the value written should contain the correct key for the command to be taken into account. As a result, the system should be powered down.

24.6.1 Wakeup Inputs

Any level change on a PIOBUx, WKUP pin, or Security Module event, can trigger a wakeup. Wakeup is configured in the Shutdown Mode Register (SHDW_MR) and Shutdown Wakeup Inputs Register (SHDW_WUIR). The transition detector can be programmed to detect either a positive or negative transition on any PIOBUx, WKUP pin. The detection can also be disabled. Programming is performed by enabling the Wakeup Input (WKUPENx bit) and defining the Wakeup Input Type (WKUPTx bit) in the SHDW_WUIR.

Moreover, a debouncing circuit can be programmed for PIOBUx, WKUP. The debouncing circuit filters pulses on PIOBUx, WKUP shorter than the programmed value in the WKUPDBC field in SHDW_MR. If the programmed level change is detected on a pin, a counter starts. When the counter reaches the value programmed in the corresponding field WKUPDBC, the SHDN pin is released. If a new input change is detected before the counter reaches the corresponding value, the counter is stopped and cleared. One counter is shared among all PIOBUx, WKUP inputs and all programmed level detection is merged into this counter. The WKUPISx bit of the Status Register (SHDW_SR) reports the detection of the programmed events on PIOBUx, WKUP with a reset after the read of SHDW_SR.

Figure 24-2: Entering and Exiting Backup Mode with a PIOBUx, WKUP Pin



26.6.14 RTC Interrupt Mask Register

Name: RTC_IMR

Address: 0xF80480D8

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	TDERR	CAL	TIM	SEC	ALR	ACK

ACK: Acknowledge Update Interrupt Mask

0: The acknowledge for update interrupt is disabled.

1: The acknowledge for update interrupt is enabled.

ALR: Alarm Interrupt Mask

0: The alarm interrupt is disabled.

1: The alarm interrupt is enabled.

SEC: Second Event Interrupt Mask

0: The second periodic interrupt is disabled.

1: The second periodic interrupt is enabled.

TIM: Time Event Interrupt Mask

0: The selected time event interrupt is disabled.

1: The selected time event interrupt is enabled.

If the RTC is configured in UTC mode, this bit is not relevant.

CAL: Calendar Event Interrupt Mask

0: The selected calendar event interrupt is disabled.

1: The selected calendar event interrupt is enabled.

If the RTC is configured in UTC mode, this bit is not relevant.

TDERR: Time and/or Date Error Mask

0: The time and/or date error event is disabled.

1: The time and/or date error event is enabled.

If the RTC is configured in UTC mode, this bit has no effect.

40.8.13 GMAC Interrupt Mask Register

Name: GMAC_IMR

Address: 0xF8008030

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	TSUTIMCOMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
23	22	21	20	19	18	17	16
PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR	–	–
15	14	13	12	11	10	9	8
EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR	–	–
7	6	5	4	3	2	1	0
TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS

The Interrupt Mask Register is a read-only register indicating which interrupts are masked. All bits are set at reset and can be reset individually by writing to the Interrupt Enable Register or set individually by writing to the Interrupt Disable Register. Having separate address locations for enable and disable saves the need for performing a read modify write when updating the Interrupt Mask Register.

For test purposes there is a write-only function to this register that allows the bits in the Interrupt Status Register to be set or cleared, regardless of the state of the mask register. A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

The following values are valid for all listed bit names of this register when read:

0: The corresponding interrupt is enabled.

1: The corresponding interrupt is not enabled.

MFS: Management Frame Sent

RCOMP: Receive Complete

RXUBR: RX Used Bit Read

TXUBR: TX Used Bit Read

TUR: Transmit Underrun

RLEX: Retry Limit Exceeded

TFC: Transmit Frame Corruption Due to AHB Error

TCOMP: Transmit Complete

ROVR: Receive Overrun

HRESP: HRESP Not OK

PFNZ: Pause Frame with Non-zero Pause Quantum Received

PTZ: Pause Time Zero

PFTR: Pause Frame Transmitted

EXINT: External Interrupt

DRQFR: PTP Delay Request Frame Received

SFR: PTP Sync Frame Received

DRQFT: PTP Delay Request Frame Transmitted

40.8.82 GMAC Jabbers Received Register

Name: GMAC_JR

Address: 0xF800818C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	JRX	

7	6	5	4	3	2	1	0
JRX							

JRX: Jabbers Received

The register counts the number of frames received exceeding 1518 bytes in length (1536 if bit 8 is set in Network Configuration Register) and have either a CRC error, an alignment error or a receive symbol error. See Section 40.8.2 ”GMAC Network Configuration Register”.

45.9.1 SSC Control Register

Name: SSC_CR

Address: 0xF8004000 (0), 0xFC004000 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
SWRST	–	–	–	–	–	TXDIS	TXEN
7	6	5	4	3	2	1	0
–	–	–	–	–	–	RXDIS	RXEN

RXEN: Receive Enable

0: No effect.

1: Enables Receive if RXDIS is not set.

RXDIS: Receive Disable

0: No effect.

1: Disables Receive. If a character is currently being received, disables at end of current character reception.

TXEN: Transmit Enable

0: No effect.

1: Enables Transmit if TXDIS is not set.

TXDIS: Transmit Disable

0: No effect.

1: Disables Transmit. If a character is currently being transmitted, disables at end of current character transmission.

SWRST: Software Reset

0: No effect.

1: Performs a software reset. Has priority on any other bit in SSC_CR.

45.9.3 SSC Receive Clock Mode Register

Name: SSC_RCMR

Address: 0xF8004010 (0), 0xFC004010 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
PERIOD							

23	22	21	20	19	18	17	16
STTDLY							

15	14	13	12	11	10	9	8
–	–	–	STOP	START			

7	6	5	4	3	2	1	0
CKG		CKI	CKO			CKS	

This register can only be written if the WPEN bit is cleared in the SSC Write Protection Mode Register.

CKS: Receive Clock Selection

Value	Name	Description
0	MCK	Divided Clock
1	TK	TK Clock signal
2	RK	RK pin

CKO: Receive Clock Output Mode Selection

Value	Name	Description
0	NONE	None, RK pin is an input
1	CONTINUOUS	Continuous Receive Clock, RK pin is an output
2	TRANSFER	Receive Clock only during data transfers, RK pin is an output

CKI: Receive Clock Inversion

0: The data inputs (Data and Frame Sync signals) are sampled on Receive Clock falling edge. The Frame Sync signal output is shifted out on Receive Clock rising edge.

1: The data inputs (Data and Frame Sync signals) are sampled on Receive Clock rising edge. The Frame Sync signal output is shifted out on Receive Clock falling edge.

CKI affects only the Receive Clock and not the output clock signal.

CKG: Receive Clock Gating Selection

Value	Name	Description
0	CONTINUOUS	None
1	EN_RF_LOW	Receive Clock enabled only if RF Low
2	EN_RF_HIGH	Receive Clock enabled only if RF High

The node configuration is chosen by setting the USART_MODE field in the USART Mode Register (FLEX_US_MR):

- LIN master node (USART_MODE = 0xA)
- LIN slave node (USART_MODE = 0xB)

In order to avoid unpredictable behavior, any change of the LIN node configuration must be followed by a software reset of the transmitter and of the receiver (except the initial node configuration after a hardware reset). (See Section 47.7.9.3 ”Receiver and Transmitter Control”.)

47.7.9.2 Baud Rate Configuration

See Section 47.7.1.1 ”Baud Rate in Asynchronous Mode”.

- LIN master node: The baud rate is configured in FLEX_US_BRGR.
- LIN slave node: The initial baud rate is configured in FLEX_US_BRGR. This configuration is automatically copied in the LIN Baud Rate Register (FLEX_US_LINBRR) when writing FLEX_US_BRGR. After the synchronization procedure, the baud rate is updated in FLEX_US_LINBRR.

47.7.9.3 Receiver and Transmitter Control

See Section 47.7.2 ”Receiver and Transmitter Control”.

47.7.9.4 Character Transmission

See Section 47.7.3.1 ”Transmitter Operations”.

47.7.9.5 Character Reception

See Section 47.7.3.7 ”Receiver Operations”.

47.7.9.6 Header Transmission (Master Node Configuration)

All the LIN Frames start with a header which is sent by the master node and consists of a Synch Break Field, Synch Field and Identifier Field.

So in master node configuration, the frame handling starts with the sending of the header.

The header is transmitted as soon as the identifier is written in the LIN Identifier Register (FLEX_US_LINIR). At this moment the flag TXRDY falls.

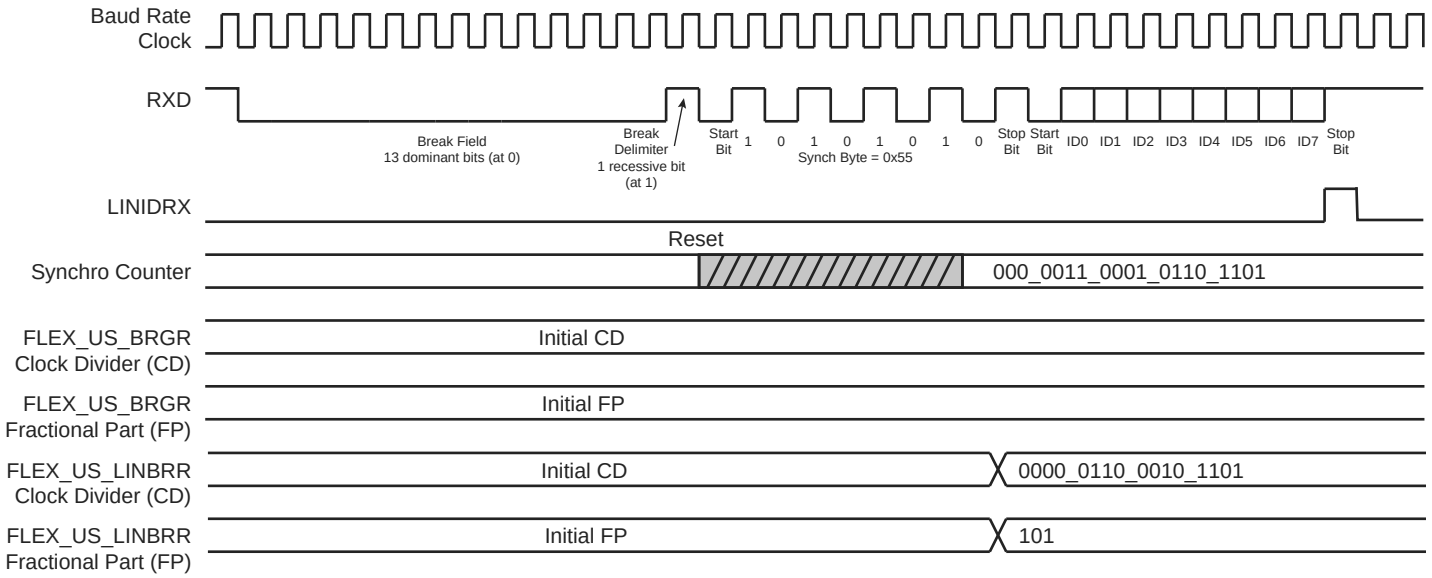
The Break Field, the Synch Field and the Identifier Field are sent automatically one after the other.

The Break Field consists of 13 dominant bits and 1 recessive bit, the Synch Field is the character 0x55 and the Identifier corresponds to the character written in the LIN Identifier Register (FLEX_US_LINIR). The Identifier parity bits can be automatically computed and sent (see **Section 47.7.9.9 “Identifier Parity”**).

The flag TXRDY rises when the identifier character is transferred into the shift register of the transmitter.

As soon as the Synch Break Field is transmitted, the FLEX_US_CSR.LINBK flag bit is set. Likewise, as soon as the Identifier Field is sent, the FLEX_US_CSR.LINID flag bit is set. These flags are reset by writing a one to the FLEX_US_CR.RSTSTA bit.

Figure 47-44: Slave Node Synchronization



The synchronization accuracy depends on several parameters:

- The nominal clock frequency (f_{Nom}) (the theoretical slave node clock frequency)
- The baud rate
- The oversampling (OVER = 0 => 16X or OVER = 1 => 8X)

The following formula is used to compute the deviation of the slave bit rate relative to the master bit rate after synchronization (f_{SLAVE} is the real slave node clock frequency).

$$\text{Baud rate deviation} = \left(100 \times \frac{[\alpha \times 8 \times (2 - \text{Over}) + \beta] \times \text{Baud rate}}{8 \times f_{SLAVE}}\right)\%$$

$$\text{Baud rate deviation} = \left(100 \times \frac{[\alpha \times 8 \times (2 - \text{Over}) + \beta] \times \text{Baud rate}}{8 \times \left(\frac{f_{TOL\_UNSYNCH}}{100}\right) \times f_{Nom}}\right)\%$$

$$-0.5 \le \alpha \le +0.5 \quad -1 < \beta < +1$$

$f_{TOL\_UNSYNCH}$ is the deviation of the real slave node clock from the nominal clock frequency. The LIN Standard imposes that it must not exceed ±15%. The LIN Standard imposes also that for communication between two nodes, their bit rate must not differ by more than ±2%. This means that the baud rate deviation must not exceed ±1%.

Therefore, a minimum value for the nominal clock frequency can be computed as follows:

$$f_{Nom}(\text{min}) = \left(100 \times \frac{[0.5 \times 8 \times (2 - \text{Over}) + 1] \times \text{Baud rate}}{8 \times \left(\frac{-15}{100} + 1\right) \times 1\%}\right)\text{Hz}$$

Examples:

- Baud rate = 20 kbit/s, OVER = 0 (Oversampling 16X) => f_{Nom}(min) = 2.64 MHz
- Baud rate = 20 kbit/s, OVER = 1 (Oversampling 8X) => f_{Nom}(min) = 1.47 MHz
- Baud rate = 1 kbit/s, OVER = 0 (Oversampling 16X) => f_{Nom}(min) = 132 kHz
- Baud rate = 1 kbit/s, OVER = 1 (Oversampling 8X) => f_{Nom}(min) = 74 kHz

47.8.3.2 Master Mode Flowchart

Figure 47-69: Master Mode

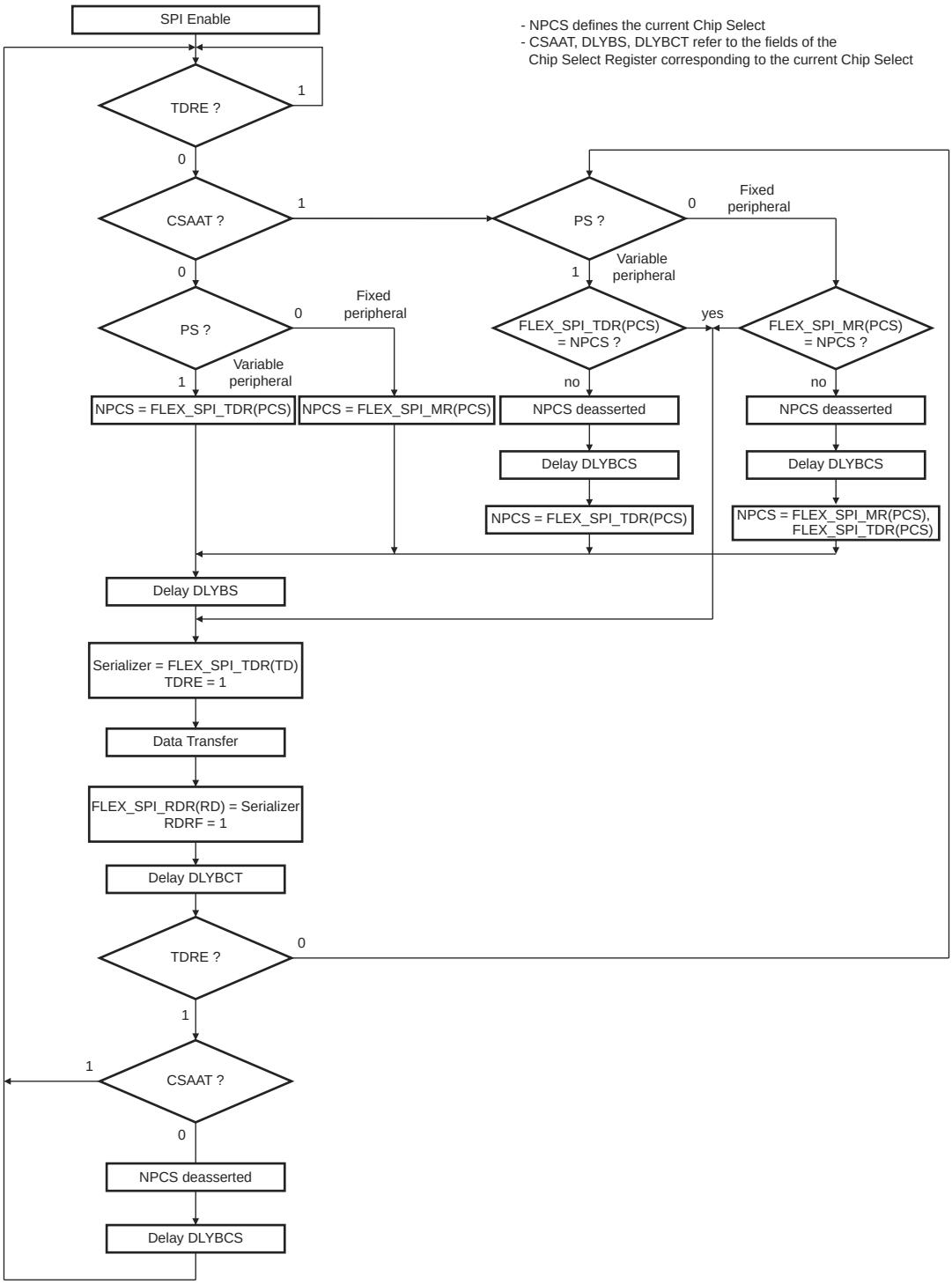
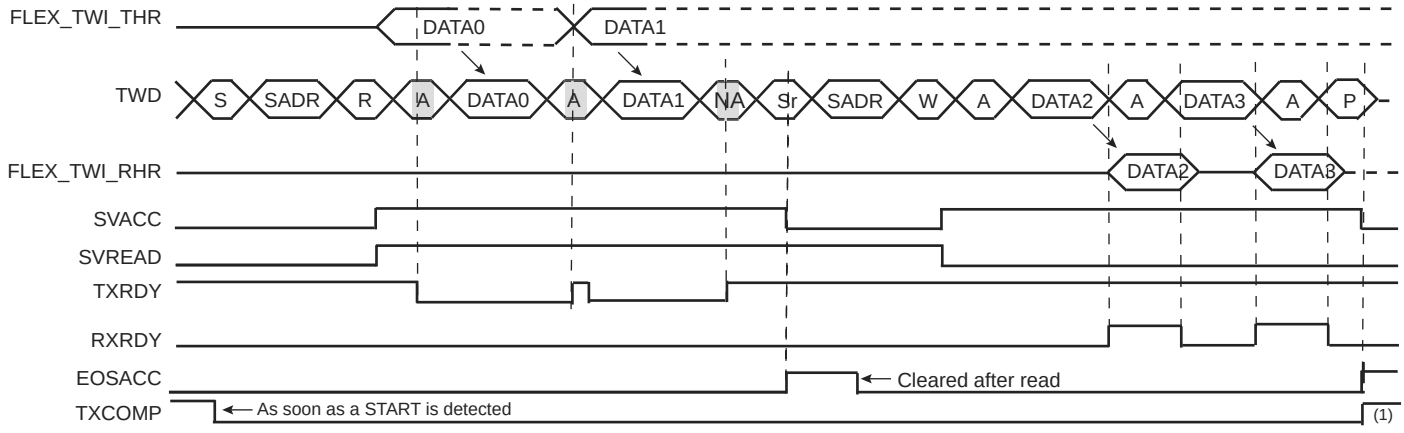


Figure 47-118: Repeated Start and Reversal from Read Mode to Write Mode

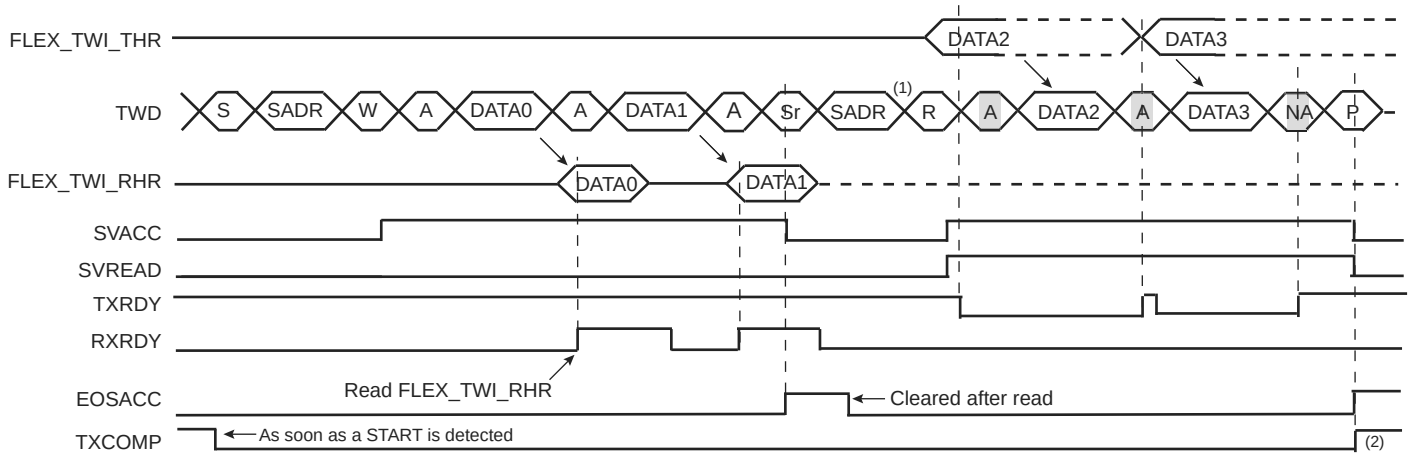


Note:
1. TXCOMP is only set at the end of the transmission because after the repeated start, SADR is detected again.

Reversal of Write to Read

The master initiates the communication by a write command and finishes it by a read command. Figure 47-119 describes the repeated start and the reversal from Write mode to Read mode.

Figure 47-119: Repeated Start and Reversal from Write Mode to Read Mode



Notes:
1. In this case, if FLEX_TWI_THR has not been written at the end of the read command, the clock is automatically stretched before the ACK.
2. TXCOMP is only set at the end of the transmission because after the repeated start, SADR is detected again.

- SMBus Mode

SMBus mode is enabled when the FLEX_TWI_CR.SMEN bit is written to one. SMBus mode operation is similar to I²C operation with the following exceptions:

1. Only 7-bit addressing can be used.
2. The SMBus standard describes a set of timeout values to ensure progress and throughput on the bus. These timeout values must be programmed into FLEX_TWI_SMBTR.
3. Transmissions can optionally include a CRC byte, called Packet Error Check (PEC).
4. A set of addresses have been reserved for protocol handling, such as alert response address (ARA) and host header (HH) address. Address matching on these addresses can be enabled by configuring FLEX_TWI_CR appropriately.

Packet Error Checking

Each SMBus transfer can optionally end with a CRC byte, called the PEC byte. Writing the FLEX_TWI_CR.PECEN bit to one will send/check the FLEX_TWI_ACR.PEC field in the current transfer. The PEC generator is always updated on every bit transmitted or received, so that PEC handling on following linked transfers will be correct.

47.10.36 USART FIFO Level Register

Name: FLEX_US_FLR

Address: 0xF80342A4 (0), 0xF80382A4 (1), 0xFC0102A4 (2), 0xFC0142A4 (3), 0xFC0182A4 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	RXFL					
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	TXFL					

TXFL: Transmit FIFO Level

0: There is no data in the Transmit FIFO

1–32: Indicates the number of data in the Transmit FIFO

RXFL: Receive FIFO Level

0: There is no unread data in the Receive FIFO

1–32: Indicates the number of unread data in the Receive FIFO

47.10.45 SPI Receive Data Register

Name: FLEX_SPI_RDR

Address: 0xF8034408 (0), 0xF8038408 (1), 0xFC010408 (2), 0xFC014408 (3), 0xFC018408 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	PCS			
15	14	13	12	11	10	9	8
RD							
7	6	5	4	3	2	1	0
RD							

Note: If FIFO is enabled (FLEX_SPI_CR.FIFOEN) and FLEX_SPI_FMR.RXRDYM = 0, see Section 47.8.7.6 “SPI Single Data Mode” for details.

RD: Receive Data

Data received by the SPI Interface is stored in this register in a right-justified format. Unused bits are read as zero.

PCS: Peripheral Chip Select

In Master mode only, these bits indicate the value on the NPCS pins at the end of a transfer. Otherwise, these bits are read as zero.

Note: When using Variable Peripheral Select mode (FLEX_SPI_MR.PS = 1), it is mandatory to set the FLEX_SPI_MR.WDRBT bit to 1 if the PCS field must be processed in FLEX_SPI_RDR.

47.10.74 TWI Transmit Holding Register (FIFO Enabled)

Name: FLEX_TWI_THR (FIFO_ENABLED)

Address: 0xF8034634 (0), 0xF8038634 (1), 0xFC010634 (2), 0xFC014634 (3), 0xFC018634 (4)

Access: Write-only

31	30	29	28	27	26	25	24
TXDATA3							
23	22	21	20	19	18	17	16
TXDATA2							
15	14	13	12	11	10	9	8
TXDATA1							
7	6	5	4	3	2	1	0
TXDATA0							

Note: If FIFO is enabled (FLEX_US_CR.FIFOEN bit) and FLEX_TWI_FMR.TXRDYM > 0, see Section 47.9.6.8 “TWI Multiple Data Mode” for details.

TXDATA0: Master or Slave Transmit Holding Data 0

TXDATA1: Master or Slave Transmit Holding Data 1

TXDATA2: Master or Slave Transmit Holding Data 2

TXDATA3: Master or Slave Transmit Holding Data 3

50.7.4 QSPI Transmit Data Register

Name: QSPI_TDR

Address: 0xF002000C (0), 0xF002400C (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
TD							
7	6	5	4	3	2	1	0
TD							

TD: Transmit Data

Data to be transmitted by the QSPI is stored in this register. Information to be transmitted must be written to the Transmit Data register in a right-justified format.

52.6.15 ISC White Balance Control Register

Name: ISC_WB_CTRL

Address: 0xF0008058

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ENABLE

ENABLE: White Balance Enable

0: The white balance is disabled.

1: The white balance is enabled.

52.6.35 ISC Color Space Conversion YR YG Register

Name: ISC_CSC_YR_YG

Address: 0xF000839C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	YGGAIN			

23	22	21	20	19	18	17	16
YGGAIN							

15	14	13	12	11	10	9	8
–	–	–	–	YRGAIN			

7	6	5	4	3	2	1	0
YRGAIN							

YRGAIN: Reg Gain for Luminance (signed 12 bits 1:3:8)

YGGAIN: Green Gain for Luminance (signed 12 bits 1:3:8)

71.2.8 Quad I/O Serial Peripheral Interface (QSPI)

Issue: QSPI hangs with long DLYCS

QSPI hangs if a command is written to any QSPI register during the DLYCS delay. There is no status bit to flag the end of the delay.

Workaround: The field DLYCS defines a minimum period for which Chip Select is deasserted, required by some memories. This delay is generally < 60 ns and comprises internal execution time, arbitration and latencies. Thus, DLYCS must be configured to be slightly higher than the value specified for the slave device. The software must wait for this same period of time plus an additional delay before a command can be written to the QSPI.

71.2.9 Master/Processor Clock Prescaler

Issue: Change of the field PMC_MCKR.PRES is not allowed if Master/Processor Clock Prescaler frequency is too high

PMC_MCKR.PRES cannot be changed if the clock applied to the Master/Processor Clock Prescaler (see “Master Clock Controller”, in Section 33. “Power Management Controller (PMC)”) is greater than 312 MHz (VDDCORE[1.1, 1.32]) and 394 MHz (VDDCORE[1.2, 1.32]).

Workaround:

1. Set PMC_MCKR.CSS to MAIN_CLK.
2. Set PMC_MCKR.PRES to the required value.
3. Change PMC_MCKR.CSS to the new clock source (PLLA_CLK, UPLLCK).

71.2.10 Master CAN-FD Controller (MCAN)

Issue: Flexible data rate feature does not support CRC

CAN-FD peripheral (BOSCH V320) does not support the CRC scheme which includes the stuff bit count introduced by the ISO standardization committee.

CAN 2.0 operation is not impacted.

Workaround: None.

71.2.11 MCAN Interrupt MCAN_IR.MRAF

Issue: Needless activation of interrupt MCAN_IR.MRAF

During frame reception while the MCAN is in Error Passive state and the Receive Error Counter has the value MCAN_ECR.REC = 127, it may happen that MCAN_IR.MRAF is set although there was no Message RAM access failure. If MCAN_IR.MRAF is enabled, an interrupt to the Host CPU is generated.

Workaround: The Message RAM Access Failure interrupt routine needs to check whether MCAN_ECR.RP = ’1’ and MCAN_ECR.REC = 127. In this case, reset MCAN_IR.MRAF. No further action is required.