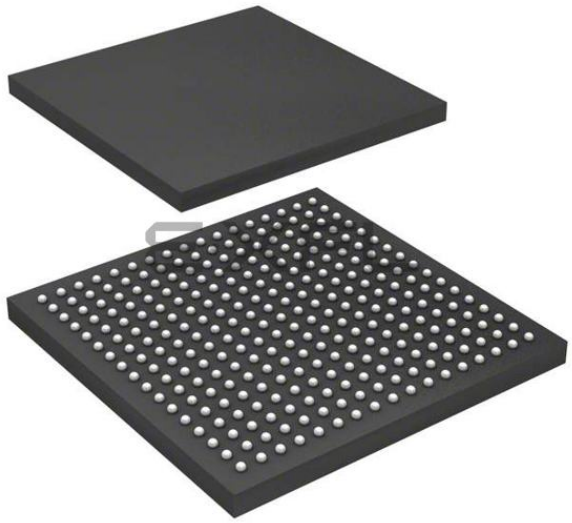

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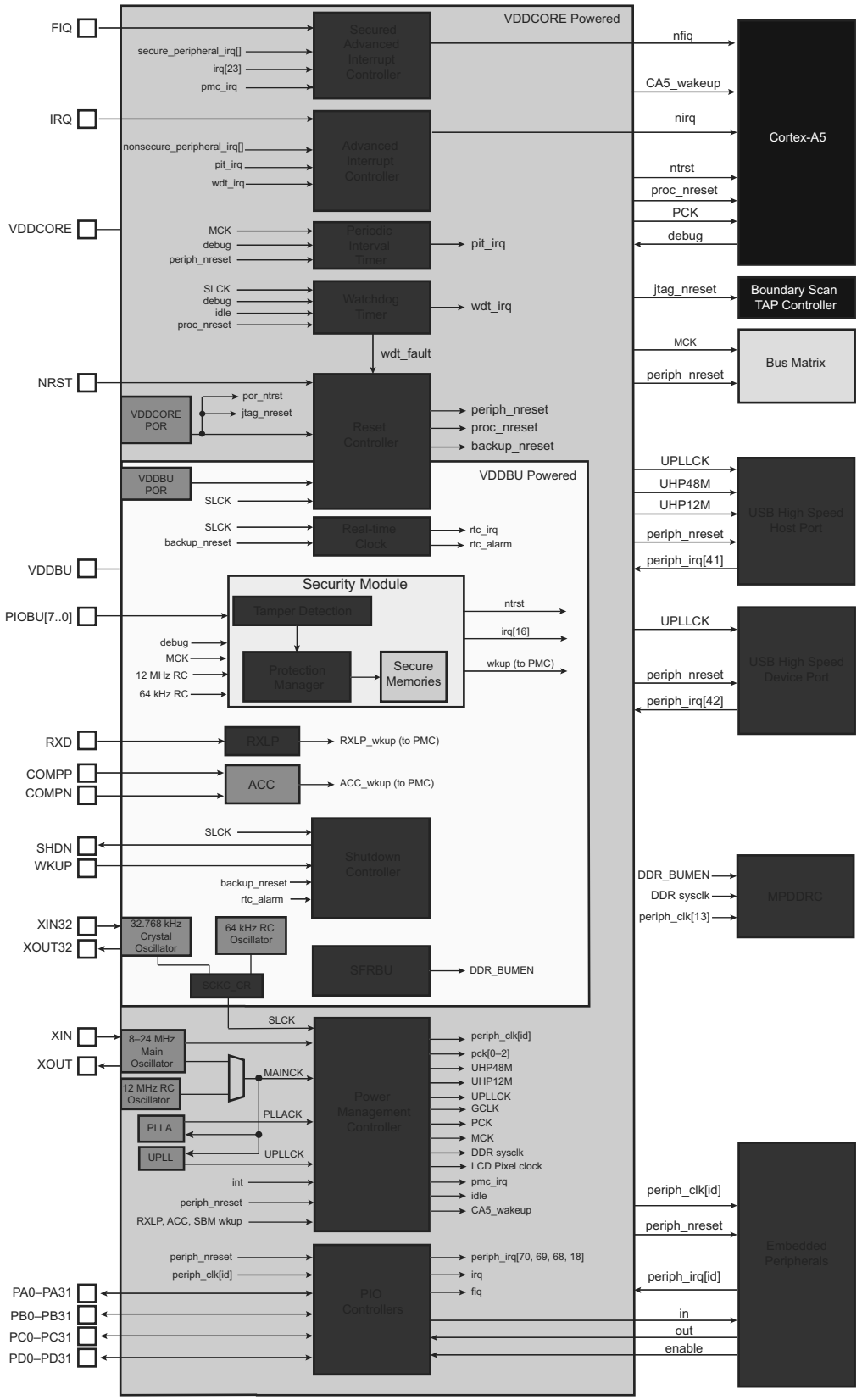
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26c-cnr

Figure 10-1: System Controller Block Diagram



14.5.10 L2CC Event Counter 1 Value Register

Name: L2CC_EVR1

Address: 0x00A0020C

Access: Read/Write

31	30	29	28	27	26	25	24
VALUE							

23	22	21	20	19	18	17	16
VALUE							

15	14	13	12	11	10	9	8
VALUE							

7	6	5	4	3	2	1	0
VALUE							

Note: Counter 1 must be disabled in the L2CC Event Counter 1 Configuration Register prior to any write access to this register.

VALUE: Event Counter Value

Value returns the number of instance of the selected event.

If a counter reaches its maximum value, it remains saturated at that value until it is reset.

14.5.23 L2CC Clean Invalidate Index Register

Name: L2CC_CIIR

Address: 0x00A007F8

Access: Read/Write

31	30	29	28	27	26	25	24
–	WAY			–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	IDX					

7	6	5	4	3	2	1	0
IDX			–	–	–	–	C

C: Cache Synchronization Status

0: No background operation is in progress. When written, must be zero.

1: A background operation is in progress.

IDX: Index Number

WAY: Way Number

34.7.15 Secure PIO Mask Register

Name: S_PIO_MSKRx [x=0..3]

Address: 0xFC039000 [0], 0xFC039040 [1], 0xFC039080 [2], 0xFC0390C0 [3]

Access: Read/Write

31	30	29	28	27	26	25	24
MSK31	MSK30	MSK29	MSK28	MSK27	MSK26	MSK25	MSK24
23	22	21	20	19	18	17	16
MSK23	MSK22	MSK21	MSK20	MSK19	MSK18	MSK17	MSK16
15	14	13	12	11	10	9	8
MSK15	MSK14	MSK13	MSK12	MSK11	MSK10	MSK9	MSK8
7	6	5	4	3	2	1	0
MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0

This register can only be written if the WPEN bit is cleared in the Secure PIO Write Protection Mode Register.

MSKy: PIO Line y Mask

These bits define the I/O lines to be configured when writing the Secure PIO Configuration Register.

0 (DISABLED): Writing the S_PIO_CFGRx, S_PIO_ODSRx or S_PIO_IOFRx does not affect the corresponding I/O line configuration.

1 (ENABLED): Writing the S_PIO_CFGRx, S_PIO_ODSRx or S_PIO_IOFRX updates the corresponding I/O line configuration.

36.6.2 DDR-SDRAM Address Mapping for 32-bit Memory Data Bus Width

Table 36-15: Sequential Mapping DDR-SDRAM Configuration Mapping: 2K Rows, 512/1024/2048 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					Bk[1:0]		Row[10:0]											Column[8:0]										M[1:0]	
				Bk[1:0]			Row[10:0]											Column[9:0]										M[1:0]	
			Bk[1:0]				Row[10:0]											Column[10:0]										M[1:0]	

Table 36-16: Interleaved Mapping DDR-SDRAM Configuration Mapping: 2K Rows, 512/1024/2048 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					Row[10:0]											Bk[1:0]		Column[8:0]										M[1:0]	
				Row[10:0]											Bk[1:0]			Column[9:0]										M[1:0]	
			Row[10:0]											Bk[1:0]				Column[10:0]										M[1:0]	

Table 36-17: Sequential Mapping DDR-SDRAM Configuration Mapping: 4K Rows, 256/512/1024/2048 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					Bk[1:0]		Row[11:0]												Column[7:0]									M[1:0]	
				Bk[1:0]			Row[11:0]											Column[8:0]									M[1:0]	
			Bk[1:0]				Row[11:0]											Column[9:0]									M[1:0]	
		Bk[1:0]					Row[11:0]											Column[10:0]									M[1:0]	

Table 36-18: Interleaved Mapping DDR-SDRAM Configuration Mapping: 4K Rows, 256/512/1024/2048 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					Row[11:0]												Bk[1:0]		Column[7:0]									M[1:0]	
				Row[11:0]												Bk[1:0]			Column[8:0]									M[1:0]	
			Row[11:0]												Bk[1:0]				Column[9:0]									M[1:0]	
		Row[11:0]												Bk[1:0]					Column[10:0]									M[1:0]	

Table 36-19: Sequential Mapping DDR-SDRAM Configuration Mapping: 8K Rows, 512/1024/2048 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			Bk[1:0]				Row[12:0]											Column[8:0]									M[1:0]	
		Bk[1:0]					Row[12:0]												Column[9:0]									M[1:0]	
	Bk[1:0]				Row[12:0]													Column[10:0]									M[1:0]	

MASKVAL. A 16-bit word comparison is done. The byte at the offset number of bytes from the index start is compared to bits 7:0 of the configured COMPVAL and MASKVAL. The byte at the offset number of bytes + 1 from the index start is compared to bits 15:8 of the configured COMPVAL and MASKVAL.

The offset value in bytes, OFFSVAL, ranges from 0 to 127 bytes from either the start of the frame, the byte after the EtherType field, the byte after the IP header (IPv4 or IPv6) or the byte after the TCP/UDP header. Note the logic to decode the IP header or the TCP/UDP header is reused from the TCP/UDP/IP checksum offload logic and therefore has the same restrictions on use (the main limitation is that IP fragmentation is not supported). Refer to the Checksum Offload for IP, TCP and UDP section of this documentation for further details.

Compare A, B, and C use a common set of 24 GMAC_ST2CW0/1 registers, thus all COMPA, COMPB and COMPC fields in the registers GMAC_ST2RPQ point to a single pool of 24 GMAC_ST2CW0/1 registers.

Note that Compare A, B and C together allow matching against an arbitrary 48 bits of data and so can be used to match against a MAC address.

All enabled comparisons are ANDed together to form the overall type 2 screening match.

40.6.4 MAC Transmit Block

The MAC transmitter can operate in either half duplex or full duplex mode and transmits frames in accordance with the Ethernet IEEE 802.3 standard. In half duplex mode, the CSMA/CD protocol of the IEEE 802.3 specification is followed.

A small input buffer receives data through the FIFO interface which will extract data in 32-bit form. All subsequent processing prior to the final output is performed in bytes.

Transmit data can be output using the MII interface.

Frame assembly starts by adding preamble and the start frame delimiter. Data is taken from the transmit FIFO interface a word at a time.

If necessary, padding is added to take the frame length to 60 bytes. CRC is calculated using an order 32-bit polynomial. This is inverted and appended to the end of the frame taking the frame length to a minimum of 64 bytes. If the no CRC bit is set in the second word of the last buffer descriptor of a transmit frame, neither pad nor CRC are appended. The no CRC bit can also be set through the FIFO interface.

In full duplex mode (at all data rates), frames are transmitted immediately. Back to back frames are transmitted at least 96 bit times apart to guarantee the interframe gap.

In half duplex mode, the transmitter checks carrier sense. If asserted, the transmitter waits for the signal to become inactive, and then starts transmission after the interframe gap of 96 bit times. If the collision signal is asserted during transmission, the transmitter will transmit a jam sequence of 32 bits taken from the data register and then retry transmission after the backoff time has elapsed. If the collision occurs during either the preamble or Start Frame Delimiter (SFD), then these fields will be completed prior to generation of the jam sequence.

The backoff time is based on an XOR of the 10 least significant bits of the data coming from the transmit FIFO interface and a 10-bit pseudo random number generator. The number of bits used depends on the number of collisions seen. After the first collision 1 bit is used, then the second 2 bits and so on up to the maximum of 10 bits. All 10 bits are used above ten collisions. An error will be indicated and no further attempts will be made if 16 consecutive attempts cause collision. This operation is compliant with the description in Clause 4.2.3.2.5 of the IEEE 802.3 standard which refers to the truncated binary exponential backoff algorithm.

In 10/100 mode, both collisions and late collisions are treated identically, and backoff and retry will be performed up to 16 times. This condition is reported in the transmit buffer descriptor word 1 (late collision, bit 26) and also in the Transmit Status register (late collision, bit 7). An interrupt can also be generated (if enabled) when this exception occurs, and bit 5 in the Interrupt Status register will be set.

In all modes of operation, if the transmit DMA underruns, a bad CRC is automatically appended using the same mechanism as jam insertion and the GTXER signal is asserted. For a properly configured system this should never happen and also it is impossible if configured to use the DMA with packet buffers, as the complete frame is buffered in local packet buffer memory.

By setting when bit 28 is set in the Network Configuration register, the Inter Packet Gap (IPG) may be stretched beyond 96 bits depending on the length of the previously transmitted frame and the value written to the IPG Stretch register (GMAC_IPGS). The least significant 8 bits of the IPG Stretch register multiply the previous frame length (including preamble). The next significant 8 bits (+1 so as not to get a divide by zero) divide the frame length to generate the IPG. IPG stretch only works in full duplex mode and when bit 28 is set in the Network Configuration register. The IPG Stretch register cannot be used to shrink the IPG below 96 bits.

If the back pressure bit is set in the Network Control register, or if the HDFC configuration bit is set in the GMAC_UR register (10M or 100M half duplex mode), the transmit block transmits 64 bits of data, which can consist of 16 nibbles of 1011 or in bit rate mode 64 1s, whenever it sees an incoming frame to force a collision. This provides a way of implementing flow control in half duplex mode.

40.6.5 MAC Receive Block

All processing within the MAC receive block is implemented using a 16-bit data path. The MAC receive block checks for valid preamble, FCS, alignment and length, presents received frames to the FIFO interface and stores the frame destination address for use by the address checking block.

40.8.59 GMAC Greater Than 1518 Byte Frames Transmitted Register

Name: GMAC_GTBFT1518

Address: 0xF8008130

Access: Read-only

31	30	29	28	27	26	25	24
NFTX							

23	22	21	20	19	18	17	16
NFTX							

15	14	13	12	11	10	9	8
NFTX							

7	6	5	4	3	2	1	0
NFTX							

NFTX: Greater than 1518 Byte Frames Transmitted without Error

This register counts the number of 1518 or above byte frames successfully transmitted without error i.e., no underrun and not too many retries.

46.6.3.5 Master Receiver Mode

Master Receiver mode is not available if High-speed mode is selected.

The read sequence begins by setting the START bit. After the START condition has been sent, the master sends a 7-bit slave address to notify the slave device. The bit following the slave address indicates the transfer direction, 1 in this case (MREAD = 1 in TWIHS_MMR). During the acknowledge clock pulse (9th pulse), the master releases the data line (HIGH), enabling the slave to pull it down in order to generate the acknowledge. The master polls the data line during this clock pulse and sets the NACK bit in the TWIHS_SR if the slave does not acknowledge the byte.

If an acknowledge is received, the master is then ready to receive data from the slave. After data has been received, the master sends an acknowledge condition to notify the slave that the data has been received except for the last data (see Figure 46-7). When the RXRDY bit is set in the TWIHS_SR, a character has been received in the Receive Holding register (TWIHS_RHR). The RXRDY bit is reset when reading the TWIHS_RHR.

When a single data byte read is performed, with or without internal address **(**IADR), the START and STOP bits must be set at the same time. See Figure 46-7. When a multiple data byte read is performed, with or without internal address **(**IADR), the STOP bit must be set after the next-to-last data received (same condition applies for START bit to generate a REPEATED START). See Figure 46-8. For internal address usage, see Section 46.6.3.6, Internal Address.

If TWIHS_RHR is full (RXRDY high) and the master is receiving data, the serial clock line is tied low before receiving the last bit of the data and until the TWIHS_RHR is read. Once the TWIHS_RHR is read, the master stops stretching the serial clock line and ends the data reception. See Figure 46-9.

Warning: When receiving multiple bytes in Master Read mode, if the next-to-last access is not read (the RXRDY flag remains high), the last access is not completed until TWIHS_RHR is read. The last access stops on the next-to-last bit (clock stretching). When the TWIHS_RHR is read, there is only half a bit period to send the STOP (or START) command, else another read access might occur (spurious access).

A possible workaround is to set the STOP (or START) bit before reading the TWIHS_RHR on the next-to-last access (within IT handler).

Figure 46-7: Master Read with One Data Byte

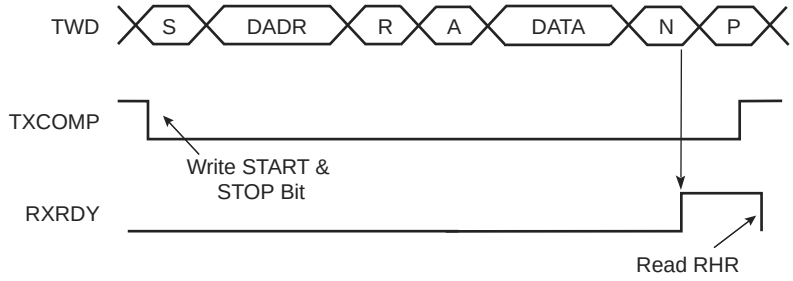


Figure 46-8: Master Read with Multiple Data Bytes

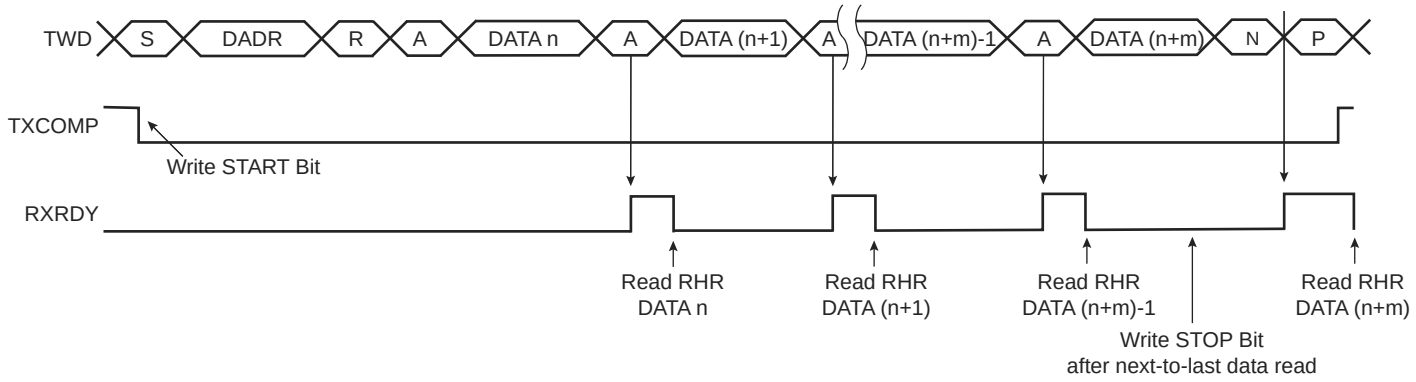
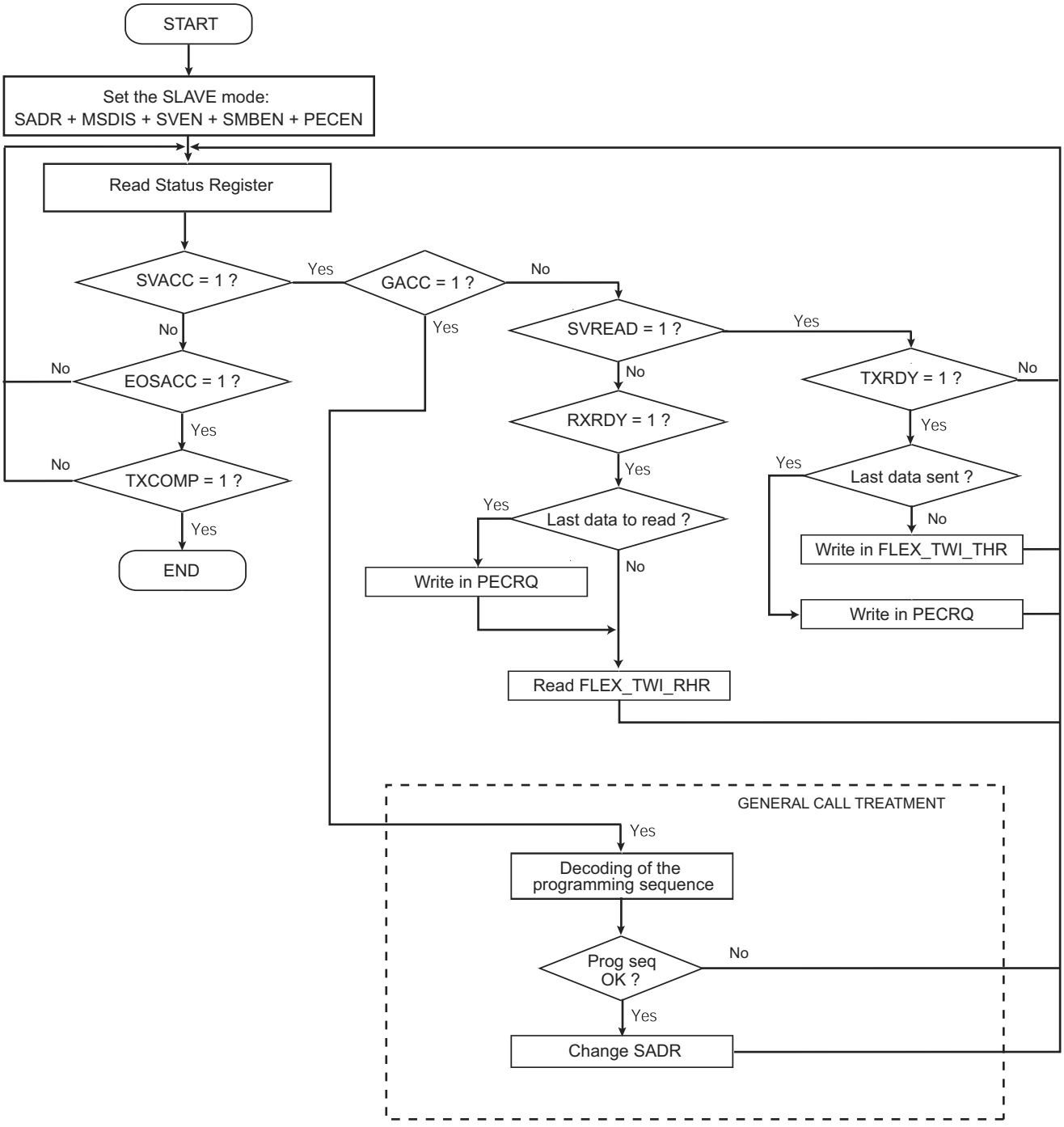


Figure 47-126: Read/Write in Slave Mode with SMBus PEC



FSDIS: Frame Slot Mode Disable

0: The Frame Slot mode is enabled.

1: The Frame Slot mode is disabled.

WKUPTYP: Wakeup Signal Type

0: Setting the LINWKUP bit in the control register sends a LIN 2.0 wakeup signal.

1: Setting the LINWKUP bit in the control register sends a LIN 1.3 wakeup signal.

DLC: Data Length Control

0–255: Defines the response data length if DLM = 0,in that case the response data length is equal to DLC+1 bytes.

PDCM: DMAC Mode

0: The LIN mode register FLEX_US_LINMR is not written by the DMAC.

1: The LIN mode register FLEX_US_LINMR (excepting that flag) is written by the DMAC.

SYNCDIS: Synchronization Disable

0: The synchronization procedure is performed in LIN slave node configuration.

1: The synchronization procedure is not performed in LIN slave node configuration.

47.10.37 USART FIFO Interrupt Enable Register

Name: FLEX_US_FIER

Address: 0xF80342A8 (0), 0xF80382A8 (1), 0xFC0102A8 (2), 0xFC0142A8 (3), 0xFC0182A8 (4)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	RXFTHF2	–
7	6	5	4	3	2	1	0
RXFPTEF	TXFPTEF	RXFTHF	RXFFF	RXFEF	TXFTHF	TXFFF	TXFEF

TXFEF: TXFEF Interrupt Enable

TXFFF: TXFFF Interrupt Enable

TXFTHF: TXFTHF Interrupt Enable

RXFEF: RXFEF Interrupt Enable

RXFFF: RXFFF Interrupt Enable

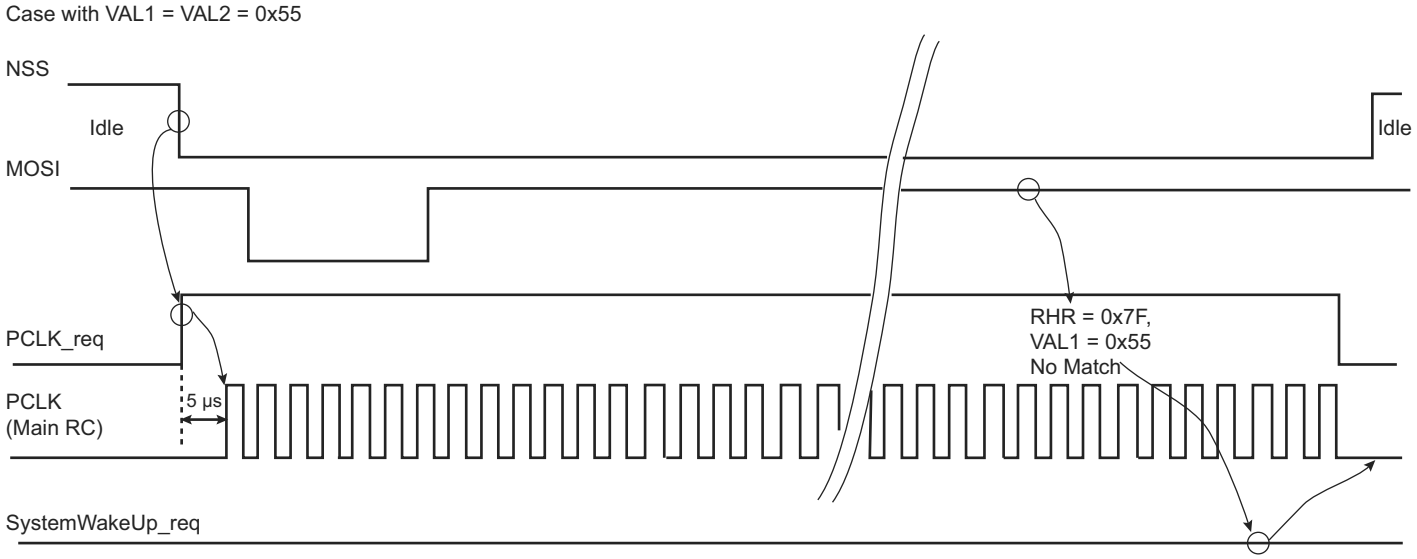
RXFTHF: RXFTHF Interrupt Enable

TXFPTEF: TXFPTEF Interrupt Enable

RXFPTEF: RXFPTEF Interrupt Enable

RXFTHF2: RXFTHF2 Interrupt Enable

Figure 49-15: Asynchronous Event Generating Only Partial Wakeup



49.7.7 FIFOs

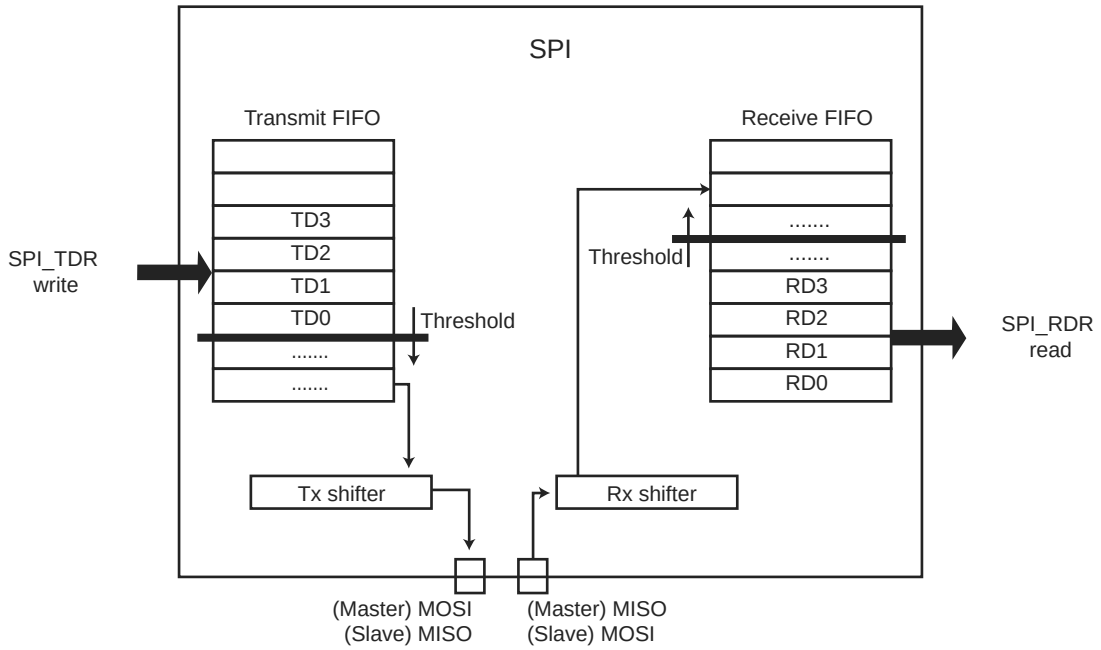
49.7.7.1 Overview

The SPI includes two FIFOs which can be enabled/disabled using SPI_CR.FIFOEN/FIFODIS. It is recommended to disable the SPI module before enabling or disabling the SPI FIFOs (SPI_CR.SPIDIS).

Writing SPI_CR.FIFOEN to ‘1’ enables a 16-data Transmit FIFO and a 16-data Receive FIFO.

It is possible to write or to read single or multiple data in the same access to SPI_TDR/RDR. Refer to Section 49.7.7.6 “Single Data Mode” and to Section 49.7.7.7 “Multiple Data Mode”.

Figure 49-16: FIFOs Block Diagram



49.7.7.2 Sending Data with FIFO Enabled

When the Transmit FIFO is enabled, write access to SPI_TDR loads the Transmit FIFO.

The OPTL field determines the length of the option code. The value written in OPTL must be consistent with the value written in the field WIDTH. For example, OPTL = 0 (1-bit option code) is not consistent with WIDTH = 6 (option code sent with QuadSPI protocol, thus the minimum length of the option code is 4 bits).

Value	Name	Description
0	OPTION_1BIT	The option code is 1 bit long.
1	OPTION_2BIT	The option code is 2 bits long.
2	OPTION_4BIT	The option code is 4 bits long.
3	OPTION_8BIT	The option code is 8 bits long.

ADDRL: Address Length

The ADDRL bit determines the length of the address.

0 (24_BIT): The address is 24 bits long.

1 (32_BIT): The address is 32 bits long.

TFRTYP: Data Transfer Type

Value	Name	Description
0	TRSFR_READ	Read transfer from the serial memory. Scrambling is not performed. Read at random location (fetch) in the serial Flash memory is not possible.
1	TRSFR_READ_MEMORY	Read data transfer from the serial memory. If enabled, scrambling is performed. Read at random location (fetch) in the serial Flash memory is possible.
2	TRSFR_WRITE	Write transfer into the serial memory. Scrambling is not performed.
3	TRSFR_WRITE_MEMORY	Write data transfer into the serial memory. If enabled, scrambling is performed.

CRM: Continuous Read Mode

0 (DISABLED): Continuous Read mode is disabled.

1 (ENABLED): Continuous Read mode is enabled.

NBDUM: Number Of Dummy Cycles

The NBDUM field defines the number of dummy cycles required by the serial Flash memory before data transfer.

51.11.2.1 SDMMC Tuning Sequence

The SDMMC tuning sequence must only be done when SD/SDIO SDR104 or e.MMC HS200 is selected and for a 100-MHz SDCLK frequency or higher.

1. Enable the retuning timer (TMREN = 1 in SDMMC_RTC1R).
2. Configure the retuning period by setting TCVAL in SDMMC_RTCVR.
3. Set 'Retuning Timer Event' (TEVT) to 1 in SDMMC_RTISTER so that the TEVT status flag in SDMMC_RTISTR rises each time the retuning timer counter period elapses.
4. Set TEVT to 1 in SDMMC_RTISIER to generate an interrupt on the TEVT status flag assertion (optional).
5. Execute the tuning procedure as defined in "Sampling Clock Tuning Procedure" in the "SD Host Controller Simplified Specification V3.00" .
6. Start the retuning timer count (write RLD to 1 in SDMMC_RTC2R). At this step, data can be read by the SDMMC.
7. Each time TEVT is set to 1 in SDMMC_RTISTR:
   a) Execute the tuning procedure as defined in "Sampling Clock Tuning Procedure" in the "SD Host Controller Simplified Specification V3.00" before issuing the next command.
   b) Restart the retuning timer count (write RLD to 1 in SDMMC_RTC2R).
   c) Resume data reading from the device.

When several instances of SDMMC are implemented in a product, the TEVT status flag of each SDMMC instance can be checked by reading SDMMC_RTSSR.

51.12 I/O Calibration

The need for output impedance calibration arises with higher data rates. As the data rate increases, some transmission line effects can occur and lead to the generation of undershoots and overshoots, hence degrading the signal quality.

To avoid these transmission problems, an I/O calibration cell is used to adjust the output impedance to the driven I/Os.

The I/O calibration sequence is mandatory when one of the SD/SDIO UHS-I modes (VS18EN = 1 in SDMMC_HC2R) or e.MMC HS200 (HS200EN = $B_{(hexa)}$) is selected. It must be performed periodically to prevent the output impedance drift. Once the calibration is finished, the I/O calibration cell provides two four-bit control words (CALP[3:0] and CALN[3:0] in the Calibration Control register (SDMMC_CALCR)) to tune the output impedance, and thus reach the best transmission performances.

The I/O calibration sequence can be started manually by writing a '1' to SDMMC_CALCR.EN. This bit is cleared automatically at the end of the calibration.

The I/O calibration sequence can also be performed automatically if SDMMC_CALCR.TUNDIS is cleared. In this case, the calibration starts automatically at the beginning of the tuning procedure when writing EXTUN to 1 in SDMMC_HC2R.

The I/O calibration cell requires a startup time defined by SDMMC_CALCR.CNTVAL. Thus, CNTVAL must be configured prior to start the calibration sequence. If SDMMC_CALCR.ALWYSON is set to '1', the startup time is only required for the first calibration sequence as the analog circuitry is not shut down at the end of the calibration. In order to reduce the power consumption, the analog circuitry can be shut down at the end of the calibration sequence by clearing ALWYSON. In this case, the startup time is performed each time a calibration sequence is started.

51.13.54 SDMMC Retuning Interrupt Status Register

Name: SDMMC_RTISTR

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	TEVT

TEVT: Retuning Timer Event

This bit is set to 1 when the retuning timer count is elapsed if TEVT is set to 1 in SDMMC_RTISTER. An interrupt is generated if TEVT is set to 1 in SDMMC_RTISIER.

Writing this bit to 1 clears this bit.

0: No retuning timer event.

1: Retuning timer event.

55.6.2.4 Low Pass Filter

The PDMIC includes a sixth-order IIR filter that performs a low pass transfer function and decimates by 2 the output of the sinc filter. The coefficients are computed for a decimated sampling rate of 48 kHz and optimize the 0 to 20 kHz band flatness while rejecting the aliasing of the PDM microphone by at least 60 dB in the 28 to 48 kHz band.

If the decimated sampling rate is modified, the frequency response of this filter is scaled proportionally to the new frequency.

Figure 55-7 and Figure 55-8 are drawn for an output sampling frequency of 48 kHz.

Figure 55-7: Low Pass Filter Spectral Mask

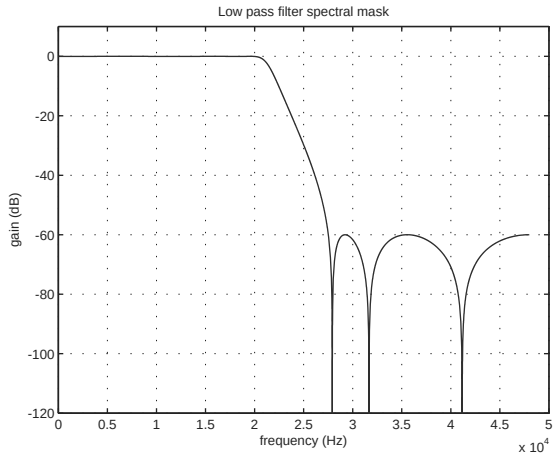
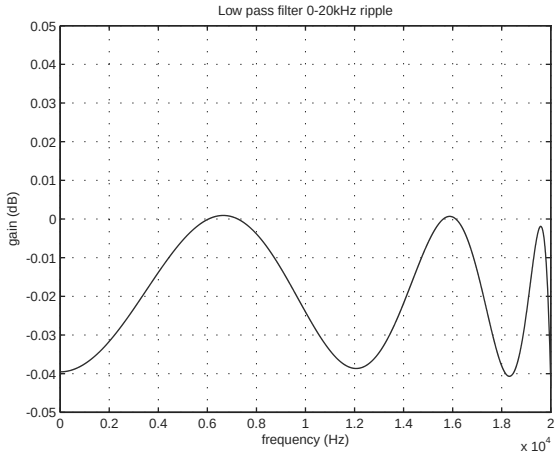


Figure 55-8: Low Pass Filter Ripple in the 0 to 20 kHz Band



56.7.9 PWM Sync Channels Mode Register

Name: PWM_SCM

Address: 0xF802C020

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
PTRCS			PTRM	–	–	UPDM	

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	SYNC3	SYNC2	SYNC1	SYNC0

This register can only be written if bits WPSWS2 and WPHWS2 are cleared in the PWM Write Protection Status Register.

SYNCx: Synchronous Channel x

0: Channel x is not a synchronous channel.

1: Channel x is a synchronous channel.

UPDM: Synchronous Channels Update Mode

Value	Name	Description
0	MODE0	Manual write of double buffer registers and manual update of synchronous channels(1)
1	MODE1	Manual write of double buffer registers and automatic update of synchronous channels(2)
2	MODE2	Automatic write of duty-cycle update registers by the DMA Controller and automatic update of synchronous channels(2)

Note 1: The update occurs at the beginning of the next PWM period, when the UPDULOCK bit in PWM Sync Channels Update Control Register is set.

2: The update occurs when the Update Period is elapsed.

PTRM: DMA Controller Transfer Request Mode

UPDM	PTRM	WRDY Flag and DMA Controller Transfer Request
0	x	The WRDY flag in PWM Interrupt Status Register 2 and the DMA transfer request are never set to ‘1’.
1	x	The WRDY flag in PWM Interrupt Status Register 2 is set to ‘1’ as soon as the update period is elapsed, the DMA Controller transfer request is never set to ‘1’.
2	0	The WRDY flag in PWM Interrupt Status Register 2 and the DMA transfer request are set to ‘1’ as soon as the update period is elapsed.
	1	The WRDY flag in PWM Interrupt Status Register 2 and the DMA transfer request are set to ‘1’ as soon as the selected comparison matches.

PTRCS: DMA Controller Transfer Request Comparison Selection

Selection of the comparison used to set the flag WRDY and the corresponding DMA Controller transfer request.

64.3 Block Diagram

Figure 64-1: SECUMOD Block Diagram

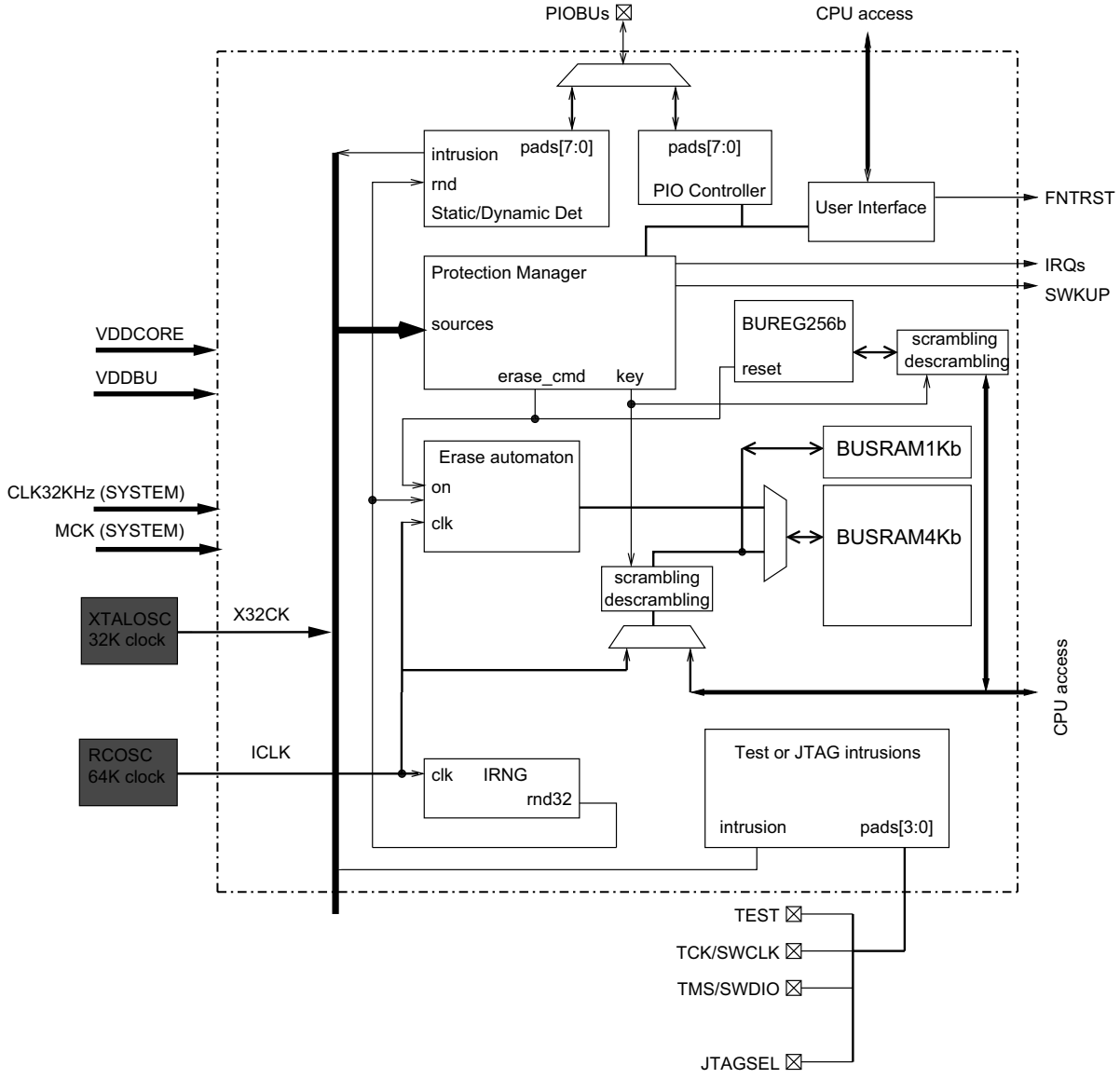


Figure 64-1 represents the logic inside the SECUMOD. Analog cells are external to the IP and highlighted in green.

Table 66-53: FLEXCOM0 in SPI Mode IOSET1 Timings (Continued)

	Power Supply	1.8V		3.3V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
SPI_7	MOSI Setup time before SPCK rises	5.3	–	5	–	ns
SPI_8	MOSI Hold time after SPCK rises	0.4	–	0.3	–	ns
SPI_9	SPCK rising to MISO	10.7	13.1	9	11.5	ns
SPI_{10}	MOSI Setup time before SPCK falls	5.3	–	5	–	ns
SPI_{11}	MOSI Hold time after SPCK falls	0.4	–	0.3	–	ns
SPI_{12}	NPCS0 setup to SPCK rising	5.6	–	5.4	–	ns
SPI_{13}	NPCS0 hold after SPCK falling	0.7	–	0.6	–	ns
SPI_{14}	NPCS0 setup to SPCK falling	5.4	–	5.2	–	ns
SPI_{15}	NPCS0 hold after SPCK rising	0.2	–	0.1	–	ns
SPI_{16}	NPCS0 falling to MISO valid	17.5	–	16.2	–	ns

66.26 GMAC Timings

66.26.1 Timing Conditions

Timings assuming a capacitance load on data and clock are given in Table 66-99.

Table 66-99: Capacitance Load on Data, Clock Pads

Supply	Corner	
	Max	Min
3.3V	20 pF	0 pF

66.26.2 Timing Constraints

Table 66-100: Ethernet MAC Signals Relative to GMDC

Symbol	Parameter	Min	Max	Unit
$EMAC_1$	Setup for GMDIO from GMDC rising	10	–	ns
$EMAC_2$	Hold for GMDIO from GMDC rising	10	–	ns
$EMAC_3$	GMDIO toggling from GMDC rising(1)	0	300	ns

Note 1: For Ethernet MAC output signals, minimum and maximum access time are defined. The minimum access time is the time between the GMDC rising edge and the signal change. The maximum access timing is the time between the GMDC rising edge and the signal stabilizes. Figure 66-41 illustrates minimum and maximum accesses for $EMAC_3$.

Figure 66-41: Minimum and Maximum Access Time of Ethernet MAC Output Signals