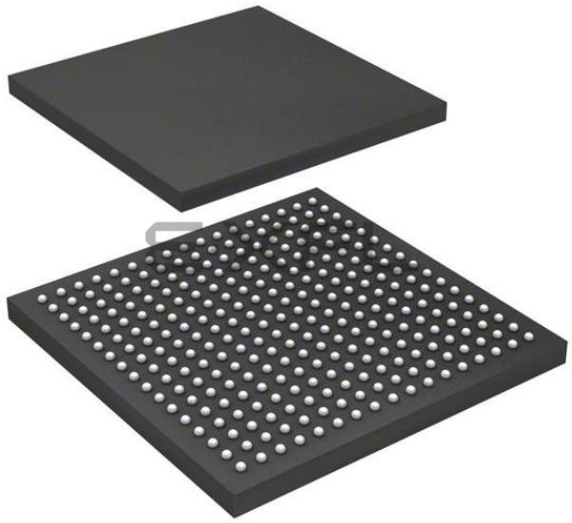

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26c-cu

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)(1)(2)
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
K5	L2	K4	GNDANA	ground	GNDANA	I	–	–	–	–	–	–	–
M6	P5	L2	VDDANA	–	ADVREF	I	–	–	–	–	–	–	–
K3	J1	H2	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
L3	J2	J2	GNDANA	ground	GNDANA	I	–	–	–	–	–	–	–
H16, D16	J17, D12	H12, C12	VDDIODDR	DDR	DDR_VREF	–	–	–	–	–	–	–	–
B12	B12	B7	VDDIODDR	DDR	DDR_D0	–	–	–	–	–	–	–	–
A12	B13	A7	VDDIODDR	DDR	DDR_D1	–	–	–	–	–	–	–	–
C12	D13	C8	VDDIODDR	DDR	DDR_D2	–	–	–	–	–	–	–	–
A13	A13	B9	VDDIODDR	DDR	DDR_D3	–	–	–	–	–	–	–	–
A14	A15	A9	VDDIODDR	DDR	DDR_D4	–	–	–	–	–	–	–	–
C13	D14	C9	VDDIODDR	DDR	DDR_D5	–	–	–	–	–	–	–	–
A15	B15	A10	VDDIODDR	DDR	DDR_D6	–	–	–	–	–	–	–	–
B15	B16	B10	VDDIODDR	DDR	DDR_D7	–	–	–	–	–	–	–	–
G17	G18	H13	VDDIODDR	DDR	DDR_D8	–	–	–	–	–	–	–	–
G16	K17	H14	VDDIODDR	DDR	DDR_D9	–	–	–	–	–	–	–	–
H17	J13	J13	VDDIODDR	DDR	DDR_D10	–	–	–	–	–	–	–	–
K17	H15	J14	VDDIODDR	DDR	DDR_D11	–	–	–	–	–	–	–	–
K16	J15	L13	VDDIODDR	DDR	DDR_D12	–	–	–	–	–	–	–	–
J13	J14	L14	VDDIODDR	DDR	DDR_D13	–	–	–	–	–	–	–	–
K14	K13	J12	VDDIODDR	DDR	DDR_D14	–	–	–	–	–	–	–	–
K15	K18	K12	VDDIODDR	DDR	DDR_D15	–	–	–	–	–	–	–	–
B8	A8	–	VDDIODDR	DDR	DDR_D16	–	–	–	–	–	–	–	–
B9	B9	–	VDDIODDR	DDR	DDR_D17	–	–	–	–	–	–	–	–
C9	D9	–	VDDIODDR	DDR	DDR_D18	–	–	–	–	–	–	–	–
A9	A9	–	VDDIODDR	DDR	DDR_D19	–	–	–	–	–	–	–	–
A10	B11	–	VDDIODDR	DDR	DDR_D20	–	–	–	–	–	–	–	–
D10	D10	–	VDDIODDR	DDR	DDR_D21	–	–	–	–	–	–	–	–
B11	A11	–	VDDIODDR	DDR	DDR_D22	–	–	–	–	–	–	–	–
A11	A12	–	VDDIODDR	DDR	DDR_D23	–	–	–	–	–	–	–	–
J12	L18	–	VDDIODDR	DDR	DDR_D24	–	–	–	–	–	–	–	–
H10	K15	–	VDDIODDR	DDR	DDR_D25	–	–	–	–	–	–	–	–
J11	K14	–	VDDIODDR	DDR	DDR_D26	–	–	–	–	–	–	–	–
K11	M18	–	VDDIODDR	DDR	DDR_D27	–	–	–	–	–	–	–	–
L13	N17	–	VDDIODDR	DDR	DDR_D28	–	–	–	–	–	–	–	–
L11	M14	–	VDDIODDR	DDR	DDR_D29	–	–	–	–	–	–	–	–
L12	M15	–	VDDIODDR	DDR	DDR_D30	–	–	–	–	–	–	–	–
M17	N18	–	VDDIODDR	DDR	DDR_D31	–	–	–	–	–	–	–	–

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)(1)(2)
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
F12	D17	E11	VDDIODDR	DDR	DDR_A0	–	–	–	–	–	–	–	–
C17	A17	C11	VDDIODDR	DDR	DDR_A1	–	–	–	–	–	–	–	–
B17	A18	B12	VDDIODDR	DDR	DDR_A2	–	–	–	–	–	–	–	–
B16	F15	A12	VDDIODDR	DDR	DDR_A3	–	–	–	–	–	–	–	–
C16	G12	D11	VDDIODDR	DDR	DDR_A4	–	–	–	–	–	–	–	–
G14	H12	D14	VDDIODDR	DDR	DDR_A5	–	–	–	–	–	–	–	–
F14	F13	B14	VDDIODDR	DDR	DDR_A6	–	–	–	–	–	–	–	–
F11	H10	D9	VDDIODDR	DDR	DDR_A7	–	–	–	–	–	–	–	–
C14	A16	C10	VDDIODDR	DDR	DDR_A8	–	–	–	–	–	–	–	–
D13	E12	D10	VDDIODDR	DDR	DDR_A9	–	–	–	–	–	–	–	–
C15	H11	F9	VDDIODDR	DDR	DDR_A10	–	–	–	–	–	–	–	–
A16	J10	A11	VDDIODDR	DDR	DDR_A11	–	–	–	–	–	–	–	–
A17	D15	B11	VDDIODDR	DDR	DDR_A12	–	–	–	–	–	–	–	–
G11	J11	E13	VDDIODDR	DDR	DDR_A13	–	–	–	–	–	–	–	–
E17	C18	A13	VDDIODDR	DDR	DDR_CLK	–	–	–	–	–	–	–	–
D17	C17	B13	VDDIODDR	DDR	DDR_CLKN	–	–	–	–	–	–	–	–
F16	F18	E14	VDDIODDR	DDR	DDR_CKE	–	–	–	–	–	–	–	–
E16	F17	D13	VDDIODDR	DDR	DDR_RESETN	–	–	–	–	–	–	–	–
G13	J12	F11	VDDIODDR	DDR	DDR_CS	–	–	–	–	–	–	–	–
F15	D18	A14	VDDIODDR	DDR	DDR_WE	–	–	–	–	–	–	–	–
F13	E18	C14	VDDIODDR	DDR	DDR_RAS	–	–	–	–	–	–	–	–
G12	E17	C13	VDDIODDR	DDR	DDR_CAS	–	–	–	–	–	–	–	–
C11	D11	D8	VDDIODDR	DDR	DDR_DQM0	–	–	–	–	–	–	–	–
G15	H14	G14	VDDIODDR	DDR	DDR_DQM1	–	–	–	–	–	–	–	–
C8	B8	–	VDDIODDR	DDR	DDR_DQM2	–	–	–	–	–	–	–	–
H11	L13	–	VDDIODDR	DDR	DDR_DQM3	–	–	–	–	–	–	–	–
B13	A14	B8	VDDIODDR	DDR	DDR_DQS0	–	–	–	–	–	–	–	–
J17	H18	K14	VDDIODDR	DDR	DDR_DQS1	–	–	–	–	–	–	–	–
C10	A10	–	VDDIODDR	DDR	DDR_DQS2	–	–	–	–	–	–	–	–
L17	M17	–	VDDIODDR	DDR	DDR_DQS3	–	–	–	–	–	–	–	–
B14	B14	A8	VDDIODDR	DDR	DDR_DQSN0	–	–	–	–	–	–	–	–
J16	J18	K13	VDDIODDR	DDR	DDR_DQSN1	–	–	–	–	–	–	–	–
B10	B10	–	VDDIODDR	DDR	DDR_DQSN2	–	–	–	–	–	–	–	–
L16	L17	–	VDDIODDR	DDR	DDR_DQSN3	–	–	–	–	–	–	–	–
H12	H13	F13	VDDIODDR	DDR	DDR_BA0	–	–	–	–	–	–	–	–
H13	K12	G13	VDDIODDR	DDR	DDR_BA1	–	–	–	–	–	–	–	–
F17	H17	F14	VDDIODDR	DDR	DDR_BA2	–	–	–	–	–	–	–	–

8.1 Embedded Memories

8.1.1 Internal SRAM

The SAMA5D2 embeds a total of 128 Kbytes of high-speed SRAM. After reset, and until the Remap command is performed, the SRAM is accessible at address 0x0020 0000. When the AXI Bus Matrix is remapped, the SRAM is also available at address 0x0.

The device features a second 128-Kbyte SRAM that can be allocated either to the L2 cache controller or used as an internal SRAM. After reset, this block is connected to the system SRAM, making the two 128-Kbyte RAMs contiguous. The SRAM_SEL bit, located in the SFR_L2CC_HRAMC register, is used to reassign this memory as a L2 cache memory.

8.1.2 Internal ROM

The product embeds one 160-Kbyte secured internal ROM mapped at address 0 after reset. The ROM contains a standard and secure bootloader as well as the BCH (Bose, Chaudhuri and Hocquenghem) code tables for NAND Flash ECC correction. The memory area containing the secure boot is automatically hidden after the execution of the secure boot while the one containing the code tables for ECC remains visible.

8.1.3 Boot Strategies

For standard boot strategies, refer to Section 16. “Standard Boot Strategies” of this datasheet.

For secure boot strategies, refer to the document “SAMA5D2x Secure Boot Strategy”, document no. 44040 (Non-Disclosure Agreement required).

8.2 External Memory

The SAMA5D2 offers connections to a wide range of external memories or to parallel peripherals.

8.2.1 External Bus Interface

The External Bus Interface (EBI) is a 16-bit wide interface working at MCK/2.

The EBI supports:

- Static memories
- 8-bit NAND Flash with 32-bit BCH ECC
- 16-bit NAND Flash

EBI I/Os accept three drive levels (Low, Medium, High) to avoid overshoots and provide the best performances according to the bus load and external memories voltage.

The drive levels are configured with the DRVSTR field in the PIO Configuration Register (PIO_CFGRx) if the corresponding line is non-secure or the Secure PIO Configuration Register (S_PIO_CFGRx) if the I/O line is secure.

At reset, the selected drive is low. The user must make sure to program the correct drive according to the device load. The I/O embeds serial resistors for impedance matching.

8.2.2 Supported Memories on DDR2/DDR3/LPDDR1/LPDDR2/LPDDR3 Interface

- 16-bit or 32-bit external interface
- 512 Mbytes of address space on DDR CS and DDR/AES CS in 32-bit mode
- 256 Mbytes of address space on DDR CS and DDR/AES CS in 16-bit mode
- Supports 16-bit or 32-bit 8-bank DDR2, DDR3, LPDDR1, LPDDR2 and LPDDR3 memories
- Automatic drive level control
- Multiport
- Scramblable data path
- Port 0 of this interface has an embedded automatic AES encryption and decryption mechanism (refer to Section 59. “Advanced Encryption Standard Bridge (AESB)”). Writing to or reading from the address 0x40000000 may trigger the encryption and decryption mechanism depending on the AESB on External Memories configuration.
- TrustZone: The multiport feature of this interface implies TrustZone configuration constraints. Refer to Section 18.12 “TrustZone Extension to AHB and APB” for more details.

8.2.3 Supported Memories on Static Memories and NAND Flash Interfaces

The Static Memory Controller is dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and parallel peripherals

12. Chip Identifier (CHIPID)

12.1 Description

Chip Identifier (CHIPID) registers are used to recognize the device and its revision. These registers provide the sizes and types of the on-chip memories, as well as the set of embedded peripherals.

Two CHIPID registers are embedded: Chip ID Register (CHIPID_CIDR) and Chip ID Extension Register (CHIPID_EXID). Both registers contain a hard-wired value that is read-only.

The CHIPID_CIDR register contains the following fields:

- VERSION: Identifies the revision of the silicon
- EPROC: Indicates the embedded ARM processor
- NVPTYP and NVPSIZ: Identify the type of embedded non-volatile memory and the size
- SRAMSIZ: Indicates the size of the embedded SRAM
- ARCH: Identifies the set of embedded peripherals
- EXT: Shows the use of the extension identifier register

The CHIPID_EXID register is device-dependent and reads 0 if CHIPID_CIDR.EXT = 0.

12.2 Embedded Characteristics

- Chip ID Registers
  - Identification of the Device Revision, Sizes of the Embedded Memories, Set of Peripherals, Embedded Processor

Table 12-1: SAMA5D2 Chip ID Registers

Chip Name	CHIPID_CIDR	CHIPID_EXID
ATSAMA5D22A-CU	0x8A5C08C0	0x00000059
ATSAMA5D24A-CU	0x8A5C08C0	0x00000014
ATSAMA5D27A-CU	0x8A5C08C0	0x00000011
ATSAMA5D28A-CU	0x8A5C08C0	0x00000010
ATSAMA5D21B-CU	0x8A5C08C1	0x0000005A
ATSAMA5D22B-CN	0x8A5C08C1	0x00000069
ATSAMA5D22B-CU	0x8A5C08C1	0x00000059
ATSAMA5D23B-CN	0x8A5C08C1	0x00000068
ATSAMA5D23B-CU	0x8A5C08C1	0x00000058
ATSAMA5D24B-CU	0x8A5C08C1	0x00000014
ATSAMA5D26B-CN	0x8A5C08C1	0x00000022
ATSAMA5D26B-CU	0x8A5C08C1	0x00000012
ATSAMA5D27B-CN	0x8A5C08C1	0x00000021
ATSAMA5D27B-CU	0x8A5C08C1	0x00000011
ATSAMA5D28B-CN	0x8A5C08C1	0x00000020
ATSAMA5D28B-CU	0x8A5C08C1	0x00000010
ATSAMA5D21C-CU	0x8A5C08C2	0x0000005A
ATSAMA5D22C-CN	0x8A5C08C2	0x00000069
ATSAMA5D22C-CU	0x8A5C08C2	0x00000059
ATSAMA5D23C-CN	0x8A5C08C2	0x00000068

21.8.5 Protect Mode

The Protect mode is used to read the Interrupt Vector register without performing the associated automatic operations. This is necessary when working with a debug system. When a debugger, working either with a Debug Monitor or the ARM processor's ICE, stops the applications and updates the opened windows, it might read the AIC User Interface and thus the IVR. This has adverse consequences:

- If an enabled interrupt with a higher priority than the current one is pending, it is stacked.
- If there is no enabled pending interrupt, the spurious vector is returned.

In either case, an End of Interrupt command is necessary to acknowledge and restore the context of the AIC. This operation is generally not performed by the debug system, as the debug system would become strongly intrusive and cause the application to enter an undesired state.

This is avoided by using the Protect mode. Writing PROT in the Debug Control register (AIC_DCR) at 0x1 enables the Protect mode.

When the Protect mode is enabled, the AIC performs interrupt stacking only when a write access is performed on AIC_IVR. Therefore, the Interrupt Service Routines must write (arbitrary data) to AIC_IVR just after reading it. The new context of the AIC, including the value of AIC_ISR, is updated with the current interrupt only when AIC_IVR is written.

An AIC_IVR read on its own (e.g., by a debugger) modifies neither the AIC context nor AIC_ISR. Extra AIC_IVR reads perform the same operations. However, it is recommended to not stop the processor between the read and the write of AIC_IVR of the interrupt service routine to make sure the debugger does not modify the AIC context.

To summarize, in normal operating mode, the read of AIC_IVR performs the following operations within the AIC:

1. Calculates active interrupt (higher than current or spurious).
2. Determines and returns the vector of the active interrupt.
3. Memorizes the interrupt.
4. Pushes the current priority level onto the internal stack.
5. Acknowledges the interrupt.

However, while the Protect mode is activated, only operations 1 to 3 are performed when AIC_IVR is read. Operations 4 and 5 are only performed by the AIC when AIC_IVR is written.

Software that has been written and debugged using the Protect mode runs correctly in normal mode without modification. However, in normal mode, the AIC_IVR write has no effect and can be removed to optimize the code.

21.8.6 Spurious Interrupt

The Advanced Interrupt Controller features a protection against spurious interrupts. A spurious interrupt is defined as being the assertion of an interrupt source long enough for the AIC to assert the nIRQ, but no longer present when AIC_IVR is read. This is most prone to occur when:

- An external interrupt source is programmed in Level-Sensitive mode and an active level occurs for only a short time.
- An internal interrupt source is programmed in level-sensitive and the output signal of the corresponding embedded peripheral is activated for a short time (as is the case for the watchdog).
- An interrupt occurs just a few cycles before the software begins to mask it, thus resulting in a pulse on the interrupt source.

The AIC detects a spurious interrupt at the time AIC_IVR is read while no enabled interrupt source is pending. When this happens, the AIC returns the value stored by the programmer in the Spurious Vector register (AIC_SPU). The programmer must store the address of a spurious interrupt handler in AIC_SPU as part of the application, to enable an as fast as possible return to the normal execution flow. This handler writes in AIC_EOICR and performs a return from interrupt.

21.8.7 General Interrupt Mask

The AIC features a General Interrupt Mask bit (AIC_DCR.GMSK) to prevent interrupts from reaching the processor. Both the nIRQ and the nFIQ lines are driven to their inactive state if AIC_DCR.GMSK is set. However, this mask does not prevent waking up the processor if it has entered Idle mode. This function facilitates synchronizing the processor on a next event and, as soon as the event occurs, performs subsequent operations without having to handle an interrupt. It is strongly recommended to use this mask with caution.

26.6.6 RTC Time Alarm Register

Name: RTC_TIMALR

Address: 0xF80480C0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
HOUREN	AMPM	HOUR					

15	14	13	12	11	10	9	8
MINEN	MIN						

7	6	5	4	3	2	1	0
SECEN	SEC						

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_WPMR).

Note: To change one of the SEC, MIN, HOUR fields, it is recommended to disable the field before changing the value and then re-enable it after the change has been made. This requires up to three accesses to the RTC_TIMALR. The first access clears the enable corresponding to the field to change (SECEN, MINEN, HOUREN). If the field is already cleared, this access is not required. The second access performs the change of the value (SEC, MIN, HOUR). The third access is required to re-enable the field by writing 1 in SECEN, MINEN, HOUREN fields.

SEC: Second Alarm

This field is the alarm field corresponding to the BCD-coded second counter.

SECEN: Second Alarm Enable

0: The second-matching alarm is disabled.

1: The second-matching alarm is enabled.

MIN: Minute Alarm

This field is the alarm field corresponding to the BCD-coded minute counter.

MINEN: Minute Alarm Enable

0: The minute-matching alarm is disabled.

1: The minute-matching alarm is enabled.

HOUR: Hour Alarm

This field is the alarm field corresponding to the BCD-coded hour counter.

AMPM: AM/PM Indicator

This field is the alarm field corresponding to the BCD-coded hour counter.

HOUREN: Hour Alarm Enable

0: The hour-matching alarm is disabled.

1: The hour-matching alarm is enabled.

33.22.2 PMC System Clock Disable Register

Name: PMC_SCDR

Address: 0xF0014004

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	ISCCK	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	PCK2	PCK1	PCK0

7	6	5	4	3	2	1	0
UDP	UHP	–	–	LCDCK	DDRCK	–	PCK

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

PCK: Processor Clock Disable

0: No effect.

1: Disables the Processor clock. This is used to enter the processor in Idle mode.

DDRCK: DDR Clock Disable

0: No effect.

1: Disables the DDR clock.

LCDCK: MCK2x Clock Disable

0: No effect.

1: Disables the MCK2x clock.

UHP: USB Host OHCI Clock Disable

0: No effect.

1: Disables the UHP48M and UHP12M OHCI clocks.

UDP: USB Device Clock Enable

0: No effect.

1: Disables the USB Device clock.

PCKx: Programmable Clock x Output Disable

0: No effect.

1: Disables the corresponding Programmable Clock output.

ISCCK: ISC Clock Disable

0: No effect.

1: Disables the ISC clock.

34.7.32 Secure PIO Write Protection Status Register

Name: S_PIO_WPSR

Address: 0xFC0395E4

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
WPVSRC							
15	14	13	12	11	10	9	8
WPVSRC							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPVS

WPVS: Write Protection Violation Status

0: No write protection violation has occurred since the last read of the S_PIO_WPSR.

1: A write protection violation has occurred since the last read of the S_PIO_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

WPVSRC: Write Protection Violation Source

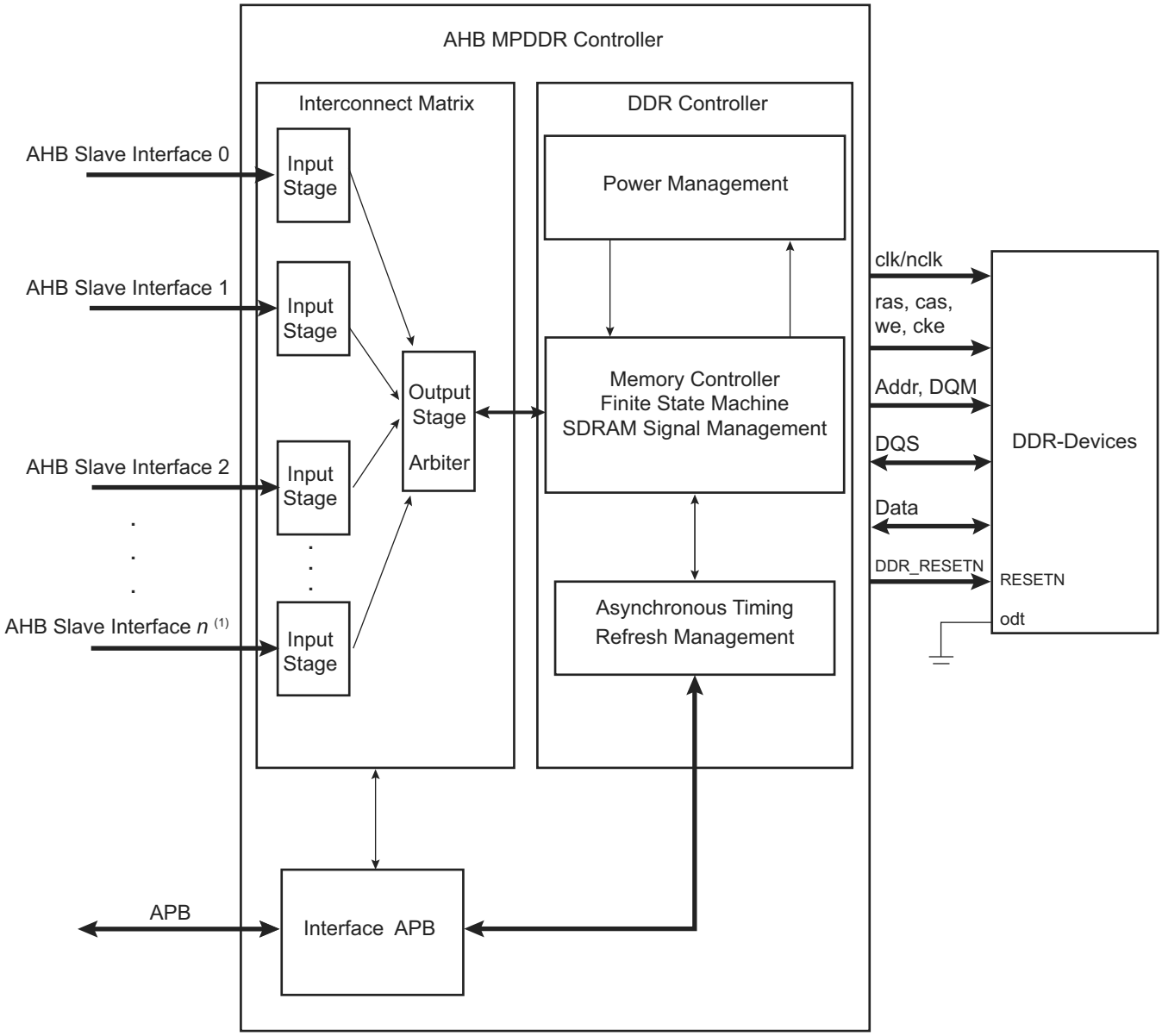
When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

36.3 MPDDRC Module Diagram

The MPDDRC is partitioned in two blocks (see Figure 36-1):

- Interconnect Matrix block that manages concurrent accesses on the AHB bus between four AHB masters and integrates an arbiter
- DDR controller that translates AHB requests (read/write) in the DDR-SDRAM protocol

Figure 36-1: MPDDRC Module Diagram



Note: 1. "*n*" can equal 3 or 7 (value is device-specific).

36.4 Product Dependencies, Initialization Sequence

36.4.1 Low-power DDR1-SDRAM Initialization

The initialization sequence is generated by software.

37.20.18 PMECC Interrupt Status Register

Name: HSMC_PMECCISR

Address: 0xF8014098

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
ERRIS							

ERRIS: Error Interrupt Status Register

When set to one, bit *i* of the HSMC_PMECCISR indicates that sector *i* is corrupted.

39.7.15 LCD Controller Attribute Register

Name: LCDC_ATTR

Address: 0xF000003C

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	PPA2Q	–	HEOA2Q	OVR2A2Q	OVR1A2Q	BASEA2Q
7	6	5	4	3	2	1	0
–	–	PP	–	HEO	OVR2	OVR1	BASE

BASE: Base Layer Update Attribute

0: No effect.

1: Update the BASE window attributes.

OVR1: Overlay 1 Update Attribute

0: No effect.

1: Update the OVR1 window attribute.

OVR2: Overlay 2 Update Attribute

0: No effect.

1: Update the OVR2 window attribute.

HEO: High-End Overlay Update Attribute

0: No effect.

1: Update the HEO window attribute.

PP: Post-Processing Update Attribute

0: No effect.

1: Update the PP window attribute.

BASEA2Q: Base Layer Update Add To Queue

0: No effect.

1: Add the descriptor pointed to by the LCDC_BASEHEAD register to the descriptor list.

OVR1A2Q: Overlay 1 Update Add To Queue

0: No effect.

1: Add the descriptor pointed to by the LCDC_OVR1HEAD register to the descriptor list.

OVR2A2Q: Overlay 2 Update Add to Queue

0: No effect.

1: Add the descriptor pointed to by the LCDC_OVR2HEAD register to the descriptor list.

HEOA2Q: High-End Overlay Update Add To Queue

0: No effect.

1: Add the descriptor pointed to by the LCDC_HEOHEAD register to the descriptor list.

39.7.45 Overlay 1 Configuration Register 0

Name: LCDC_OVR1CFG0

Address: 0xF000016C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	LOCKDIS	ROTDIS	–	–	–	DLBO

7	6	5	4	3	2	1	0
–	–	BLEN		–	–	–	SIF

SIF: Source Interface

0: Base Layer data is retrieved through AHB interface 0.

1: Base Layer data is retrieved through AHB interface 1.

BLEN: AHB Burst Length

Value	Name	Description
0	AHB_BLEN_SINGLE	AHB Access is started as soon as there is enough space in the FIFO to store one data. SINGLE, INCR, INCR4, INCR8 and INCR16 bursts are used. INCR is used for a burst of 2 and 3 beats.
1	AHB_BLEN_INCR4	AHB Access is started as soon as there is enough space in the FIFO to store a total amount of 4 data. An AHB INCR4 Burst is used. SINGLE, INCR and INCR4 bursts are used. INCR is used for a burst of 2 and 3 beats.
2	AHB_BLEN_INCR8	AHB Access is started as soon as there is enough space in the FIFO to store a total amount of 8 data. An AHB INCR8 Burst is used. SINGLE, INCR, INCR4 and INCR8 bursts are used. INCR is used for a burst of 2 and 3 beats.
3	AHB_BLEN_INCR16	AHB Access is started as soon as there is enough space in the FIFO to store a total amount of 16 data. An AHB INCR16 Burst is used. SINGLE, INCR, INCR4, INCR8 and INCR16 bursts are used. INCR is used for a burst of 2 and 3 beats.

DLBO: Defined Length Burst Only for Channel Bus Transaction

0: Undefined length INCR burst is used for a burst of 2 and 3 beats.

1: Only Defined Length burst is used (SINGLE, INCR4, INCR8 and INCR16).

ROTDIS: Hardware Rotation Optimization Disable

0: Rotation optimization is enabled.

1: Rotation optimization is disabled.

LOCKDIS: Hardware Rotation Lock Disable

0: AHB lock signal is asserted when a rotation is performed.

1: AHB lock signal is cleared when a rotation is performed.

Table 40-9: Example of Delay Request Frame in 1588 Version 1 Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–32)	E00001
IP DA (Octet 33)	81 or 82 or 83 or 84
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–42)	—
Version PTP (Octet 43)	01
Other stuff (Octets 44–73)	—
Control (Octet 74)	01
Other stuff (Octets 75–168)	—

For 1588 version 2 messages, the type of frame is determined by looking at the message type field in the first byte of the PTP frame. Whether a frame is version 1 or version 2 can be determined by looking at the version PTP field in the second byte of both version 1 and version 2 PTP frames.

In version 2 messages sync frames have a message type value of 0x0, delay_req have 0x1, Pdelay_Req have 0x2 and Pdelay_Resp have 0x3.

Table 40-10: Example of Sync Frame in 1588 Version 2 (UDP/IPv4) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–33)	E0000181
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–41)	—
Message type (Octet 42)	00
Version PTP (Octet 43)	02

46.7.20 TWIHS FIFO Mode Register

Name: TWIHS_FMR

Address: 0xF8028050 (0), 0xFC028050 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	RXFTHRES					
23	22	21	20	19	18	17	16
–	–	TXFTHRES					
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	RXRDYM		–	–	TXRDYM	

TXRDYM: Transmitter Ready Mode

If FIFOs are enabled, the TXRDY flag (in TWIHS_SR) behaves as follows.

Value	Name	Description
0x0	ONE_DATA	TXRDY will be at level ‘1’ when at least one data can be written in the Transmit FIFO
0x1	TWO_DATA	TXRDY will be at level ‘1’ when at least two data can be written in the Transmit FIFO
0x2	FOUR_DATA	TXRDY will be at level ‘1’ when at least four data can be written in the Transmit FIFO

RXRDYM: Receiver Ready Mode

If FIFOs are enabled, the RXRDY flag (in TWIHS_SR) behaves as follows.

Value	Name	Description
0x0	ONE_DATA	RXRDY will be at level ‘1’ when at least one unread data is in the Receive FIFO
0x1	TWO_DATA	RXRDY will be at level ‘1’ when at least two unread data are in the Receive FIFO
0x2	FOUR_DATA	RXRDY will be at level ‘1’ when at least four unread data are in the Receive FIFO

TXFTHRES: Transmit FIFO Threshold

0–16: Defines the Transmit FIFO threshold value (number of data). TXFTH flag in TWIHS_FSR will be set when Transmit FIFO goes from “above” threshold state to “equal or below” threshold state.

RXFTHRES: Receive FIFO Threshold

0–16: Defines the Receive FIFO threshold value (number of data). RXFTH flag in TWIHS_FSR will be set when Receive FIFO goes from “below” threshold state to “equal or above” threshold state.

47.8 SPI Functional Description

47.8.1 Modes of Operation

The SPI operates in Master mode or in Slave mode.

- The SPI operates in Master mode by writing a 1 to the MSTR bit in the SPI Mode Register (FLEX_SPI_MR):
  - The pins NPCS0 to NPCS1 are all configured as outputs.
  - The SPCK pin is driven.
  - The MISO line is wired on the receiver input.
  - The MOSI line is driven as an output by the transmitter.
- The SPI operates in Slave mode if the MSTR bit in FLEX_SPI_MR is written to 0:
  - The MISO line is driven by the transmitter output.
  - The MOSI line is wired on the receiver input.
  - The SPCK pin is driven by the transmitter to synchronize the receiver.
  - The NPCS0 pin becomes an input, and is used as a slave select signal (NSS).
  - Pin NPCS1 is not are not are not driven and can be used for other purposes.

The data transfers are identically programmable for both modes of operation. The bit rate generator is activated only in Master mode.

47.8.2 Data Transfer

Four combinations of polarity and phase are available for data transfers. The clock polarity is programmed with the CPOL bit in the SPI Chip Select Register (FLEX_SPI_CSR). The clock phase is programmed with the NCPHA bit. These two parameters determine the edges of the clock signal on which data are driven and sampled. Each of the two parameters has two possible states, resulting in four possible combinations that are incompatible with one another. Consequently, a master/slave pair must use the same parameter pair values to communicate. If multiple slaves are connected and require different configurations, the master must reconfigure itself each time it needs to communicate with a different slave.

Table 47-17 shows the four modes and corresponding parameter settings.

Table 47-17: SPI Bus Protocol Mode

SPI Mode	CPOL	NCPHA	Shift SPCK Edge	Capture SPCK Edge	SPCK Inactive Level
0	0	1	Falling	Rising	Low
1	0	0	Rising	Falling	Low
2	1	1	Rising	Falling	High
3	1	0	Falling	Rising	High

Figure 47-65 and Figure 47-66 show examples of data transfers.

56.7.40 PWM Channel Mode Register

Name: PWM_CMRx [x=0..3]

Address: 0xF802C200 [0], 0xF802C220 [1], 0xF802C240 [2], 0xF802C260 [3]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	PPM	DTLI	DTHI	DTE
15	14	13	12	11	10	9	8
–	–	TCTS	DPOLI	UPDS	CES	CPOL	CALG
7	6	5	4	3	2	1	0
–	–	–	–	CPRE			

This register can only be written if bits WPSWS2 and WPHWS2 are cleared in the PWM Write Protection Status Register.

CPRE: Channel Prescaler

Value	Name	Description
0	MCK	Peripheral clock
1	MCK_DIV_2	Peripheral clock/2
2	MCK_DIV_4	Peripheral clock/4
3	MCK_DIV_8	Peripheral clock/8
4	MCK_DIV_16	Peripheral clock/16
5	MCK_DIV_32	Peripheral clock/32
6	MCK_DIV_64	Peripheral clock/64
7	MCK_DIV_128	Peripheral clock/128
8	MCK_DIV_256	Peripheral clock/256
9	MCK_DIV_512	Peripheral clock/512
10	MCK_DIV_1024	Peripheral clock/1024
11	CLKA	Clock A
12	CLKB	Clock B

CALG: Channel Alignment

0: The period is left-aligned.

1: The period is center-aligned.

CPOL: Channel Polarity

0: The OCx output waveform (output from the comparator) starts at a low level.

1: The OCx output waveform (output from the comparator) starts at a high level.

65.6.15 Touchscreen

65.6.15.1 Touchscreen Mode

The TSMODE parameter of the ADC Touchscreen Mode register (ADC_TSMR) is used to enable/disable the touchscreen functionality, to select the type of screen (4-wire or 5-wire) and, in the case of a 4-wire screen and to activate (or not) the pressure measurement.

In 4-wire mode, channel 0, 1, 2 and 3 must not be used for classic ADC conversions. Likewise, in 5-wire mode, channel 0, 1, 2, 3, and 4 must not be used for classic ADC conversions.

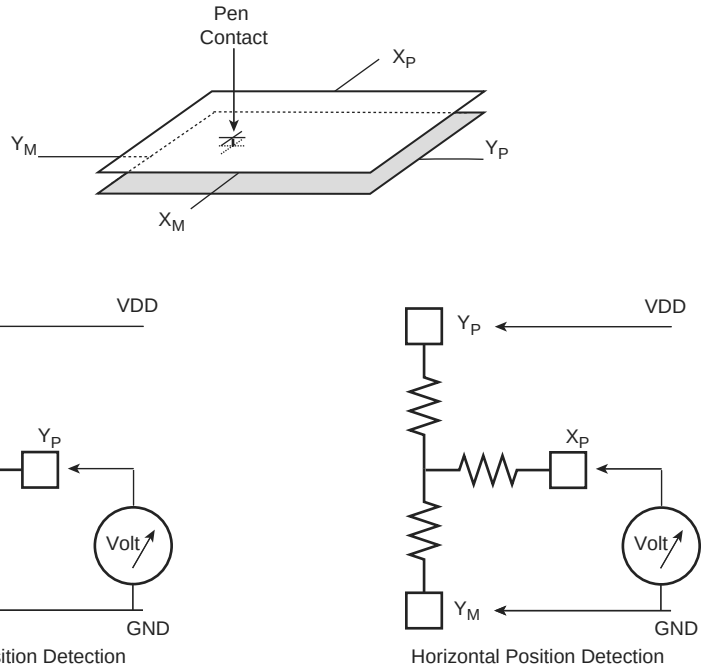
65.6.15.2 4-wire Resistive Touchscreen Principles

A resistive touchscreen is based on two resistive films, each one being fitted with a pair of electrodes, placed at the top and bottom on one film, and on the right and left on the other. In between, there is a layer acting as an insulator, but also enables contact when you press the screen. This is illustrated in Figure 65-14.

The ADC controller can perform the following tasks without external components:

- position measurement
- pressure measurement
- pen detection

Figure 65-14: Touchscreen Position Measurement



65.6.15.3 4-wire Position Measurement Method

As shown in Figure 65-14, to detect the position of a contact, a supply is first applied from top to bottom. Due to the linear resistance of the film, there is a voltage gradient from top to bottom. When a contact is performed on the screen, the voltage propagates at the point the two surfaces come into contact with the second film. If the input impedance on the right and left electrodes sense is high enough, the film does not affect this voltage, despite its resistive nature.

For the horizontal direction, the same method is used, but by applying supply from left to right. The range depends on the supply voltage and on the loss in the switches that connect to the top and bottom electrodes.

In an ideal world (linear, with no loss through switches), the horizontal position is equal to:

VY_M / VDD or VY_P / VDD.

The implementation with on-chip power switches is shown in Figure 65-15. The voltage measurement at the output of the switch compensates for the switches loss.

It is possible to correct for switch loss by performing the operation:

66. Electrical Characteristics

66.1 Absolute Maximum Ratings

Table 66-1: Absolute Maximum Ratings*

Storage Temperature . . . . . -60°C to + 150°C
Voltage on Input Pins with Respect to Ground . . . . . .-0.3V to +4.0V
Maximum Operating Voltage VDDCORE, VDDPLLA, VDDUTMIC and VDDHSIC 1.5V
VDDIODDR. 2.0V
VDDBU 4.0V
VDDIOPx, VDDUTMII, VDDISC, VDDSDMMC, VDDOSC, VDDANA, VDDAUDIOPLL 4.0V
VDDFUSE. 3.0V
Total DC Output Current on all I/O lines . . . . . .350 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

66.2 DC Characteristics

The following characteristics are applicable to the operating temperature range T_A = -40°C to +105°C, unless otherwise specified.

Table 66-2: Recommended Thermal Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A	Operating Temperature	–	-40	–	+105	°C
T_J	Junction Temperature	–	-40	–	+125	°C
R_{thJA}	Junction-to-ambient thermal resistance	LFBGA289	–	34.8	–	°C/W
		TFBGA256	–	27.4	–	
		TFBGA196	–	44.6	–	
R_{thJC}	Junction-to-case thermal resistance	LFBGA289	–	10.9	–	°C/W
		TFBGA256	–	9.3	–	
		TFBGA196	–	11.2	–	
P_D	Power Dissipation	At T_A = 85°C, LFBGA289	–	–	1149	mW
		At T_A = 105°C, LFBGA289	–	–	575	mW
P_D	Power Dissipation	At T_A = 85°C, TFBGA256	–	–	1460	mW
		At T_A = 105°C, TFBGA256	–	–	730	mW
P_D	Power Dissipation	At T_A = 85°C, TFBGA196	–	–	897	mW
		At T_A = 105°C, TFBGA196	–	–	448	mW

Figure 66-23: SPI Slave Mode - NPCS Timings

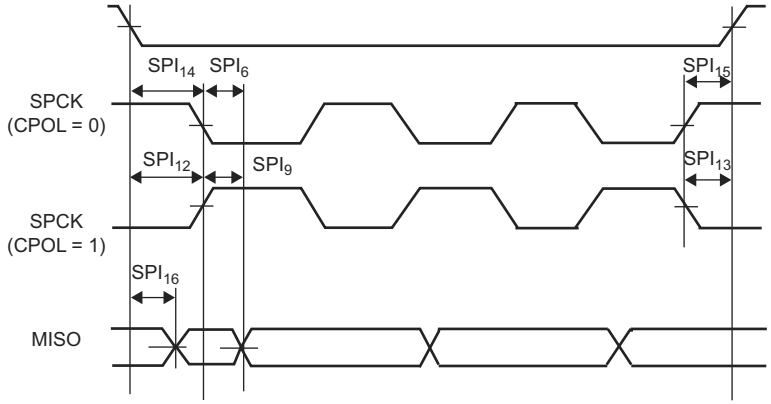


Table 66-64: SPI0 IOSET1 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
	Master Mode					
SPI_0	MISO Setup time before SPCK rises	14.3	–	12.4	–	ns
SPI_1	MISO Hold time after SPCK rises	0	–	0	–	ns
SPI_2	SPCK rising to MOSI	0	1.9	0	2.4	ns
SPI_3	MISO Setup time before SPCK falls	13.8	–	12.6	–	ns
SPI_4	MISO Hold time after SPCK falls	0	–	0	–	ns
SPI_5	SPCK falling to MOSI	0	1.2	0	2.3	ns
	Slave Mode					
SPI_6	SPCK falling to MISO	10.5	12.6	8.4	10.9	ns
SPI_7	MOSI Setup time before SPCK rises	1.5	–	1.4	–	ns
SPI_8	MOSI Hold time after SPCK rises	1.7	–	1.5	–	ns
SPI_9	SPCK rising to MISO	10	12	8	10.2	ns
SPI_{10}	MOSI Setup time before SPCK falls	1.5	–	1.4	–	ns
SPI_{11}	MOSI Hold time after SPCK falls	1.7	–	1.5	–	ns
SPI_{12}	NPCS0 setup to SPCK rising	4.4	–	4.3	–	ns
SPI_{13}	NPCS0 hold after SPCK falling	1.5	–	1.3	–	ns
SPI_{14}	NPCS0 setup to SPCK falling	3.9	–	3.9	–	ns
SPI_{15}	NPCS0 hold after SPCK rising	0.8	–	0.5	–	ns
SPI_{16}	NPCS0 falling to MISO valid	13.3	–	11.7	–	ns

Table 72-5: SAMA5D2 Datasheet Rev. 11267C Revision History (Continued)

Issue Date	Changes
8-Jan-16	Section 41. “Inter-IC Sound Controller (I2SC)”
	Section 41.6.3 “Master, Controller and Slave Modes”: removed text fragment: ‘in order to avoid unwanted glitches on the I2SWS and I2SCK pins.’
	Section 41.8.2 “Inter-IC Sound Controller Mode Register”: removed text fragment: ‘in order to avoid unexpected behavior on the I2SWS, I2SCK and I2SDO outputs.’ and added note (2) below IMCKDIV field description.
	Section 44. “Flexible Serial Communication Controller (FLEXCOM)”
	Restored all references to ISO7816 specification
	Updated Figure 44-3 “Fractional Baud Rate Generator”
	Added Figure 44-27 “RTS line software control when FLEX_US_MR.USART_MODE = 2”
	Section 44.10.6 “USART Mode Register”: updated USART_MODE field description (SPI_MASTER item)
	Section 44.10.44 “SPI Mode Register”: added LBHPC bit
	Section 55. “Universal Asynchronous Receiver Transmitter (UART)”
	Section 55.6.9 “UART Baud Rate Generator Register”: in CD field description, corrected equation after “If BRSRCCK = 1”
	Section 59. “Quad SPI Interface (QSPI)”
	Section 59.7.5 “QSPI Status Register”: updated RDRF, TDRE, TXEMPTY, and OVRES field descriptions
	Section 48. “Secure Digital Multimedia Card Controller (SDMMC)”
	Section 48.12.41 “SDMMC Preset Value Register”: updated CLKGSEL field description
	Section 49. “Image Sensor Controller (ISC)”
	Section 49.1 “Description”: removed "serial csi-2 based CMOS/CCD sensor" (not supported).
	Section 50. “Controller Area Network (MCAN)”
	Changed MCAN interrupt line names to MCAN_INT0 and MCAN_INT1 thoughout the section
	Section 50.6.7 “MCAN CC Control Register”: added bit NISO
	Section 51. “Timer Counter (TC)”
	Reformatted and renamed Table 51-2 “Channel Signal Description”
	Section 51.6.3 “Clock Selection”: updated notes (1) and (2)
	Section 52. “Pulse Density Modulation Interface Controller (PDMIC)”
	Replaced all instances of “PCK” with “GCLK”
	Section 52.2 “Embedded Characteristics”: removed ‘Multiplexed PDM Input Support’ characteristic
	Updated Section 52.5.2 “Power Management” and Section 52.6.2.1 “Description”
	Section 52.6.2.6 “Gain and Offset Compensation”: updated *dgain* bullet
	Section 52.7.3 “PDMIC Converted Data Register”: updated DATA field description
	Section 52.7.8 “PDMIC DSP Configuration Register 0”: updated OSR field description
	Section 61. “Security Module”
	Section 61.5.5 “SECUMOD Status Clear Register”: removed MCKM field description
	Section 61.5.18 “SECUMOD Wake Up Register”: removed TPML field description
	Section 77. “Analog-to-Digital Converter (ADC)”
	Section 77.7.2 “ADC Mode Register”: updated TRACKTIM and TRANSFER field descriptions.