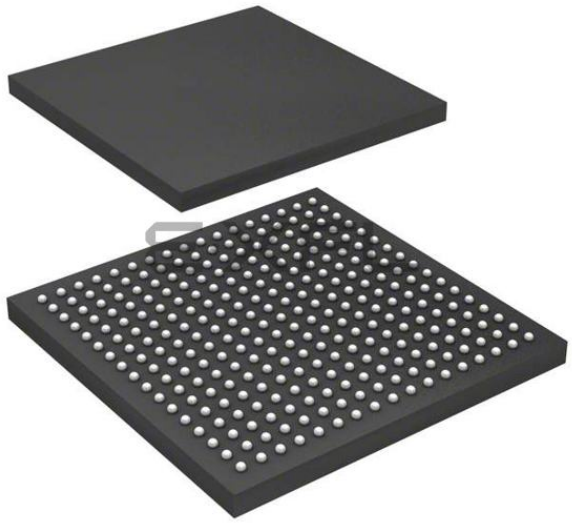

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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d26c-cur

13. ARM Cortex-A5

13.1 Description

The ARM Cortex-A5 processor is a high-performance, low-power, ARM macrocell with an L1 cache subsystem that provides full virtual memory capabilities. The Cortex-A5 processor implements the ARMv7 architecture and runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java™ byte codes in Jazelle® state.

The Cortex-A5 NEON Media Processing Engine (MPE) extends the Cortex-A5 functionality to provide support for the ARM v7 Advanced SIMD v2 and *Vector Floating-Point v4* (VFPv4) instruction sets. The Cortex-A5 NEON MPE provides flexible and powerful acceleration for signal processing algorithms including multimedia such as image processing, video decode/encode, 2D/3D graphics, and audio. See the *Cortex-A5 NEON Media Processing Engine Technical Reference Manual*.

The Cortex-A5 processor includes TrustZone® technology to enhance security by partitioning the SoC's hardware and software resources in a Secure world for the security subsystem and a Normal world for the rest, enabling a strong security perimeter to be built between the two. See *Security Extensions overview* in the *Cortex-A5 Technical Reference Manual*. See the *ARM Architecture Reference Manual* for details on how TrustZone works in the architecture.

Note: All ARM publications referenced in this datasheet can be found at www.arm.com.

13.1.1 Power Management

The Cortex-A5 design supports the following main levels of power management:

- Run Mode
- Standby Mode

13.1.1.1 Run Mode

Run mode is the normal mode of operation where all of the processor functionality is available. Everything, including core logic and embedded RAM arrays, is clocked and powered up.

13.1.1.2 Standby Mode

Standby mode disables most of the clocks of the processor, while keeping it powered up. This reduces the power drawn to the static leakage current, plus a small clock power overhead required to enable the processor to wake up from Standby mode. The transition from Standby mode to Run mode is caused by one of the following:

- the arrival of an interrupt, either masked or unmasked
- the arrival of an event, if standby mode was initiated by a Wait for Event (WFE) instruction
- a debug request, when either debug is enabled or disabled
- a reset.

13.5.3.2 Main TLB

Misses from the instruction and data micro TLBs are handled by a unified main TLB. Accesses to the main TLB take a variable number of cycles, according to competing requests from each of the micro TLBs and other implementation-dependent factors.

The main TLB is 128-entry two-way set-associative.

TLB match process

Each TLB entry contains a virtual address, a page size, a physical address, and a set of memory properties. Each is marked as being associated with a particular application space (ASID), or as global for all application spaces. The CONTEXTIDR determines the currently selected application space.

A TLB entry matches when these conditions are true:

- Its virtual address matches that of the requested address.
- Its Non-secure TLB ID (NSTID) matches the Secure or Non-secure state of the MMU request.
- Its ASID matches the current ASID in the CONTEXTIDR or is global.

The operating system must ensure that, at most, one TLB entry matches at any time. The TLB can store entries based on the following block sizes:

Supersections	Describe 16 Mbyte blocks of memory
Sections	Describe 1 Mbyte blocks of memory
Large pages	Describe 64 Kbyte blocks of memory
Small pages	Describe 4 Kbyte blocks of memory

Supersections, sections and large pages are supported to permit mapping of a large region of memory while using only a single entry in the TLB. If no mapping for an address is found within the TLB, then the translation table is automatically read by hardware and a mapping is placed in the TLB.

13.5.4 Memory Access Sequence

When the processor generates a memory access, the MMU:

1. Performs a lookup for the requested virtual address and current ASID and security state in the relevant instruction or data micro TLB.
2. If there is a miss in the micro TLB, performs a lookup for the requested virtual address and current ASID and security state in the main TLB.
3. If there is a miss in main TLB, performs a hardware translation table walk.

The MMU can be configured to perform hardware translation table walks in cacheable regions by setting the IRGN bits in Translation Table Base Register 0 and Translation Table Base Register 1. If the encoding of the IRGN bits is write-back, an L1 data cache lookup is performed and data is read from the data cache. If the encoding of the IRGN bits is write-through or non-cacheable, an access to external memory is performed. For more information, see *Cortex-A5 Technical Reference Manual*.

The MMU might not find a global mapping, or a mapping for the currently selected ASID, with a matching Non-secure TLB ID (NSTID) for the virtual address in the TLB. In this case, the hardware does a translation table walk if the translation table walk is enabled by the PD0 or PD1 bit in the Translation Table Base Control Register. If translation table walks are disabled, the processor returns a Section Translation fault. For more information, see *Cortex-A5 Technical Reference Manual*.

If the TLB finds a matching entry, it uses the information in the entry as follows:

1. The access permission bits and the domain determine if the access is enabled. If the matching entry does not pass the permission checks, the MMU signals a memory abort. See the *ARM Architecture Reference Manual, ARMv7-A and ARMv7-R edition* for a description of access permission bits, abort types and priorities, and for a description of the Instruction Fault Status Register (IFSR) and Data Fault Status Register (DFSR).
2. The memory region attributes specified in both the TLB entry and the CP15 c10 remap registers determine if the access is
   - Secure or Non-secure
   - Shared or not
   - Normal memory, Device, or Strongly-ordered

For more information, see *Cortex-A5 Technical Reference Manual*, Memory region remap.

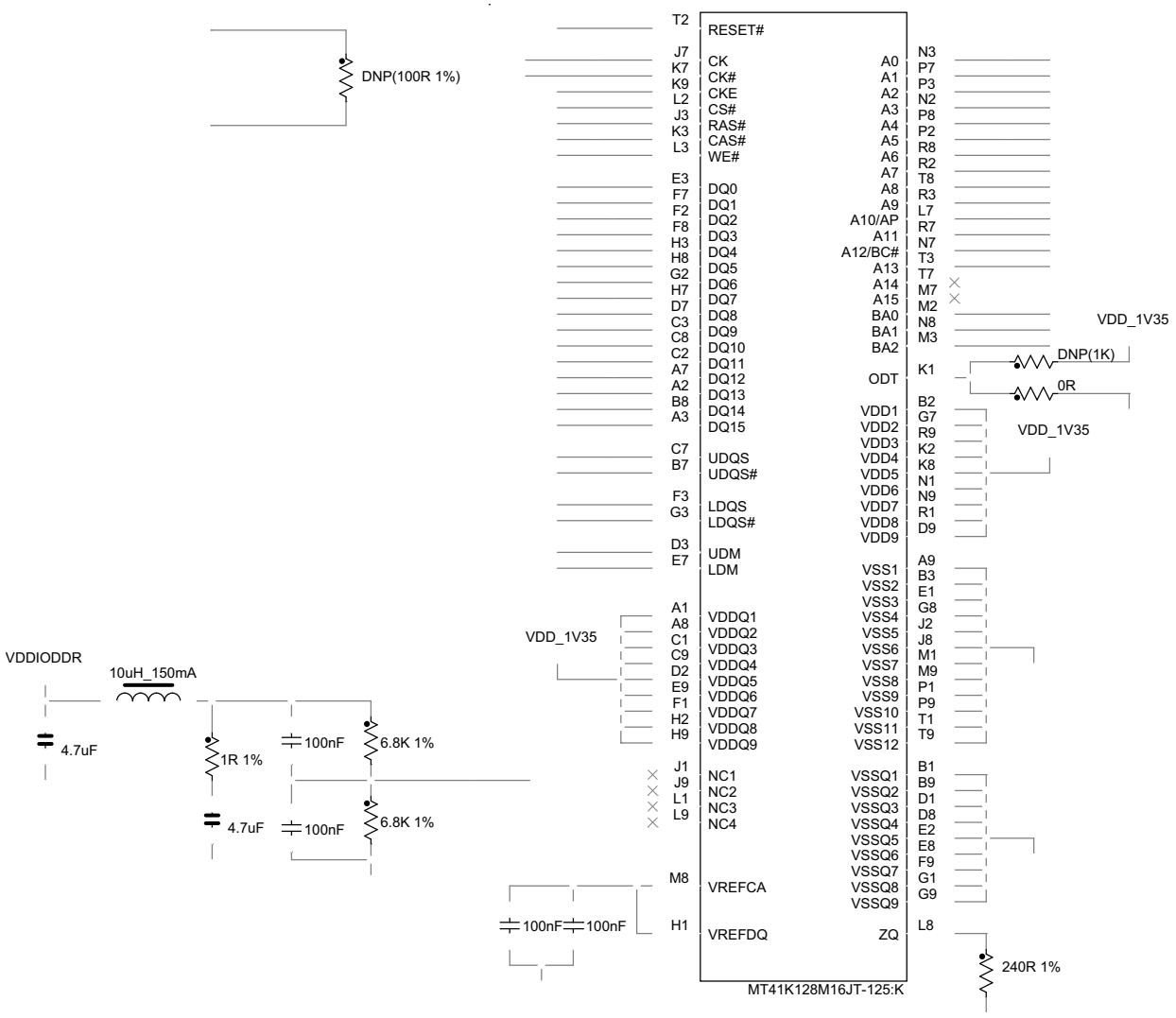
3. The TLB translates the virtual address to a physical address for the memory access.

Table 18-10: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x016C	Master 3 Error Address Register	MATRIX_MEAR3	Read-only	0x00000000
0x0170	Master 4 Error Address Register	MATRIX_MEAR4	Read-only	0x00000000
0x0174	Master 5 Error Address Register	MATRIX_MEAR5	Read-only	0x00000000
0x0178	Master 6 Error Address Register	MATRIX_MEAR6	Read-only	0x00000000
0x017C	Master 7 Error Address Register	MATRIX_MEAR7	Read-only	0x00000000
0x0180	Master 8 Error Address Register	MATRIX_MEAR8	Read-only	0x00000000
0x0184	Master 9 Error Address Register	MATRIX_MEAR9	Read-only	0x00000000
0x0188	Master 10 Error Address Register	MATRIX_MEAR10	Read-only	0x00000000
0x018C	Master 11 Error Address Register	MATRIX_MEAR11	Read-only	0x00000000
0x0190–0x01E0	Reserved	–	–	–
0x01E4	Write Protection Mode Register	MATRIX_WPMR	Read/Write	0x00000000
0x01E8	Write Protection Status Register	MATRIX_WPSR	Read-only	0x00000000
0x01EC–0x01FC	Reserved	–	–	–
0x0200	Security Slave 0 Register	MATRIX_SSR0	Read/Write	0x00000000
0x0204	Security Slave 1 Register	MATRIX_SSR1	Read/Write	0x00000000
0x0208	Security Slave 2 Register	MATRIX_SSR2	Read/Write	0x00000000
0x020C	Security Slave 3 Register	MATRIX_SSR3	Read/Write	0x00000000
0x0210	Security Slave 4 Register	MATRIX_SSR4	Read/Write	0x00000000
0x0214	Security Slave 5 Register	MATRIX_SSR5	Read/Write	0x00000000
0x0218	Security Slave 6 Register	MATRIX_SSR6	Read/Write	0x00000000
0x021C	Security Slave 7 Register	MATRIX_SSR7	Read/Write	0x00000000
0x0220	Security Slave 8 Register	MATRIX_SSR8	Read/Write	0x00000000
0x0224	Security Slave 9 Register	MATRIX_SSR9	Read/Write	0x00000000
0x0228	Security Slave 10 Register	MATRIX_SSR10	Read/Write	0x00000000
0x022C	Security Slave 11 Register	MATRIX_SSR11	Read/Write	0x00000000
0x0230	Security Slave 12 Register	MATRIX_SSR12	Read/Write	0x00000000
0x0234	Security Slave 13 Register	MATRIX_SSR13	Read/Write	0x00000000
0x0238	Security Slave 14 Register	MATRIX_SSR14	Read/Write	0x00000000
0x023C	Reserved	–	–	–
0x0240	Security Areas Split Slave 0 Register	MATRIX_SASSR0	Read/Write	(1)
0x0244	Security Areas Split Slave 1 Register	MATRIX_SASSR1	Read/Write	(1)
0x0248	Security Areas Split Slave 2 Register	MATRIX_SASSR2	Read/Write	(1)
0x024C	Security Areas Split Slave 3 Register	MATRIX_SASSR3	Read/Write	(1)
0x0250	Security Areas Split Slave 4 Register	MATRIX_SASSR4	Read/Write	(1)
0x0254	Security Areas Split Slave 5 Register	MATRIX_SASSR5	Read/Write	(1)
0x0258	Security Areas Split Slave 6 Register	MATRIX_SASSR6	Read/Write	(1)

35.1.5.3 16-bit DDR3/DDR3L

Figure 35-5: 16-bit DDR3/DDR3L Hardware Configuration



37.18.1 MLC/SLC Write Page Operation Using PMECC

When an MLC write page operation is performed, the PMECC controller is configured with the NANDWR bit of the PMECCFG register set to one. When the NAND spare area contains file system information and redundancy (PMECCx), the spare area is error protected, then the SPAREEN bit of the PMECCFG register is set. When the NAND spare area contains only redundancy information, the SPAREEN bit is cleared.

When the write page operation is terminated, the user writes the redundancy in the NAND spare area. This operation can be done with DMA assistance.

Table 37-14: Relevant Redundancy Registers

BCH_ERR Field	Sector Size Set to 512 Bytes	Sector Size Set to 1024 Bytes
0	PMECC0	PMECC0
1	PMECC0, PMECC1	PMECC0, PMECC1
2	PMECC0, PMECC1, PMECC2, PMECC3	PMECC0, PMECC1, PMECC2, PMECC3
3	PMECC0, PMECC1, PMECC2, PMECC3, PMECC4, PMECC5, PMECC6	PMECC0, PMECC1, PMECC2, PMECC3, PMECC4, PMECC5, PMECC6
4	PMECC0, PMECC1, PMECC2, PMECC3, PMECC4, PMECC5, PMECC6, PMECC7, PMECC8, PMECC9	PMECC0, PMECC1, PMECC2, PMECC3, PMECC4, PMECC5, PMECC6, PMECC7, PMECC8, PMECC9, PMECC10
5	PMECC0, PMECC1, PMECC2, PMECC3, PMECC4, PMECC5, PMECC6, PMECC7, PMECC8, PMECC9, PMECC10, PMECC11, PMECC12	PMECC0, PMECC1, PMECC2, PMECC3, PMECC4, PMECC5, PMECC6, PMECC7, PMECC8, PMECC9, PMECC10, PMECC11, PMECC12, PMECC13

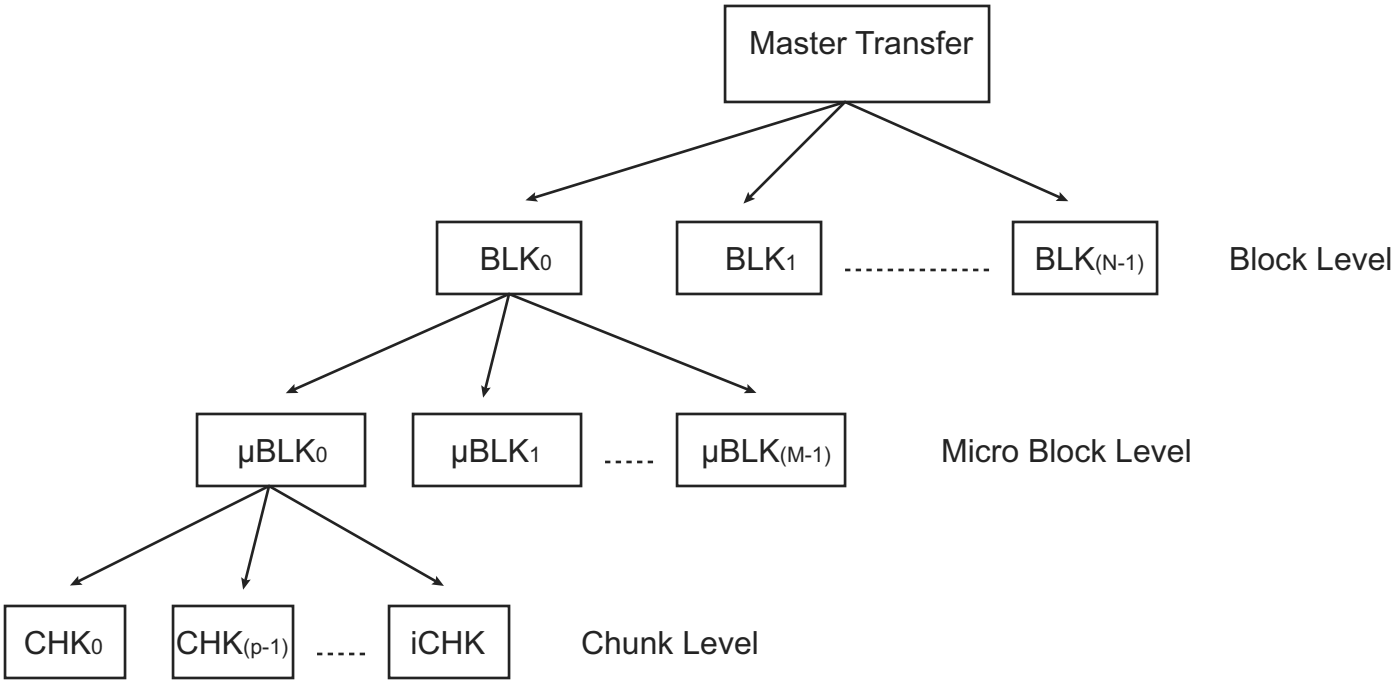
Table 37-15: Number of Relevant ECC Bytes per Sector, Copied from LSByte to MSByte

BCH_ERR Field	Sector Size Set to 512 Bytes	Sector Size Set to 1024 Bytes
0	4 bytes	4 bytes
1	7 bytes	7 bytes
2	13 bytes	14 bytes
3	20 bytes	21 bytes
4	39 bytes	42 bytes
5	52 bytes	56 bytes

37.18.1.1 SLC/MLC Write Operation with Spare Enable Bit Set

When the SPAREEN bit of the PMECCFG register is set, the spare area of the page is encoded with the stream of data of the last sector of the page. This mode is entered by setting the DATA bit of the PMECCTRL register. When the encoding process is over, the redundancy shall be written to the spare area in User mode. The USER bit of the PMECCTRL register must be set.

Figure 38-3: XDAMC Peripheral Transfer Hierarchy



39.7.23 Base DMA Head Register

Name: LCDC_BASEHEAD

Address: 0xF000005C

Access: Read/Write

31	30	29	28	27	26	25	24
HEAD							

23	22	21	20	19	18	17	16
HEAD							

15	14	13	12	11	10	9	8
HEAD							

7	6	5	4	3	2	1	0
HEAD						–	–

HEAD: DMA Head Pointer

The Head Pointer points to a new descriptor.

39.7.150 Post Processing Configuration Register 2

Name: LCDC_PPCFG2

Address: 0xF0000574

Access: Read/Write

31	30	29	28	27	26	25	24
XSTRIDE							

23	22	21	20	19	18	17	16
XSTRIDE							

15	14	13	12	11	10	9	8
XSTRIDE							

7	6	5	4	3	2	1	0
XSTRIDE							

XSTRIDE: Horizontal Stride

XSTRIDE represents the memory offset, in bytes, between two rows of the image memory.

40.8.5 GMAC DMA Configuration Register

Name: GMAC_DCFGR

Address: 0xF8008010

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	DDRP

23	22	21	20	19	18	17	16
DRBS							

15	14	13	12	11	10	9	8
–	–	–	–	TXCOEN	TXPBMS	RXBMS	

7	6	5	4	3	2	1	0
ESPA	ESMA	–	FBLDO				

FBLDO: Fixed Burst Length for DMA Data Operations:

Selects the burst length to attempt to use on the AHB when transferring frame data. Not used for DMA management operations and only used where space and data size allow. Otherwise SINGLE type AHB transfers are used.

One-hot priority encoding enforced automatically on register writes as follows, where ‘x’ represents don’t care:

Value	Name	Description
0	–	Reserved
1	SINGLE	00001: Always use SINGLE AHB bursts
2	–	Reserved
4	INCR4	001xx: Attempt to use INCR4 AHB bursts (Default)
8	INCR8	01xxx: Attempt to use INCR8 AHB bursts
16	INCR16	1xxxx: Attempt to use INCR16 AHB bursts

ESMA: Endian Swap Mode Enable for Management Descriptor Accesses

When set, selects swapped endianism for AHB transfers. When clear, selects little endian mode.

ESPA: Endian Swap Mode Enable for Packet Data Accesses

When set, selects swapped endianism for AHB transfers. When clear, selects little endian mode.

RXBMS: Receiver Packet Buffer Memory Size Select

The default receive packet buffer size is 4 Kbytes. The table below shows how to configure this memory to FULL, HALF, QUARTER or EIGHTH of the default size.

Value	Name	Description
0	EIGHTH	4/8 Kbyte Memory Size
1	QUARTER	4/4 Kbytes Memory Size
2	HALF	4/2 Kbytes Memory Size
3	FULL	4 Kbytes Memory Size

40.8.34 GMAC Wake on LAN Register

Name: GMAC_WOL

Address: 0xF80080B8

Access: Read/Write

31	30	29	28	27	26	25	24
–							

23	22	21	20	19	18	17	16
–				MTI	SA1	ARP	MAG

15	14	13	12	11	10	9	8
IP							

7	6	5	4	3	2	1	0
IP							

IP: ARP Request IP Address

Wake on LAN ARP request IP address. Written to define the least significant 16 bits of the target IP address that is matched to generate a Wake on LAN event. A value of zero will not generate an event, even if this is matched by the received frame.

MAG: Magic Packet Event Enable

Wake on LAN magic packet event enable.

ARP: ARP Request Event Enable

Wake on LAN ARP request event enable.

SA1: Specific Address Register 1 Event Enable

Wake on LAN Specific Address Register 1 event enable.

MTI: Multicast Hash Event Enable

Wake on LAN multicast hash event enable.

40.8.64 GMAC Late Collisions Register

Name: GMAC_LC

Address: 0xF8008144

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	LCOL	

7	6	5	4	3	2	1	0
LCOL							

LCOL: Late Collisions

This register counts the number of late collisions occurring after the slot time (512 bits) has expired. In 10/100 mode, late collisions are counted twice i.e., both as a collision and a late collision.

47.8 SPI Functional Description

47.8.1 Modes of Operation

The SPI operates in Master mode or in Slave mode.

- The SPI operates in Master mode by writing a 1 to the MSTR bit in the SPI Mode Register (FLEX_SPI_MR):
  - The pins NPCS0 to NPCS1 are all configured as outputs.
  - The SPCK pin is driven.
  - The MISO line is wired on the receiver input.
  - The MOSI line is driven as an output by the transmitter.
- The SPI operates in Slave mode if the MSTR bit in FLEX_SPI_MR is written to 0:
  - The MISO line is driven by the transmitter output.
  - The MOSI line is wired on the receiver input.
  - The SPCK pin is driven by the transmitter to synchronize the receiver.
  - The NPCS0 pin becomes an input, and is used as a slave select signal (NSS).
  - Pin NPCS1 is not are not are not driven and can be used for other purposes.

The data transfers are identically programmable for both modes of operation. The bit rate generator is activated only in Master mode.

47.8.2 Data Transfer

Four combinations of polarity and phase are available for data transfers. The clock polarity is programmed with the CPOL bit in the SPI Chip Select Register (FLEX_SPI_CSR). The clock phase is programmed with the NCPHA bit. These two parameters determine the edges of the clock signal on which data are driven and sampled. Each of the two parameters has two possible states, resulting in four possible combinations that are incompatible with one another. Consequently, a master/slave pair must use the same parameter pair values to communicate. If multiple slaves are connected and require different configurations, the master must reconfigure itself each time it needs to communicate with a different slave.

Table 47-17 shows the four modes and corresponding parameter settings.

Table 47-17: SPI Bus Protocol Mode

SPI Mode	CPOL	NCPHA	Shift SPCK Edge	Capture SPCK Edge	SPCK Inactive Level
0	0	1	Falling	Rising	Low
1	0	0	Rising	Falling	Low
2	1	1	Rising	Falling	High
3	1	0	Falling	Rising	High

Figure 47-65 and Figure 47-66 show examples of data transfers.

47.10.39 USART FIFO Interrupt Mask Register

Name: FLEX_US_FIMR

Address: 0xF80342B0 (0), 0xF80382B0 (1), 0xFC0102B0 (2), 0xFC0142B0 (3), 0xFC0182B0 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	RXFTHF2	–
7	6	5	4	3	2	1	0
RXFPTEF	TXFPTEF	RXFTHF	RXFFF	RXFEF	TXFTHF	TXFFF	TXFEF

TXFEF: TXFEF Interrupt Mask

TXFFF: TXFFF Interrupt Mask

TXFTHF: TXFTHF Interrupt Mask

RXFEF: RXFEF Interrupt Mask

RXFFF: RXFFF Interrupt Mask

RXFTHF: RXFTHF Interrupt Mask

TXFPTEF: TXFPTEF Interrupt Mask

RXFPTEF: RXFPTEF Interrupt Mask

RXFTHF2: RXFTHF2 Interrupt Mask

51.13.39 SDMMC ADMA Error Status Register

Name: SDMMC_AESR

Access: Read-only

7	6	5	4	3	2	1	0
–	–	–	–	–	LMIS	ERRST	

ERRST: ADMA Error State

This field indicates the state of ADMA when an error has occurred during an ADMA data transfer. This field never indicates 2 because ADMA never stops in this state.

Value	ADMA Error State when Error Occurred	Content of SDMMC_ASARx Registers
0	ST_STOP (Stop DMA)	Points to the descriptor following the error descriptor
1	ST_FDS (Fetch Descriptor)	Points to the error descriptor
2	–	(Not used)
3	ST_TRF (Transfer Data)	Points to the descriptor following the error descriptor

LMIS: ADMA Length Mismatch Error

This error occurs in the following two cases:

- While Block Count Enable (BCEN) is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count (BLKCNT) and Transfer Block Size (BLKSIZE).
- The total data length cannot be divided by the Transfer Block Size (BLKSIZE).

0: No error.

1: Error.

56.7.5 PWM Interrupt Enable Register 1

Name: PWM_IER1

Address: 0xF802C010

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	FCHID3	FCHID2	FCHID1	FCHID0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

CHIDx: Counter Event on Channel x Interrupt Enable

FCHIDx: Fault Protection Trigger on Channel x Interrupt Enable

64.5 Functional Description

64.5.1 Memory Mapping

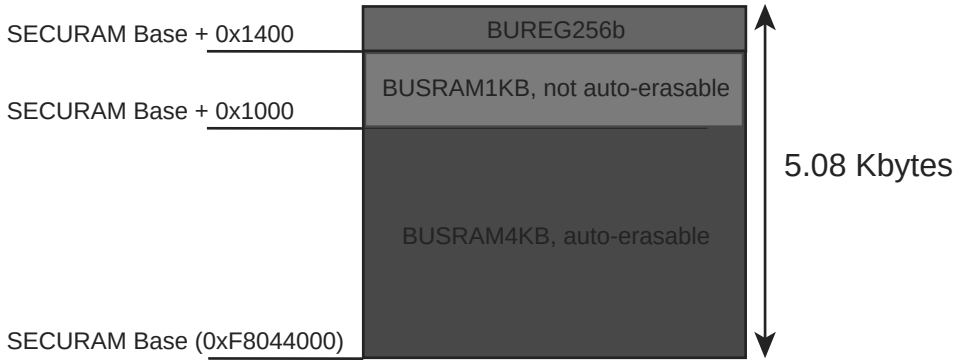
The SECUMOD embeds 5 Kbytes of SRAM split in two parts: the lower 4 Kbytes are erased in case of intrusion (BUSRAM4KB) while the upper 1 Kbyte is never erased (BUSRAM1KB). A 256-bit register bank is available as an additional memory and is totally erased in case of intrusion (BUREG256b).

All memories support 8-bit, 16-bit and 32-bit access sizes.

For power optimization, the transfers between the processor and these memories are decreased by a factor of 4.

The base address value of the SECURAM is 0xF8044000.

Figure 64-2: SECUMOD Internal Memory Map



64.5.2 Scrambling Keys

The secure memories (BUSRAM4KB, BUSRAM1KB and BUREG256b) are scrambled. The scrambling is enabled after reset and a scrambling key is automatically generated. The scrambling key can be modified through the Scrambling Key register (SECUMOD_SCRKEY).

Scrambling can be disabled using the Control register (SECUMOD_CR).

64.5.3 Internal Random Number Generator (IRNG)

The RNG cannot be read through the User Interface (a TrueRNG external to the SECUMOD is available for this purpose).

AUTOBKP: Automatic Backup Mode Enabled (RO)

0: Disabled.

1: Enabled.

SCRAMB: Scrambling Enabled (RO)

0: Disabled.

1: Enabled.

NOPEN: No Pen Contact (cleared on read)

0: No loss of pen contact since the last read of ADC_ISR.

1: At least one loss of pen contact since the last read of ADC_ISR.

PENS: Pen Detect Status

0: The pen does not press the screen.

1: The pen presses the screen.

Note: PENS is not a source of interruption.

66.7 Oscillator Characteristics

66.7.1 Main Oscillator Characteristics

Table 66-17: 8 to 24 MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	FREQ[2] = 00, 11 FREQ = 01 FREQ = 10	8 12 16	–	12 16 24	MHz
–	Duty Cycle	–	40	50	60	%
t_{START}	Startup Time	FREQ[2] = 00, 11 FREQ = 01 FREQ = 10	–	–	18.5 10.5 6	ms
I_{DDON}	Current Consumption (on VDDIO)	@ 12 MHz @ 24 MHz	–	1.2 1.7	3.5 4	mA
I_{DD_STDBY}	Standby Current	–	–	0.02	0.1	µA
C_{PARA}	Internal Parasitic Capacitance[1]	From XIN to XOUT	1.4	1.6	1.8	pF
P_{ON}	Drive level	FREQ = 00 FREQ = 01, 11 FREQ = 10	–	–	150 300 400	µW

Notes: 1. The external capacitors value can be determined by using the following formula:

$C_{LEXT} = (2 \times C_{CRYSTAL}) - C_{BOARD} - (C_{PARA} \times 2)$

where:

C_{LEXT}: external capacitor value which must be soldered from XIN to GND and XOUT to GND

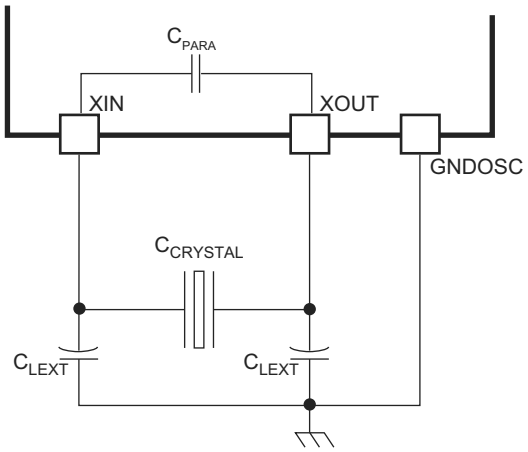
$C_{CRYSTAL}$: crystal targeted load

C_{BOARD}: external board parasitic capacitance (from XIN to GND or XOUT to GND)

C_{PARA}: internal parasitic capacitance

2. The SFR_UTMICKTRIM.FREQ field defines the input frequency for the UTMI and the main oscillator. It is important to select the correct FREQ value because this has a direct influence on USB frequency.

Figure 66-3: Main Oscillator Schematics



72. Revision History

Table 72-1: SAMA5D2 Datasheet DS60001476 Rev. B Revision History

Issue Date	Changes
Jul-2017	Section 6. “Package and Pinout” Table 6-2 Pin Description: added notes (2) and (3). Table 6-3 Pin Description (SAMA5D23 pins different from those in Table 6-2 “Pin Description”): added note (2). Table 6-4 Pin Description (SAMA5D28B/C pins different from those in Table 6-2 “Pin Description”): added note (2).
	Section 7. “Power Considerations” Updated Figure 7-1 “Recommended Powerup Sequence” and Table 7-2 “Powerup Timing Specification”.
	Section 16. “Standard Boot Strategies” Updated Section 16.4.7.3 “SDCard / e.MMC Boot”. Reworked Section 16.4.7.6 “QSPI NOR Flash Boot for MRL C”.
	Section 29. “Peripheral Touch Controller (PTC)” - Replaced "Peripheral Touch Controller" with "Peripheral Touch Controller Subsystem". - Changed "PTC_IRQ_EVT" to "PTC_IRQ". - Replaced "PIO" and "IO" with "GPIO". Updated: - Figure 29-1. "PTC Block Diagram" - Section 29.2 “Embedded Characteristics” - Section 29.5.2 “I/O Lines” - Section 29.5.3 “Interrupt Sources” - Section 29.6.2.3 “Firmware in SRAM Code Area” Section 29.5.1 “Power Management”: updated description of “SLCK”. Section 29.6.3.1 “PTC Digital Controller Operations”: modified Sensing mode description. Renamed and reworked Section 29.7.1 “PTC Command Register” and Section 29.7.2 “PTC Interrupt Status Register”. Section 29.7.3 “PTC Enable Register”: removed field CLR_IRQEN, and replaced field SET_IRQEN with bits IER0, IER1, IER2, IER3. Renamed the following registers: - “Mode 1: Write Access” to “PTC Command Register” - “Host Flags” to “PTC Interrupt Status Register” - “Host Flags Control” to “PTC Enable Register”
	Section 39. “LCD Controller (LCDC)” Corrected Figure 39-1. Block Diagram (added “PP Layer” block).
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