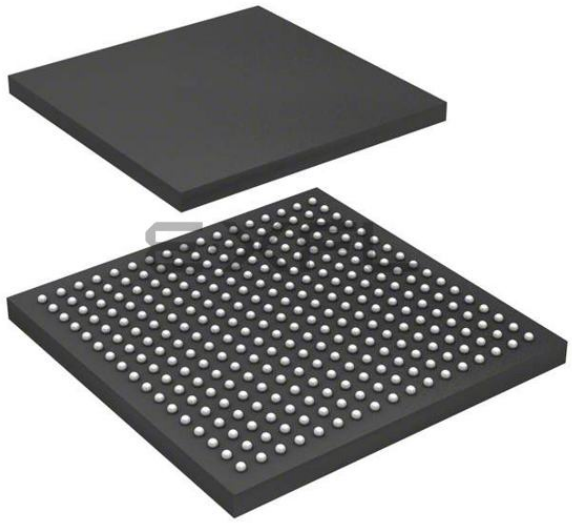


Welcome to E-XFL.COM

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-A5 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 500MHz |
| Co-Processors/DSP | Multimedia; NEON™ MPE |
| RAM Controllers | LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keyboard, LCD, Touchscreen |
| Ethernet | 10/100Mbps (1) |
| SATA | - |
| USB | USB 2.0 + HSIC |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC |
| Package / Case | 289-LFBGA |
| Supplier Device Package | 289-LFBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27a-cur |

## 2. Configuration Summary

**Table 2-1: SAMA5D2 Configuration Summary**

| Feature | SAMA5D21 | SAMA5D22 | SAMA5D23 | SAMA5D24 | SAMA5D26 | SAMA5D27 | SAMA5D28 |
|---|---|---|---|---|---|---|---|
| Package | TFBGA196 | | | TFBGA256 | LFBGA289 | | |
| PIOs | 72 | | | 105 | 128 | | |
| DDR Bus | 16-bit | | | 16/32-bit | | | |
| SMC | Up to 16-bit | | | | | | |
| SRAM | 128 Kbytes | | | | | | |
| QSPI | 2 | | | | | | |
| LCD | 24-bit RGB | | | | | | |
| Camera Interface (ISC) | 1 | | | | | | |
| EMAC | 1 | | | | | | |
| PTC | – | 4 X-lines x 8 Y-lines | | 8 X-lines x 8 Y-lines | – | 8 X-lines x 8 Y-lines | |
| CAN | – | 1 | | – | | 2 | |
| USB | 2 (2 Hosts or 1 Host/1 Device) | | | 3 (2 Hosts/ 1 HSIC, or 1 Host/ 1 Device/ 1 HSIC) | 2 (2 Hosts or 1 Host/ 1 Device) | 3 (2 Hosts/1 HSIC or 1 Host/1 Device/1 HSIC) | |
| UART/SPI/$I^2C$ | 9 / 6 / 6 | | | 10 / 7 / 7 | | | |
| SDIO/SD/MMC | 1 | | | 2 | | | |
| $I^2S$/SSC/ Class D/PDM | 2 / 2 / 1 / 1 | | | | | | |
| ADC Inputs | 5 | | | 12 | | | |
| Timers | 5 | | | 6 | | | |
| PWM | 4 (PWM) + 5 (TC) | | | 4 (PWM) + 6 (TC) | | | |
| Tamper Pins | 6 | | | 2 | 8 | | |
| AESB | – | Yes | | | – | Yes | |
| Environmental Monitors, Die Shield | – | | Yes | – | | | Yes |

For information on device pin compatibility, see Section 6.2 “Pinouts”.

**Table 6-2: Pin Description (Continued)**

| 289-pin BGA | 256-pin BGA | 196-pin BGA | Power Rail | I/O Type | Primary | | Alternate | | PIO peripheral | | | | Reset State (Signal, Dir, PU, PD, HiZ, ST)(1)(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Signal | Dir | Signal | Dir | Func | Signal | Dir | IO Set | |
| G10 | E9 | – | VDDIOP2 | GPIO_CLK | PD0 | I/O | – | – | A | LCDPCK | O | 2 | PIO, I, PU, ST |
| | | | | | | | | | B | FLEXCOM4_IO4 | O | 1 | |
| | | | | | | | | | C | UTXD3 | O | 2 | |
| | | | | | | | | | D | GTSUCOMP | O | 2 | |
| | | | | | | | | | F | A23 | O | 2 | |
| E10 | F8 | – | VDDIOP2 | GPIO | PD1 | I/O | – | – | A | LCDDEN | O | 2 | PIO, I, PU, ST |
| | | | | | | | | | D | GRXCK | I | 2 | |
| | | | | | | | | | F | A24 | O | 2 | |
| G9 | F9 | – | VDDIOP2 | GPIO_CLK | PD2 | I/O | – | – | A | URXD1 | I | 1 | PIO, I, PU, ST |
| | | | | | | | | | D | GTXER | O | 2 | |
| | | | | | | | | | E | ISC_MCK | O | 2 | |
| | | | | | | | | | F | A25 | O | 2 | |
| K1 | J4 | – | VDDANA | GPIO_AD | PD3 | I/O | PTC_X0 | – | A | UTXD1 | O | 1 | PIO, I, PU, ST |
| | | | | | | | | | B | FIQ | I | 2 | |
| | | | | | | | | | D | GCRS | I | 2 | |
| | | | | | | | | | E | ISC_D11 | I | 2 | |
| | | | | | | | | | F | NWAIT | I | 2 | |
| J6 | H6 | – | VDDANA | GPIO_AD | PD4 | I/O | PTC_X1 | – | A | TWD1 | I/O | 2 | PIO, I, PU, ST |
| | | | | | | | | | B | URXD2 | I | 1 | |
| | | | | | | | | | D | GCOL | I | 2 | |
| | | | | | | | | | E | ISC_D10 | I | 2 | |
| | | | | | | | | | F | NCS0 | O | 2 | |
| J4 | H1 | – | VDDANA | GPIO_AD | PD5 | I/O | PTC_X2 | – | A | TWCK1 | I/O | 2 | PIO, I, PU, ST |
| | | | | | | | | | B | UTXD2 | O | 1 | |
| | | | | | | | | | D | GRX2 | I | 2 | |
| | | | | | | | | | E | ISC_D9 | I | 2 | |
| | | | | | | | | | F | NCS1 | O | 2 | |
| J2 | G4 | – | VDDANA | GPIO_AD | PD6 | I/O | PTC_X3 | – | A | TCK | I | 2 | PIO, I, PU, ST |
| | | | | | | | | | B | PCK1 | O | 1 | |
| | | | | | | | | | D | GRX3 | I | 2 | |
| | | | | | | | | | E | ISC_D8 | I | 2 | |
| | | | | | | | | | F | NCS2 | O | 2 | |
| J7 | H5 | F5 | VDDANA | GPIO_AD | PD7 | I/O | PTC_X4 | – | A | TDI | I | 2 | PIO, I, PU, ST |
| | | | | | | | | | C | UTMI_RXVAL | O | 1 | |
| | | | | | | | | | D | GTX2 | O | 2 | |
| | | | | | | | | | E | ISC_D0 | I | 2 | |
| | | | | | | | | | F | NWR1/NBS1 | O | 2 | |

### 18.13.8 Master Error Status Register

**Name:** MATRIX_MESR

**Address:** 0xF001815C (0), 0xFC03C15C (1)

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | MERR11 | MERR10 | MERR9 | MERR8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MERR7 | MERR6 | MERR5 | MERR4 | MERR3 | MERR2 | MERR1 | MERR0 |

**MERRx: Master x Access Error**

0: No Master Access Error has occurred since the last read of the MATRIX_MESR.

1: At least one Master Access Error has occurred since the last read of the MATRIX_MESR.

### 18.13.9 Master Error Address Registers

**Name:** MATRIX_MEARx [x=0..11]

**Address:** 0xF0018160 (0), 0xFC03C160 (1)

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| ERRADD | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| ERRADD | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ERRADD | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ERRADD | | | | | | | |

**ERRADD: Master Error Address**

Master Last Access Error Address

### 26.6.18 RTC TimeStamp Time Register 1

**Name:** RTC_TSTR1

**Address:** 0xF804816C

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| BACKUP | – | – | – | – | – | – | – |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| – | AMPM | HOUR | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| – | MIN | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | SEC | | | | | | |

These fields are valid for non-UTC mode only.

RTC_TSTR1 reports the timestamp of the last tamper event.

This register is cleared by reading RTC_TSSR1.

**SEC: Seconds of the Tamper**

**MIN: Minutes of the Tamper**

**HOUR: Hours of the Tamper**

**AMPM: AM/PM Indicator of the Tamper**

**BACKUP: System Mode of the Tamper**

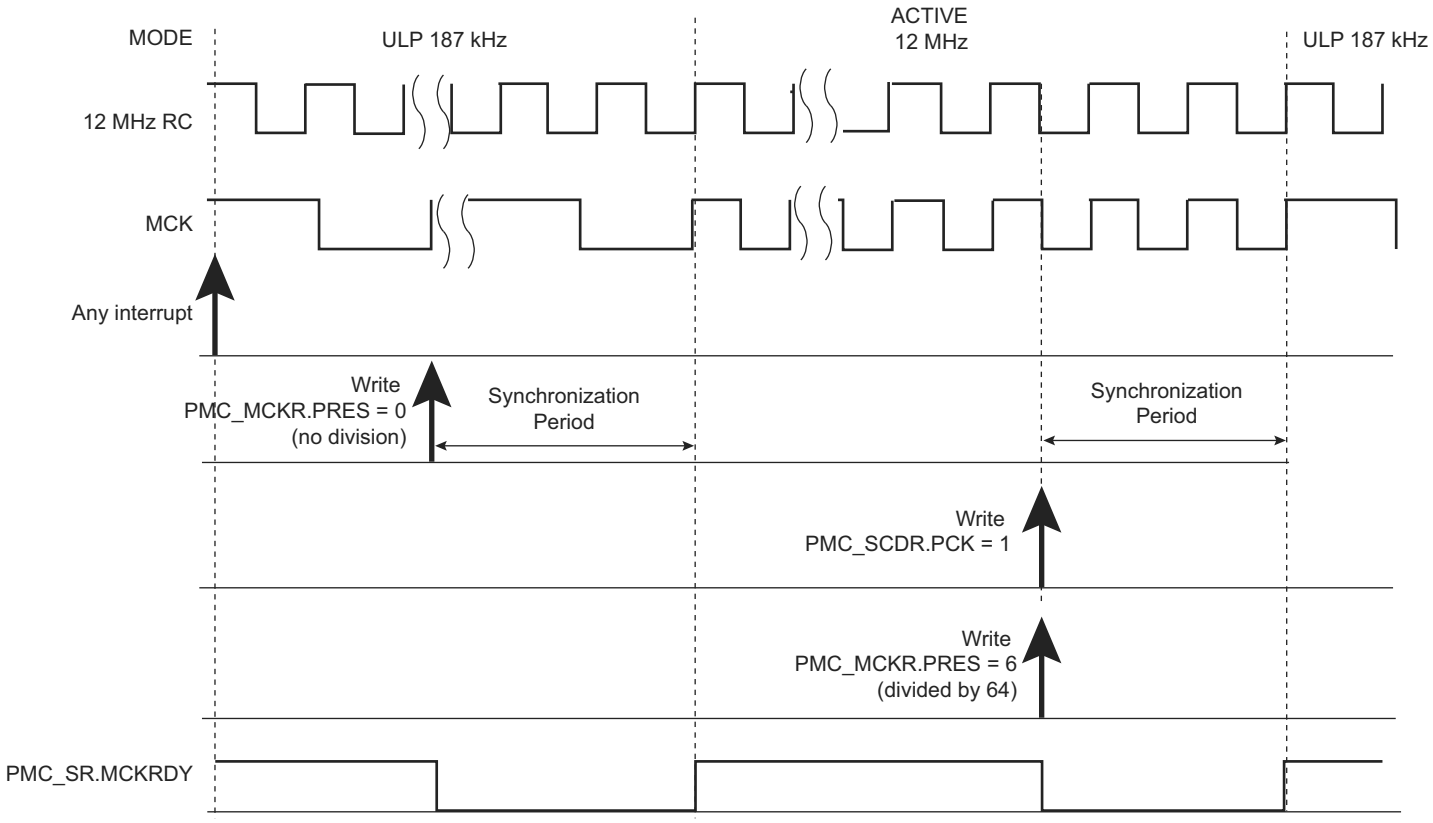
0: The state of the system is different from Backup mode when the tamper event occurs.

1: The system is in Backup mode when the tamper event occurs.

### 33.14 Fast Startup from Ultra Low-power (ULP) Mode 0

In Ultra Low-power (ULP) mode 0, the Main clock (MAINCK) must be running, thus either the 12 MHz crystal oscillator or the Fast RC oscillator must be enabled. The lowest power consumption that can be achieved in ULP Mode 0, can be obtained when dividing the selected oscillator frequency by 64 by writing PMC_MCKR.PRES to 6. Any interrupt exits the system from ULP Mode. The software must write PMC_MCKR.PRES to 1 to provide MCK with the fastest clock. If the PLL is used, the startup procedure must be done prior to writing PMC_MCKR.PRES to 1. Figure 33-5 illustrates an example of startup phase from ULP Mode 0 without use of PLL.

**Figure 33-5: Fast Startup from Ultra Low-Power Mode 0**




**Warning:** The duration of the WKUPx pins active level must be greater than four MAINCK cycles.

### 34.7.28 Secure PIO I/O Security Status Register

**Name:** S_PIO_IOSSRx [x=0..3]

**Address:** 0xFC039038 [0], 0xFC039078 [1], 0xFC0390B8 [2], 0xFC0390F8 [3]

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

**P0–P31: I/O Security Status**

0 (SECURE): The I/O line of the I/O group x is in Secure mode.

1 (NON_SECURE): The I/O line of the I/O group x is in Non-Secure mode.

**CLUTMODE: Color Lookup Table Mode Input Selection**

| Value | Name | Description |
|---|---|---|
| 0 | CLUT_1BPP | Color Lookup Table mode set to 1 bit per pixel |
| 1 | CLUT_2BPP | Color Lookup Table mode set to 2 bits per pixel |
| 2 | CLUT_4BPP | Color Lookup Table mode set to 4 bits per pixel |
| 3 | CLUT_8BPP | Color Lookup Table mode set to 8 bits per pixel |

### 39.7.51 Overlay 1 Configuration Register 6

**Name:** LCDC_OVR1CFG6

**Address:** 0xF0000184

**Access:** Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RDEF | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| GDEF | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BDEF | | | | | | | |

**RDEF: Red Default**

Default Red color when the Overlay 1 DMA channel is disabled.

**GDEF: Green Default**

Default Green color when the Overlay 1 DMA channel is disabled.

**BDEF: Blue Default**

Default Blue color when the Overlay 1 DMA channel is disabled.

### 39.7.110 High-End Overlay Configuration Register 15

**Name:** LCDC_HEOCFG15

**Address:** 0xF00003C8

**Access:** Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | CSCUOFF | CSCGV | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| CSCGV | | | | CSCGU | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CSCGU | | | | | | CSCGY | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CSCGY | | | | | | | |

**CSCGY: Color Space Conversion Y coefficient for Green Component 1:2:7 format**

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

**CSCGU: Color Space Conversion U coefficient for Green Component 1:2:7 format**

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

**CSCGV: Color Space Conversion V coefficient for Green Component 1:2:7 format**

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

**CSCUOFF: Color Space Conversion Offset**

0: Offset is set to 0

1: Offset is set to 128

### 40.8.98 GMAC PTP Event Frame Transmitted Seconds Low Register

**Name:** GMAC_EFTSL

**Address:** 0xF80081E0

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| RUD | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RUD | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RUD | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RUD | | | | | | | |

**RUD: Register Update**

The register is updated with the value that the 1588 Timer Seconds Register holds when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.

### 40.8.111 GMAC Transmit Buffer Queue Base Address Register Priority Queue x

**Name:** GMAC_TBQBAPQx[x=1..2]

**Address:** 0xF8008440

**Access:** Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| TXBQBA | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| TXBQBA | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TXBQBA | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TXBQBA | | | | | | – | – |

These registers hold the start address of the transmit buffer queues (transmit buffers descriptor lists) for the additional queues and must be initialized to the address of valid descriptors, even if the priority queues are not used.

**TXBQBA: Transmit Buffer Queue Base Address**

Written with the address of the start of the transmit queue.

### 40.8.121 GMAC Interrupt Mask Register Priority Queue x

**Name:** GMAC_IMRPQx[x=1..2]

**Address:** 0xF8008640

**Access:** Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| – | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| – | | | | HRESP | ROVR | – | – |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TCOMP | AHB | RLEX | – | – | RXUBR | RCOMP | – |

A read of this register returns the value of the receive complete interrupt mask.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

The following values are valid for all listed bit names of this register:

0: Corresponding interrupt is enabled.

1: Corresponding interrupt is disabled.

**RCOMP: Receive Complete**

**RXUBR: RX Used Bit Read**

**RLEX: Retry Limit Exceeded or Late Collision**

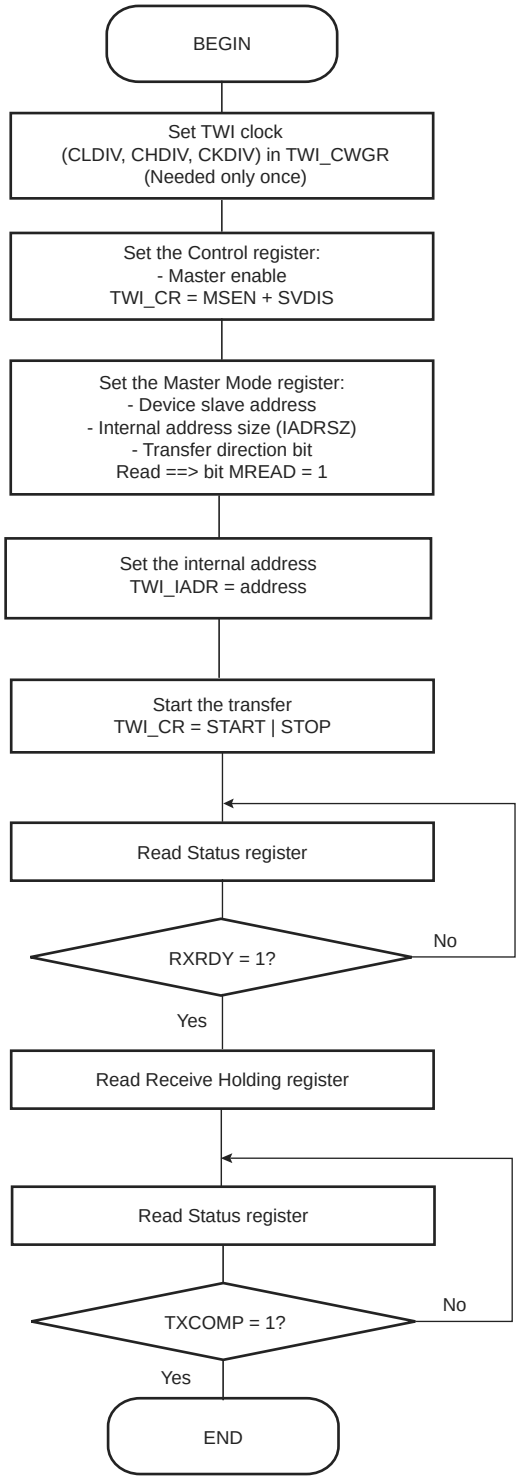
**AHB: AHB Error**

**TCOMP: Transmit Complete**

**ROVR: Receive Overrun**

**HRESP: HRESP Not OK**

**Figure 46-22: TWIHS Read Operation with Single Data Byte and Internal Address**



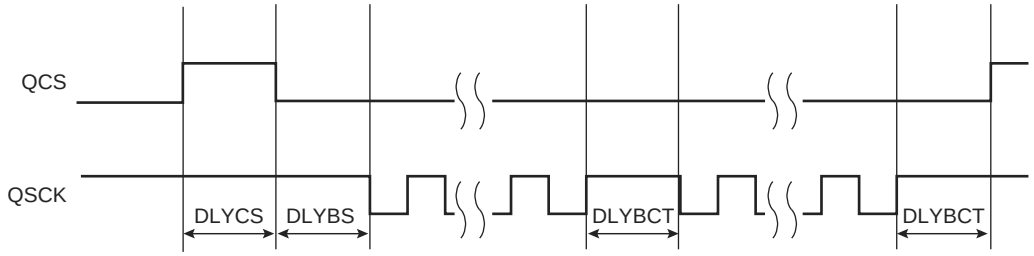
### 50.6.3 Transfer Delays

Figure 50-4 shows several consecutive transfers while the chip select is active. Three delays can be programmed to modify the transfer waveforms:

- The delay between the deactivation and the activation of QCS, programmed by writing QSPI_MR.DLYCS. Allows to adjust the minimum time of QCS at high level.
- The delay before QSCK, programmed by writing QSPI_SR.DLYBS. Allows the start of QSCK to be delayed after the chip select has been asserted.
- The delay between consecutive transfers, programmed by writing QSPI_MR.DLYBCT. Allows insertion of a delay between two consecutive transfers. In Serial Memory mode, this delay is not programmable and DLYBCT is ignored. In this mode, DLYBCT must be written to ‘0’.

These delays allow the QSPI to be adapted to the interfaced peripherals and their speed and bus release time.

**Figure 50-4: Programmable Delays**




### 50.6.4 QSPI SPI Mode

In SPI mode, the QSPI acts as a standard SPI Master.

To activate this mode, QSPI_MR.SMM must be written to ‘0’ in QSPI_MR.

#### 50.6.4.1 SPI Mode Operations

The QSPI in standard SPI mode operates on the clock generated by the internal programmable baud rate generator. It fully controls the data transfers to and from the slave connected to the SPI bus. The QSPI drives the chip select line to the slave (QCS) and the serial clock signal (QSCK).

The QSPI features two holding registers, the Transmit Data register (QSPI_TDR) and the Receive Data register (QSPI_RDR), and a single internal shift register. The holding registers maintain the data flow at a constant rate.

After enabling the QSPI, a data transfer begins when the processor writes to the QSPI_TDR. The written data is immediately transferred to the internal shift register and transfer on the SPI bus starts. While the data in the internal shift register is shifted on the MOSI line, the MISO line is sampled and shifted to the internal shift register. Receiving data cannot occur without transmitting data. If receiving mode is not needed, for example when communicating with a slave receiver only (such as an LCD), the receive status flags in the Status register (QSPI_SR) can be discarded.

If new data is written in QSPI_TDR during the transfer, it is retained there until the current transfer is completed. Then, the received data is transferred from the internal shift register to the QSPI_RDR, the data in QSPI_TDR is loaded in the internal shift register and a new transfer starts.

The transfer of a data written in QSPI_TDR in the internal shift register is indicated by the Transmit Data Register Empty (TDRE) bit in the QSPI_SR. When new data is written in QSPI_TDR, this bit is cleared. QSPI_SR.TDRE is used to trigger the Transmit DMA channel.

The end of transfer is indicated by the TXEMPTY flag in the QSPI_SR. If a transfer delay (DLYBCT) is greater than 0 for the last transfer, QSPI_SR.TXEMPTY is set after the completion of this delay. The peripheral clock can be switched off at this time.

The transfer of received data from the internal shift register in QSPI_RDR is indicated by the Receive Data Register Full (RDRF) bit in the QSPI_SR. When the received data is read, QSPI_SR.RDRF bit is cleared.

If the QSPI_RDR has not been read before new data is received, the Overrun Error Status (OVRES) bit in QSPI_SR is set. As long as this flag is set, data is loaded in QSPI_RDR. The user must read the QSPI_SR to clear the OVRES bit.

Figure 50-5 shows a block diagram of the SPI when operating in Master mode. Figure 50-6 shows a flow chart describing how transfers are handled.

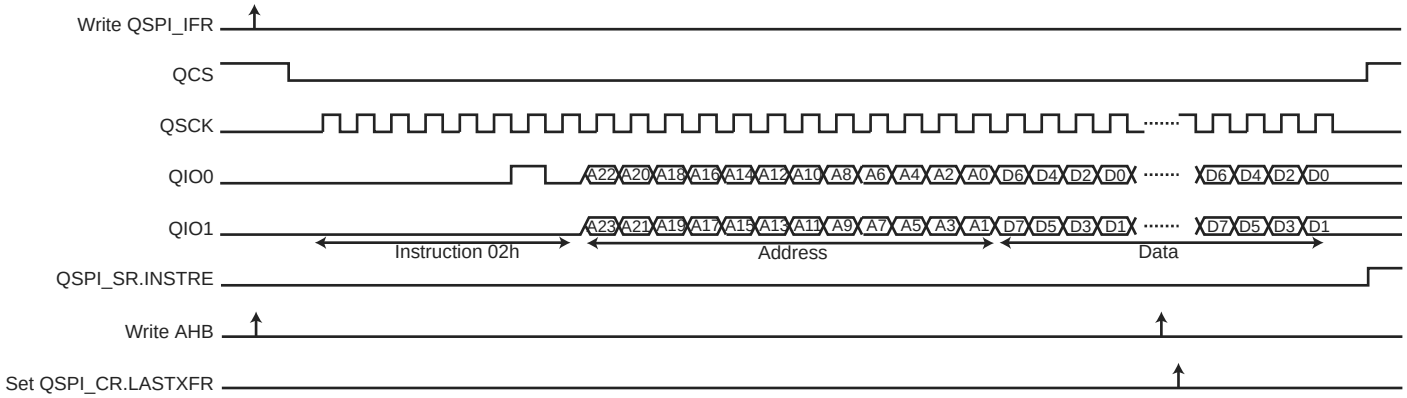
Example 5:

Instruction in Single-bit SPI, with address in Dual SPI, without option, with data write in Dual SPI.

Command: BYTE/PAGE PROGRAM (02h)

- Write 0x0000_0002 in QSPI_ICR.
- Write 0x0000_30B3 in QSPI_IFR.
- Read QSPI_IFR (dummy read) to synchronize system bus accesses.
- Write data in the QSPI system bus memory space (0x9000_00000-0x9800_00000/0XD000_0000--0XD800_0000).
  The address of the first system bus write access is sent in the instruction frame.
  The address of the next system bus write accesses is not used.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

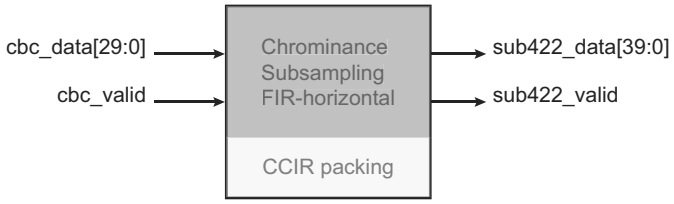
**Figure 50-15: Instruction Transmission Waveform 5**



### 52.5.12 4:4:4 To 4:2:2 Chrominance Horizontal Subsampler (SUB422) Module

The color space conversion output stream is a full-bandwidth YCbCr 4:4:4 signal. The chrominance subsampling divides the horizontal chrominance sampling rate by two. A horizontal low pass filter is applied to avoid aliasing effect. The SUB422 module samples 444 full scale YCbCr cbc_data[29:0] 30-bit data, performs horizontal subsampling and generates the sub422_data[39:0] 40-bit data bus with its validity signal sub422_valid.

**Figure 52-27: SUB422 Block Diagram**



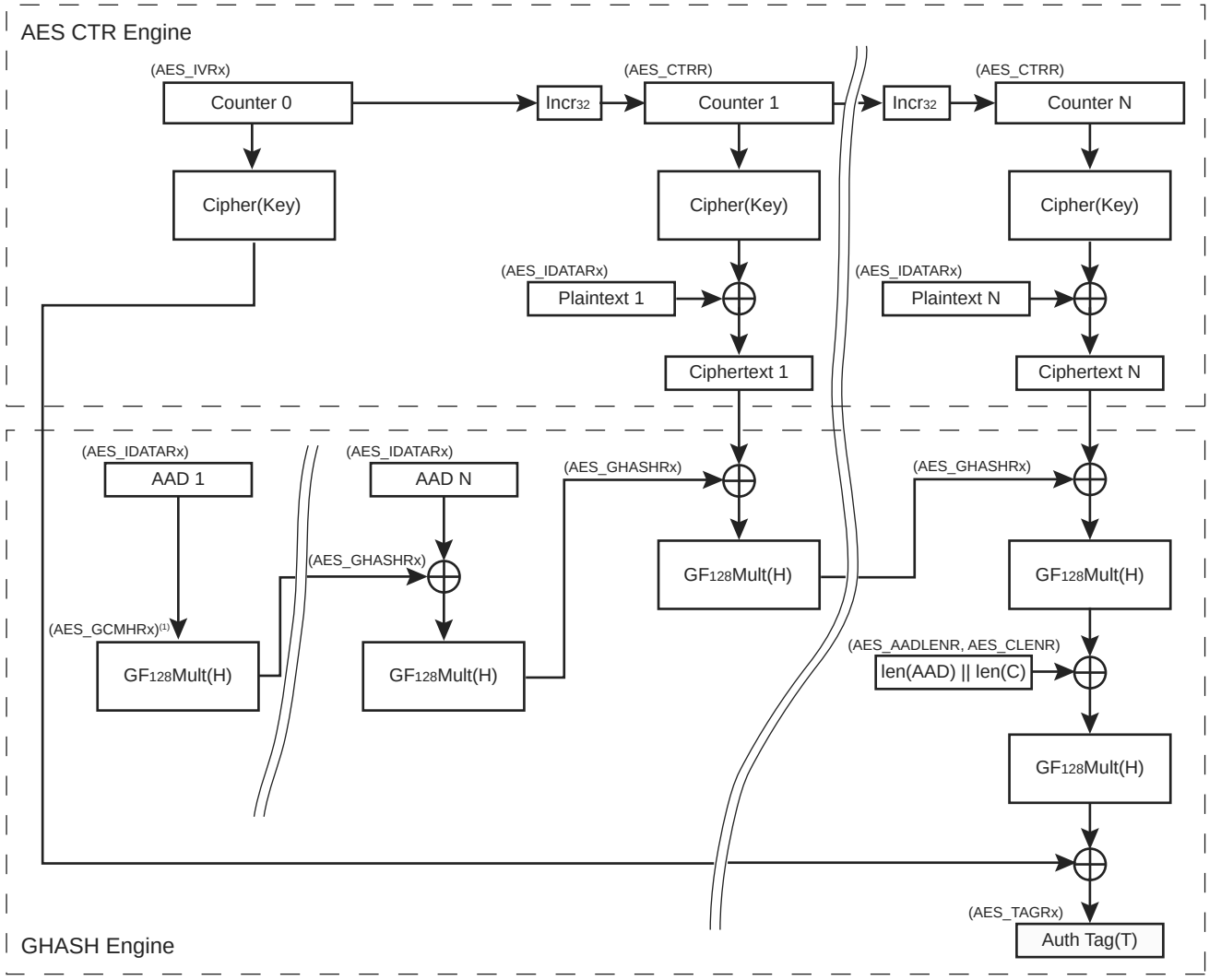

| ISC_SUB422_CTRL.ENABLE | ISC_SUB422_CFG.CCIR | SUB422_DATA Slice | Value |
|---|---|---|---|
| 0 | 0 | sub422_data[29:0] | cbc_data[29:0] |
| 1 | 0 | sub422_data[39:30] | Y1= cbc_data1[29:20] |
| | | sub422_data[29:20] | Y0 = cbc_data0[29:20] |
| | | sub422_data[19:10] | Cb = filter_hor(cbc_data[19:10]) |
| | | sub422_data[9:0] | Cr = filter_hor(cbc_data[9:0]) |
| 1 | 1 | sub422_data[39:30] | Y1 = cbc_data[9:0] |
| | | sub422_data[29:20] | Y0 = cbc_data[9:0] |
| | | sub422_data[19:10] | Cb = cbc_data[9:0] |
| | | sub422_data[9:0] | Cr = cbc_data[9:0] |

The filter_hor function included in the sub422 module is the chrominance horizontal filter.

| sub422 data slice | YCbCr mapping |
|---|---|
| sub422_data[39:30] | Y1 (sample *n*) |
| sub422_data[29:20] | Y0 (sample *n-1*) |
| sub422_data[19:10] | Cb (from filter) |
| sub422_data[9:0] | Cr (from filter) |

The filter chrominance position is selectable through the use of the ISC_SUB422_CFG.FILTER field.

**Figure 60-5: GCM Block Diagram**




Note: 1. Optional

### 60.4.6.2 Key Writing and Automatic Hash Subkey Calculation

Whenever a new key is written to the hardware, two automatic actions are processed:

- GCM Hash Subkey *H* generation—The GCM hash subkey (*H*) is automatically generated. The GCM hash subkey generation must be complete before doing any other action. AES_ISR.DATRDY indicates when the subkey generation is complete (with interrupt if configured). The GCM hash subkey calculation is processed with the formula *H* = CIPHER(Key, <128 bits to zero>). The generated GCM *H* value is then available in AES_GCMHRx. If the application software requires a specific hash subkey, the automatically generated H value can be overwritten in AES_GCMHRx.
  AES_GCMHRx can be written after the end of the hash subkey generation (see AES_ISR.DATRDY) and prior to starting the input data feed.
- AES_GHASHRx Clear—AES_GHASHRx are automatically cleared. If a hash initial value is needed for the GHASH, it must be written to AES_GHASHRx
  - after a write to the AES Key Register, if any
  - before starting the input data feed

### 60.4.6.3 GCM Processing

GCM processing is made up of three phases:

1. Processing the Additional Authenticated Data (*AAD*), hash computation only.
2. Processing the Ciphertext (*C*), hash computation + ciphering/deciphering.

When TSMODE = 1 or 3, each trigger event adds two half-words in the buffer (assuming TSAV = 0), first half-word being XPOS of ADC_XPOSR then YPOS of ADC_YPOSR. If TSAV/TSFREQ ≠ 0, the data structure remains unchanged. Not all trigger events add data to the buffer.

When TSMODE = 2, each trigger event adds four half-words to the buffer (assuming TSAV = 0), first half-word being XPOS of ADC_XPOSR followed by YPOS of ADC_YPOSR and finally Z1 followed by Z2, both located in ADC_PRESSR.

When TAG is set (ADC_EMR), the CHNB field (four most significant bits of ADC_LCDR) is cleared when XPOS is transmitted and set when YPOS is transmitted, allowing an easier post-processing of the buffer or a better checking of the buffer integrity. In case 4-wire with Pressure mode is selected, Z1 value is transmitted to the buffer along with tag set to 2 and Z2 is tagged with value 3.

XSCALE and YSCALE (calibration values) are not transmitted to the buffer because they are supposed to be constant and moreover only measured at the very first startup of the controller or upon user request.

There is no change in buffer structure whatever the value of PENDET bit configuration in ADC_TSMR but it is recommended to use the pen detection function for buffer post-processing (see Section 65.6.17.4 “Pen Detection Status”).

**Table 72-5: SAMA5D2 Datasheet Rev. 11267C Revision History (Continued)**

| Issue Date | Changes |
|---|---|
| 8-Jan-16 | Section 41. “Inter-IC Sound Controller (I2SC)” |
| | Section 41.6.3 “Master, Controller and Slave Modes”: removed text fragment: ‘in order to avoid unwanted glitches on the I2SWS and I2SCK pins.’ |
| | Section 41.8.2 “Inter-IC Sound Controller Mode Register”: removed text fragment: ‘in order to avoid unexpected behavior on the I2SWS, I2SCK and I2SDO outputs.’ and added note (2) below IMCKDIV field description. |
| | Section 44. “Flexible Serial Communication Controller (FLEXCOM)” |
| | Restored all references to ISO7816 specification |
| | Updated Figure 44-3 “Fractional Baud Rate Generator” |
| | Added Figure 44-27 “RTS line software control when FLEX_US_MR.USART_MODE = 2” |
| | Section 44.10.6 “USART Mode Register”: updated USART_MODE field description (SPI_MASTER item) |
| | Section 44.10.44 “SPI Mode Register”: added LBHPC bit |
| | Section 55. “Universal Asynchronous Receiver Transmitter (UART)” |
| | Section 55.6.9 “UART Baud Rate Generator Register”: in CD field description, corrected equation after “If BRSRCCK = 1” |
| | Section 59. “Quad SPI Interface (QSPI)” |
| | Section 59.7.5 “QSPI Status Register”: updated RDRF, TDRE, TXEMPTY, and OVRES field descriptions |
| | Section 48. “Secure Digital Multimedia Card Controller (SDMMC)” |
| | Section 48.12.41 “SDMMC Preset Value Register”: updated CLKGSEL field description |
| | Section 49. “Image Sensor Controller (ISC)” |
| | Section 49.1 “Description”: removed "serial csi-2 based CMOS/CCD sensor" (not supported). |
| | Section 50. “Controller Area Network (MCAN)” |
| | Changed MCAN interrupt line names to MCAN_INT0 and MCAN_INT1 thoughout the section |
| | Section 50.6.7 “MCAN CC Control Register”: added bit NISO |
| | Section 51. “Timer Counter (TC)” |
| | Reformatted and renamed Table 51-2 “Channel Signal Description” |
| | Section 51.6.3 “Clock Selection”: updated notes (1) and (2) |
| | Section 52. “Pulse Density Modulation Interface Controller (PDMIC)” |
| | Replaced all instances of “PCK” with “GCLK” |
| | Section 52.2 “Embedded Characteristics”: removed ‘Multiplexed PDM Input Support’ characteristic |
| | Updated Section 52.5.2 “Power Management” and Section 52.6.2.1 “Description” |
| | Section 52.6.2.6 “Gain and Offset Compensation”: updated *dgain* bullet |
| | Section 52.7.3 “PDMIC Converted Data Register”: updated DATA field description |
| | Section 52.7.8 “PDMIC DSP Configuration Register 0”: updated OSR field description |
| | Section 61. “Security Module” |
| | Section 61.5.5 “SECUMOD Status Clear Register”: removed MCKM field description |
| | Section 61.5.18 “SECUMOD Wake Up Register”: removed TPML field description |
| | Section 77. “Analog-to-Digital Converter (ADC)” |
| | Section 77.7.2 “ADC Mode Register”: updated TRACKTIM and TRANSFER field descriptions. |