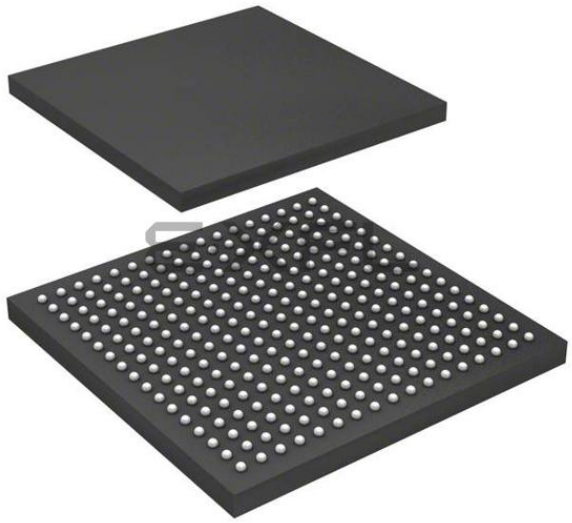

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Understanding Embedded - Microprocessors

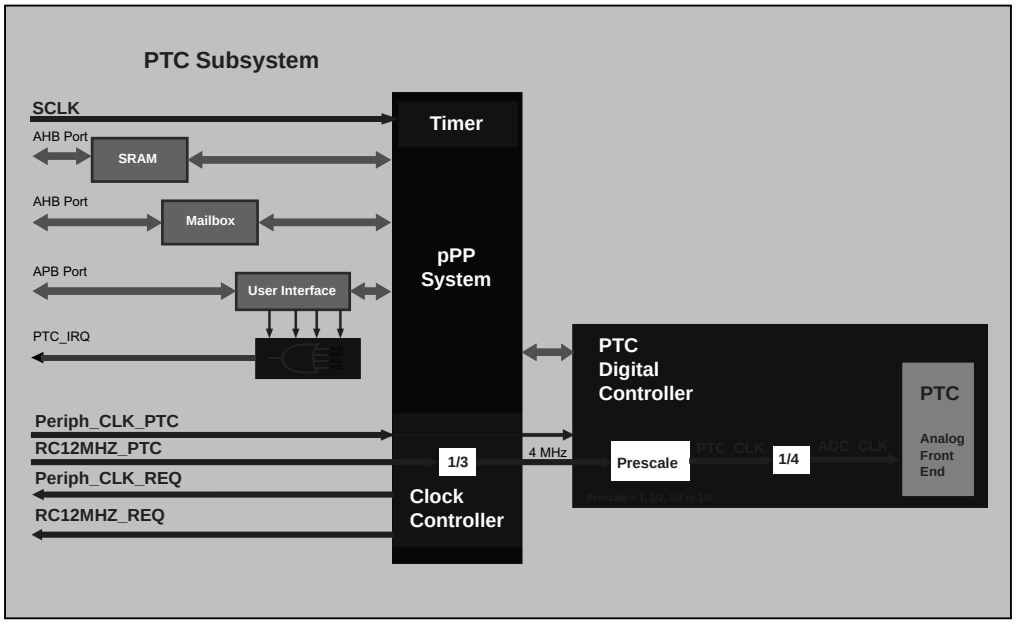
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27b-cnr

Figure 29-3: PTC Subsystem Clock Schematic



The RC12HMZ clock is internally divided by 3 in the PTC subsystem, and so a 4 MHz clock is provided to the PTC digital controller. This controller can divide the clock further by 1, 2, 4 or 8 to slow down the PTC clock.

- ADC_CLK

The prescaled clock PTC_CLK is divided by 4 to supply an ADC_CLK to the PTC analog front end.

The ADC data rate is defined by the controller. The typical value is about 33 kHz to 66 kHz depending on the timing configuration.

29.5.2 I/O Lines

The pins used for interfacing the PTC may be multiplexed with GPIO lines. When the PTC subsystem is activated and the X-Y lines selected, the GPIO switches automatically to analog state. The ADC modules possibly hanging on the same PTC analog lines should not use the same GPIO for ADC conversion. Adjacent GPIO lines to PTC lines must not be used to output high speed signals to avoid crosstalk with PTC sensing.

When a line is disabled, the corresponding I/O pin is not reserved for the PTC subsystem, and it can be used for some alternative I/O function.

There is an individual selection bit for each Y or X line. In normal cases, just one line should be active at the same time. For more advanced uses, like proximity sensing, several lines may be selected in parallel. The input and output functionality, such as charging and sensing pulses of the selected line, is controlled automatically by the PTC digital controller sequencer in various operating modes. The I/O lines used for analog PTC_X lines and PTC_Y lines must be connected to external capacitive touch sensor electrodes. External components are not required for normal operation.

29.5.3 Interrupt Sources

The PTC_IRQ interrupt line is connected on one of the internal sources of the host processor interrupt controller (AIC). Using the PTC_IRQ interrupt requires the interrupt controller to be programmed first.

Four interrupts (IRQ0,1,2,3) can be generated in the host interface register. The PTC_IRQ line is a logical “OR” between the four IRQ0, IRQ1, IRQ2 and IRQ3.

29.6 Functional Description

The PTC analog front end (AFE) and the digital controller are not managed directly by the Cortex-A5 processor. An intermediate processor (pPP) is introduced to manage all functionalities of the PTC. A pPP program, a “firmware”, is needed. This program is loaded by the ARM (host) in a shared SRAM area. The firmware embeds many software functionalities and algorithms to ensure an efficient touch detection.

33.22.24 PMC Peripheral Clock Enable Register 1

Name: PMC_PCER1

Address: 0xF0014100

Access: Write-only

31	30	29	28	27	26	25	24
PID63	PID62	PID61	PID60	PID59	PID58	PID57	PID56
23	22	21	20	19	18	17	16
PID55	PID54	PID53	PID52	PID51	PID50	PID49	PID48
15	14	13	12	11	10	9	8
PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
7	6	5	4	3	2	1	0
PID39	PID38	PID37	PID36	PID35	PID34	PID33	PID32

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

PIDx: Peripheral Clock x Enable

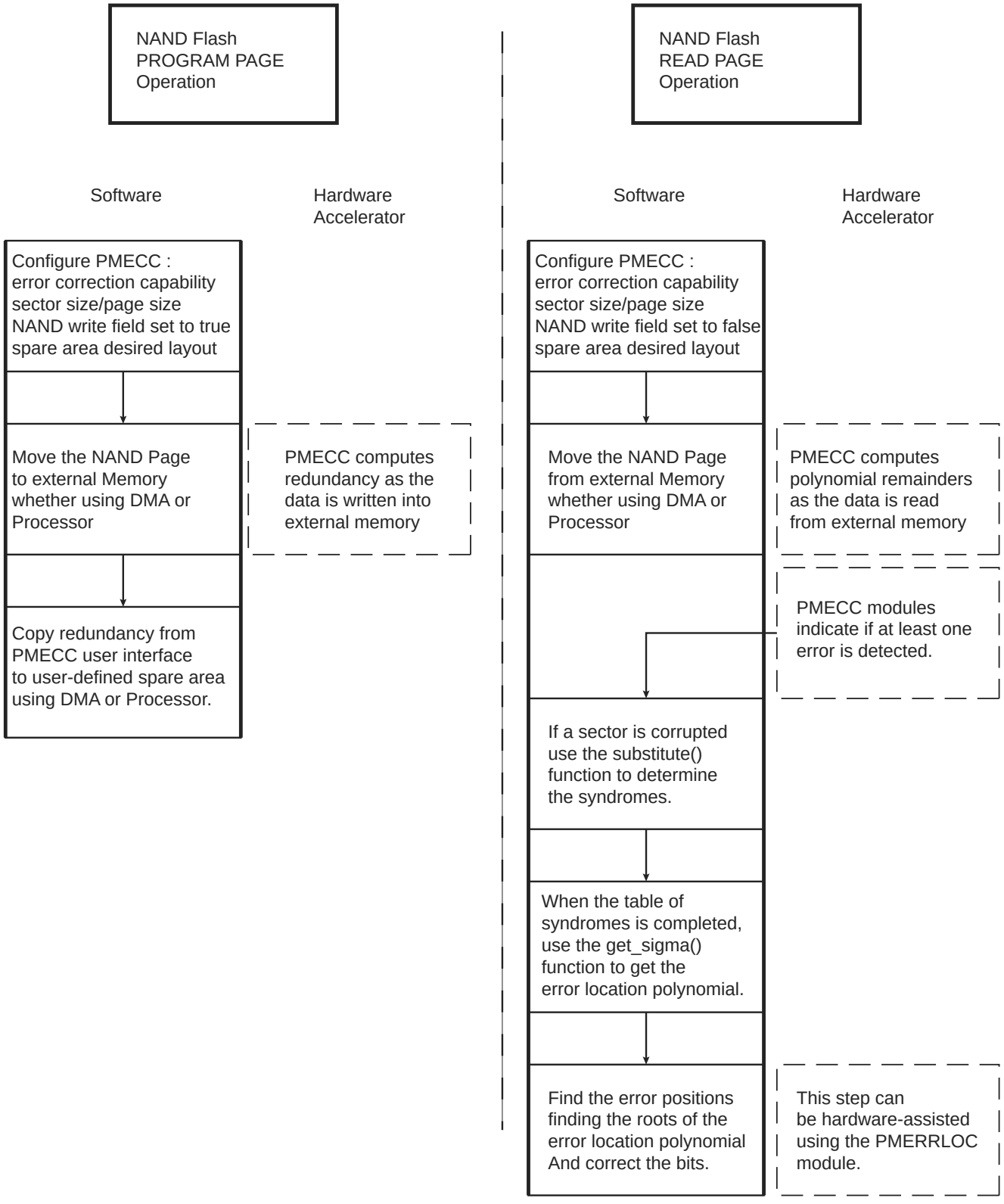
0: No effect.

1: Enables the corresponding peripheral clock.

Note 1: PID32 to PID63 refer to identifiers as defined in Section 11.2 “Peripheral Identifiers”.

2: Programming the control bits of the Peripheral ID that are not implemented has no effect on the behavior of the PMC.

Figure 37-39: Software Hardware Multibit Error Correction Dataflow



38.9.23 XDMAC Channel x [x = 0..15] Destination Address Register

Name: XDMAC_CDAx [x = 0..15]

Address: 0xF0004064 (1)[0], 0xF00040A4 (1)[1], 0xF00040E4 (1)[2], 0xF0004124 (1)[3], 0xF0004164 (1)[4], 0xF00041A4 (1)[5], 0xF00041E4 (1)[6], 0xF0004224 (1)[7], 0xF0004264 (1)[8], 0xF00042A4 (1)[9], 0xF00042E4 (1)[10], 0xF0004324 (1)[11], 0xF0004364 (1)[12], 0xF00043A4 (1)[13], 0xF00043E4 (1)[14], 0xF0004424 (1)[15], 0xF0010064 (0)[0], 0xF00100A4 (0)[1], 0xF00100E4 (0)[2], 0xF0010124 (0)[3], 0xF0010164 (0)[4], 0xF00101A4 (0)[5], 0xF00101E4 (0)[6], 0xF0010224 (0)[7], 0xF0010264 (0)[8], 0xF00102A4 (0)[9], 0xF00102E4 (0)[10], 0xF0010324 (0)[11], 0xF0010364 (0)[12], 0xF00103A4 (0)[13], 0xF00103E4 (0)[14], 0xF0010424 (0)[15]

Access: Read/Write

31	30	29	28	27	26	25	24
DA							

23	22	21	20	19	18	17	16
DA							

15	14	13	12	11	10	9	8
DA							

7	6	5	4	3	2	1	0
DA							

DA: Channel x Destination Address

Program this register with the destination address of the DMA transfer.

A configuration error is generated when this address is not aligned with the transfer data size.

39.7.18 Base Layer Channel Status Register

Name: LCDC_BASECHSR

Address: 0xF0000048

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	A2QSR	UPDATESR	CHSR

CHSR: Channel Status

0: Layer disabled

1: Layer enabled

UPDATESR: Update Overlay Attributes In Progress Status

0: No update pending

1: Overlay attributes will be updated on the next frame

A2QSR: Add To Queue Status

0: Add to queue not pending

1: Add to queue pending

39.7.123 High-End Overlay Configuration Register 28

Name: LCDC_HEOCFG28

Address: 0xF00003FC

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
XPHI5COEFF4							

XPHI5COEFF4: Horizontal Coefficient for phase 5 tap 4

Coefficient format is 1 sign bit and 7 fractional bits.

39.7.149 Post Processing Configuration Register 1

Name: LCDC_PPCFG1

Address: 0xF0000570

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	ITUBT601	–	PPMODE		

PPMODE: Post Processing Output Format Selection

Value	Name	Description
0	PPMODE_RGB_16BPP	RGB 16 bpp
1	PPMODE_RGB_24BPP_PACKED	RGB 24 bpp PACKED
2	PPMODE_RGB_24BPP_UNPACKED	RGB 24 bpp UNPACKED
3	PPMODE_YCBCR_422_MODE0	YCbCr 422 16 bpp (Mode 0)
4	PPMODE_YCBCR_422_MODE1	YCbCr 422 16 bpp (Mode 1)
5	PPMODE_YCBCR_422_MODE2	YCbCr 422 16 bpp (Mode 2)
6	PPMODE_YCBCR_422_MODE3	YCbCr 422 16 bpp (Mode 3)

ITUBT601: Color Space Conversion Luminance

0: Luminance and chrominance range is [0;255]

1: Luminance values are clamped to [16;235] range. Chrominance values are clamped to [16;240] range.

45.9.13 SSC Status Register

Name: SSC_SR

Address: 0xF8004040 (0), 0xFC004040 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	RXEN	TXEN
15	14	13	12	11	10	9	8
–	–	–	–	RXSYN	TXSYN	CP1	CP0
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	–	TXEMPTY	TXRDY

TXRDY: Transmit Ready

0: Data has been loaded in SSC_THR and is waiting to be loaded in the transmit shift register (TSR).

1: SSC_THR is empty.

TXEMPTY: Transmit Empty

0: Data remains in SSC_THR or is currently transmitted from TSR.

1: Last data written in SSC_THR has been loaded in TSR and last data loaded in TSR has been transmitted.

RXRDY: Receive Ready

0: SSC_RHR is empty.

1: Data has been received and loaded in SSC_RHR.

OVRUN: Receive Overrun

0: No data has been loaded in SSC_RHR while previous data has not been read since the last read of the Status Register.

1: Data has been loaded in SSC_RHR while previous data has not yet been read since the last read of the Status Register.

CP0: Compare 0

0: A compare 0 has not occurred since the last read of the Status Register.

1: A compare 0 has occurred since the last read of the Status Register.

CP1: Compare 1

0: A compare 1 has not occurred since the last read of the Status Register.

1: A compare 1 has occurred since the last read of the Status Register.

TXSYN: Transmit Sync

0: A Tx Sync has not occurred since the last read of the Status Register.

1: A Tx Sync has occurred since the last read of the Status Register.

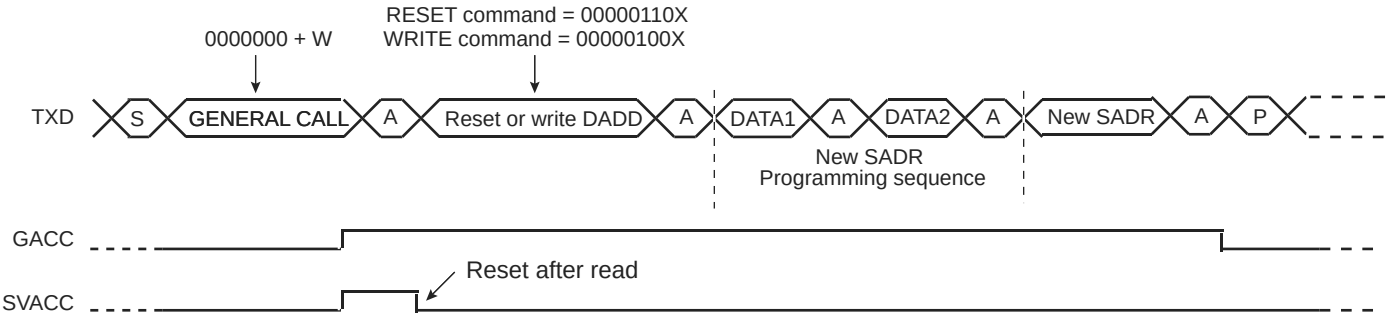
If a GENERAL CALL is detected, GACC is set.

After the detection of general call, decode the commands that follow.

In case of a WRITE command, decode the programming sequence and program a new SADR if the programming sequence matches.

Figure 46-38 describes the general call access.

Figure 46-38: Master Performs a General Call



Note: This method enables the user to create a personal programming sequence by choosing the programming bytes and their number. The programming sequence has to be provided to the master.

- Clock Stretching

In both Read and Write modes, it may occur that TWIHS_THR/TWIHS_RHR buffer is not filled/emptied before the transmission/reception of a new character. In this case, to avoid sending/receiving undesired data, a clock stretching mechanism is implemented.

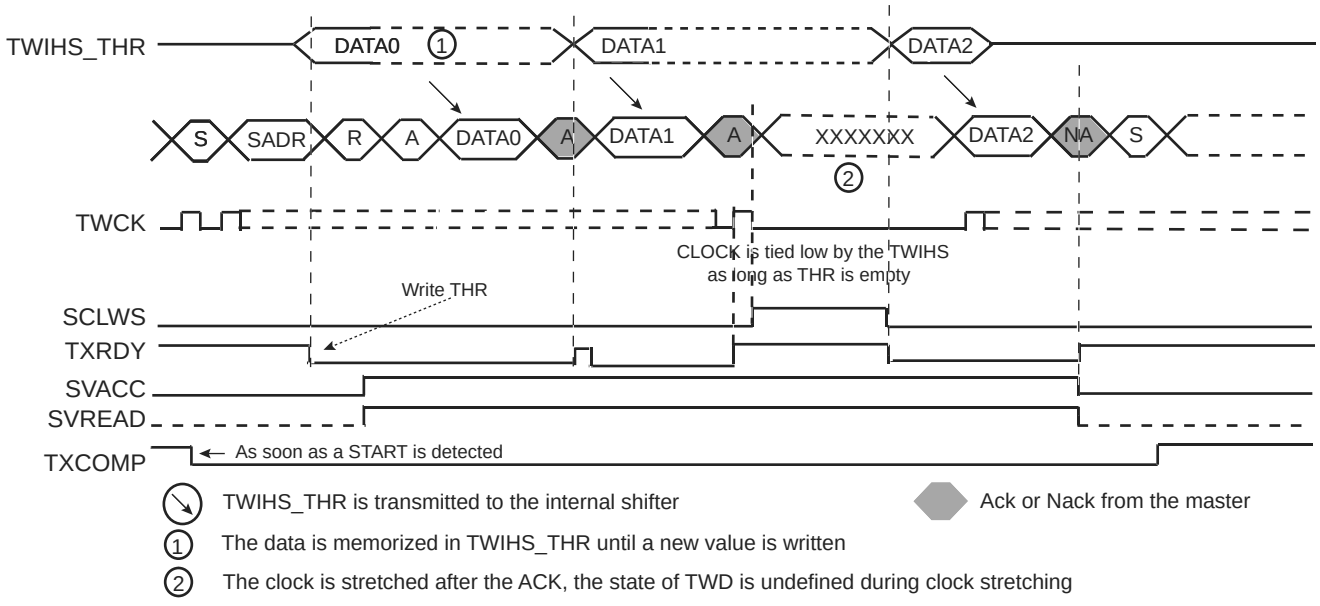
Note: Clock stretching can be disabled by setting the SCLWSDIS bit in the TWIHS_SMR. In that case the UNRE and OVRE flags indicate an underrun (when TWIHS_THR is not filled on time) or an overrun (when TWIHS_RHR is not read on time).

Clock Stretching in Read Mode

The clock is tied low if the internal shifter is empty and if a STOP or REPEATED START condition was not detected. It is tied low until the internal shifter is loaded.

Figure 46-39 describes the clock stretching in Read mode.

Figure 46-39: Clock Stretching in Read Mode



Note 1: TXRDY is reset when data has been written in the TWIHS_THR to the internal shifter and set when this data has been acknowledged or non acknowledged.

47.10.26 USART Transmitter Timeguard Register

Name: FLEX_US_TTGR

Address: 0xF8034228 (0), 0xF8038228 (1), 0xFC010228 (2), 0xFC014228 (3), 0xFC018228 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TG							

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

TG: Timeguard Value

0: The transmitter timeguard is disabled.

1–255: The transmitter timeguard is enabled and TG is timeguard delay / bit period.

48.6.7 UART Receiver Holding Register

Name: UART_RHR

Address: 0xF801C018 (0), 0xF8020018 (1), 0xF8024018 (2), 0xFC008018 (3), 0xFC00C018 (4)

Access: Read-only

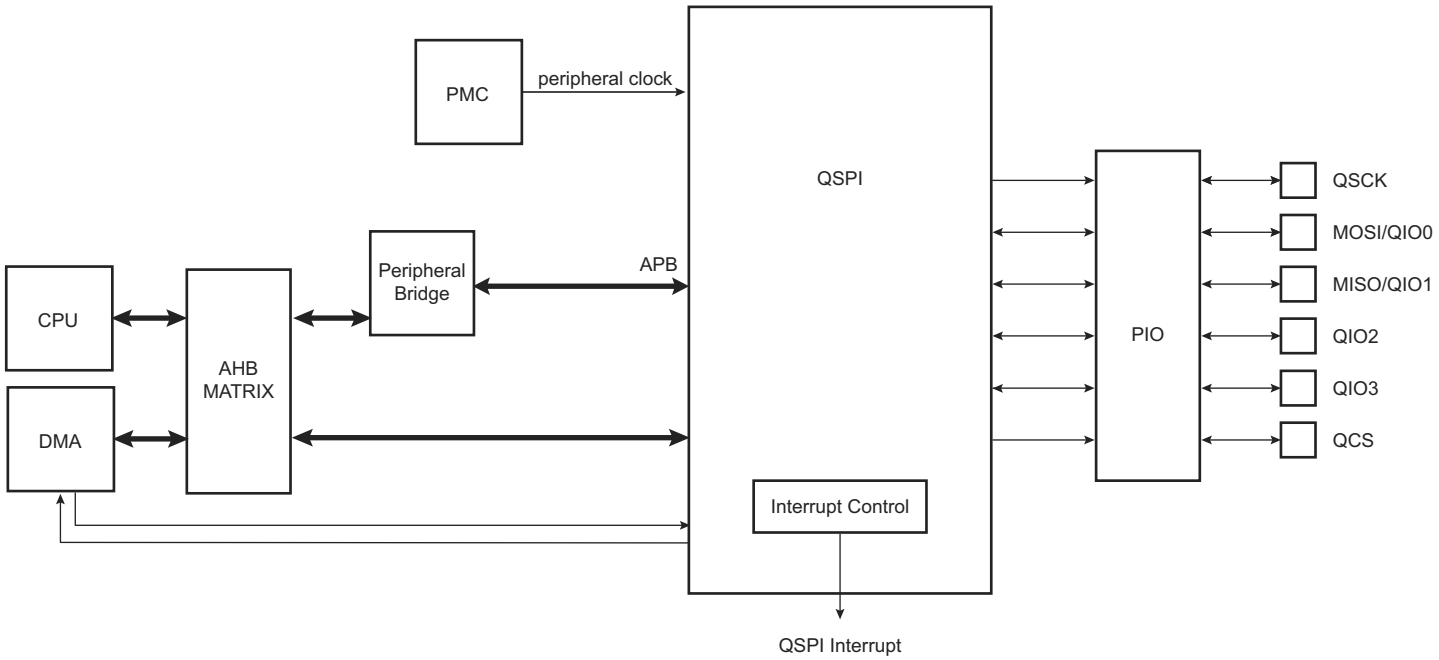
31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXCHR							

RXCHR: Received Character

Last received character if RXRDY is set.

50.3 Block Diagram

Figure 50-1: Block Diagram



50.4 Signal Description

Table 50-1: Signal Description

Pin Name	Pin Description	Type
QSCK	Serial Clock	Output
MOSI (QIO0) (1) (2)	Data Output (Data Input Output 0)	Output (Input/Output)
MISO (QIO1) (1) (2)	Data Input (Data Input Output 1)	Input (Input/Output)
QIO2 (3)	Data Input Output 2	Input/Output
QIO3 (3)	Data Input Output 3	Input/Output
QCS	Peripheral Chip Select	Output

Note 1: MOSI and MISO are used for single-bit SPI operation.

2: QIO0–QIO1 are used for Dual SPI operation.

3: QIO0–QIO3 are used for Quad SPI operation.

53.6.35 MCAN Tx Buffer Configuration

Name: MCAN_TXBC

Address: 0xF80540C0 (0), 0xFC0500C0 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	TFQM	TFQS					
23	22	21	20	19	18	17	16
–	–	NDTB					
15	14	13	12	11	10	9	8
TBSA							
7	6	5	4	3	2	1	0
TBSA						–	–

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

TBSA: Tx Buffers Start Address

Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 53-12).

Write TBSA with the bits [15:2] of the 32-bit address.

NDTB: Number of Dedicated Transmit Buffers

0: No dedicated Tx Buffers.

1-32: Number of dedicated Tx Buffers.

>32: Values greater than 32 are interpreted as 32.

TFQS: Transmit FIFO/Queue Size

0: No Tx FIFO/Queue.

1-32: Number of Tx Buffers used for Tx FIFO/Queue.

>32: Values greater than 32 are interpreted as 32.

TFQM: Tx FIFO/Queue Mode

0: Tx FIFO operation.

1: Tx Queue operation.

Note: The sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

A time base must be defined on channel 2 by writing the TC_RC2 period register. Channel 2 must be configured in Waveform mode (TC_CMR2.WAVE set). The TC_CMR.WAVSEL field must be defined with 0x10 to clear the counter by comparison and matching with TC_RC value. TC_CMR.ACPC must be defined at 0x11 to toggle TIOAx output.

This time base is automatically fed back to TIOAx of channel 0 when TC_BMR.QDEN and TC_BMR.SPEEDEN are set.

Channel 0 must be configured in Capture mode (TC_CMR0.WAVE = 0). TC_CMR0.ABETRG must be configured at 1 to select TIOAx as a trigger for this channel.

EDGTRG must be set to 0x01, to clear the counter on a rising edge of the TIOAx signal and field LDRA must be set accordingly to 0x01, to load TC_RA0 at the same time as the counter is cleared (LDRB must be set to 0x01). As a consequence, at the end of each time base period the differentiation required for the speed calculation is performed.

The process must be started by configuring bits CLKEN and SWTRG in the TC_CCR.

The speed can be read on TC_RA0.RA.

Channel 1 can still be used to count the number of revolutions of the motor.

54.6.16.6 Detecting a Missing Index Pulse

To detect a missing index pulse due contamination, dust, etc., the TC_SR0.CPCS flag can be used. It is also possible to assert the interrupt line if the TC_SR0.CPCS flag is enabled as a source of the interrupt by writing a ‘1’ to TC_IER0.CPCS.

The TC_RC0.RC field must be written with the nominal number of counts per revolution provided by the rotary encoder, plus a margin to eliminate potential noise (e.g., if nominal count per revolution is 1024, then TC_RC0.RC=1026).

If the index pulse is missing, the timer value is not cleared and the nominal value is exceeded, then the comparator on the RC triggers an event, TC_SR0.CPCS=1, and the interrupt line is asserted if TC_IER0.CPCS=1.

The missing index pulse detection is only valid if the bit TC_QISR.DIRCHG=0.

54.6.16.7 Detecting Contamination/Dust at Rotary Encoder Low Speed

The contamination/dust that can be filtered when the rotary encoder speed is high may not be filtered at low speed, thus creating unsollicited direction change, etc.

At low speed, even a minor contamination may appear as a long pulse, and thus not filtered and processed as a standard quadrature encoder pulse.

This contamination can be detected by using the similar method as the missing index detection.

A contamination exists on a phase line if TC_SR.CPCS = 1 and TC_QISR.DIRCHG = 1 when there is no sollicited change of direction.

54.6.16.8 Missing Pulse Detection and Autocorrection

The QDEC is equipped with a circuitry which detects and corrects some errors that may result from contamination on optical disks or other materials producing the quadrature phase signals.

The detection and autocorrection only works if the Count mode is configured for both phases (TC_BMR.EDGPHA = 1) and is enabled (TC_BMR.AUTOC = 1).

If a pulse is missing on a phase signal, it is automatically detected and the pulse count reported in the CV field of the TC_CV0/1 is automatically corrected.

There is no detection if both phase signals are affected at the same location on the device providing the quadrature signals because the detection requires a valid phase signal to detect the contamination on the other phase signal.

61.4.6 Automatic Padding

The SHA module features an automatic padding computation to speed up the execution of the algorithm.

The automatic padding function requires the following information:

- Complete message size in bytes to be written in the MSGSIZE field of the SHA Message Size register (SHA_MSR).
  The size of the message is written at the end of the last block, as required by the FIPS180-2 specification (the size is automatically converted into a bit-size).
- Number of remaining bytes (to write in the SHA_IDATARx) to be written in the BYTCNT field of the SHA Bytes Count register (SHA_BCR).
  Automatic padding occurs when the BYTCNT field reaches 0. At each write in the SHA Input registers, the BYTCNT field value is decreased by the number of bytes written.

The BYTCNT field value must be written with the same value as the MSGSIZE field value if the full message is processed. If the message is partially preprocessed and an initial hash value is used, BYTCNT must be written with the remaining bytes to hash while MSGSIZE holds the message size.

To disable the automatic padding feature, the MSGSIZE and BYTCNT fields must be configured with 0.

62.5.4 TDES Interrupt Disable Register

Name: TDES_IDR

Address: 0xFC044014

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	URAD
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

DATRDY: Data Ready Interrupt Disable

0: No effect.

1: Disables the corresponding interrupt.

URAD: Unspecified Register Access Detection Interrupt Disable

0: No effect.

1: Disables the corresponding interrupt.

65.6.15 Touchscreen

65.6.15.1 Touchscreen Mode

The TSMODE parameter of the ADC Touchscreen Mode register (ADC_TSMR) is used to enable/disable the touchscreen functionality, to select the type of screen (4-wire or 5-wire) and, in the case of a 4-wire screen and to activate (or not) the pressure measurement.

In 4-wire mode, channel 0, 1, 2 and 3 must not be used for classic ADC conversions. Likewise, in 5-wire mode, channel 0, 1, 2, 3, and 4 must not be used for classic ADC conversions.

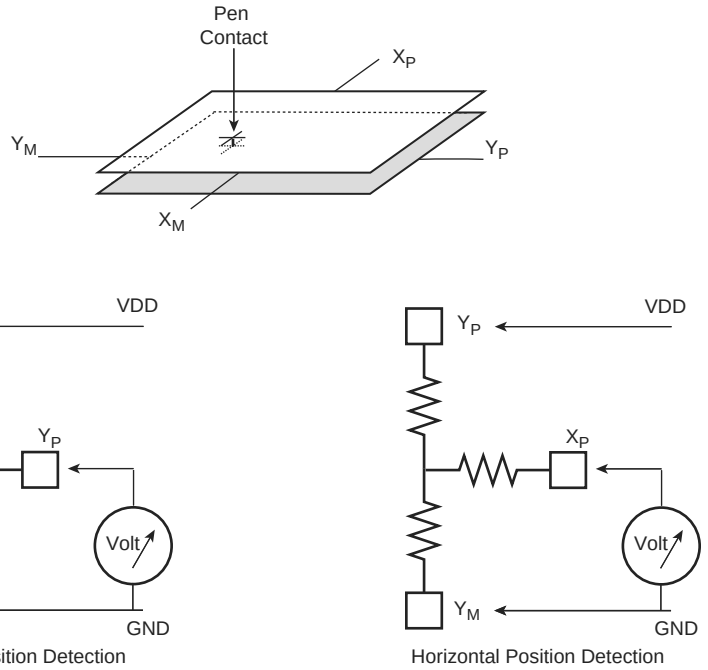
65.6.15.2 4-wire Resistive Touchscreen Principles

A resistive touchscreen is based on two resistive films, each one being fitted with a pair of electrodes, placed at the top and bottom on one film, and on the right and left on the other. In between, there is a layer acting as an insulator, but also enables contact when you press the screen. This is illustrated in Figure 65-14.

The ADC controller can perform the following tasks without external components:

- position measurement
- pressure measurement
- pen detection

Figure 65-14: Touchscreen Position Measurement



65.6.15.3 4-wire Position Measurement Method

As shown in Figure 65-14, to detect the position of a contact, a supply is first applied from top to bottom. Due to the linear resistance of the film, there is a voltage gradient from top to bottom. When a contact is performed on the screen, the voltage propagates at the point the two surfaces come into contact with the second film. If the input impedance on the right and left electrodes sense is high enough, the film does not affect this voltage, despite its resistive nature.

For the horizontal direction, the same method is used, but by applying supply from left to right. The range depends on the supply voltage and on the loss in the switches that connect to the top and bottom electrodes.

In an ideal world (linear, with no loss through switches), the horizontal position is equal to:

VY_M / VDD or VY_P / VDD.

The implementation with on-chip power switches is shown in Figure 65-15. The voltage measurement at the output of the switch compensates for the switches loss.

It is possible to correct for switch loss by performing the operation:

Figure 66-23: SPI Slave Mode - NPCS Timings

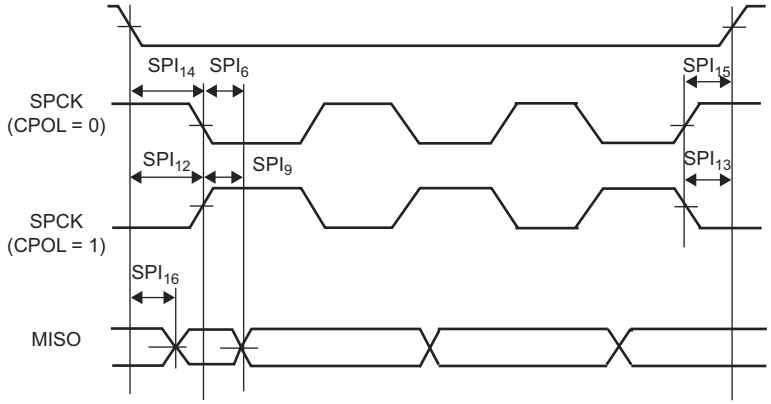
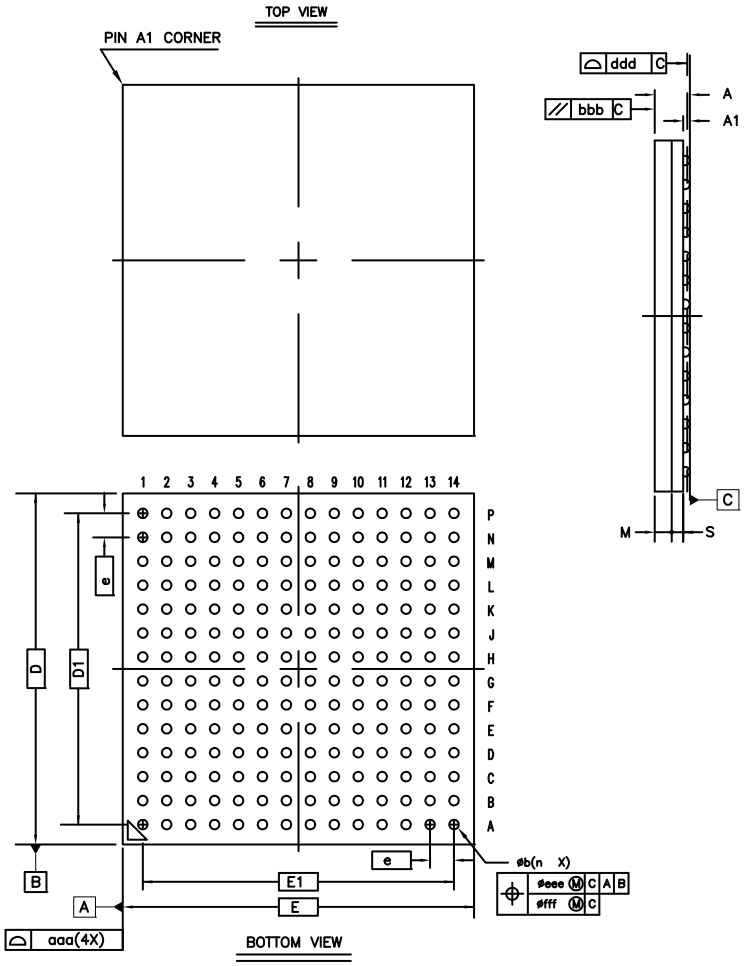


Table 66-64: SPI0 IOSET1 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
	Master Mode					
SPI_0	MISO Setup time before SPCK rises	14.3	–	12.4	–	ns
SPI_1	MISO Hold time after SPCK rises	0	–	0	–	ns
SPI_2	SPCK rising to MOSI	0	1.9	0	2.4	ns
SPI_3	MISO Setup time before SPCK falls	13.8	–	12.6	–	ns
SPI_4	MISO Hold time after SPCK falls	0	–	0	–	ns
SPI_5	SPCK falling to MOSI	0	1.2	0	2.3	ns
	Slave Mode					
SPI_6	SPCK falling to MISO	10.5	12.6	8.4	10.9	ns
SPI_7	MOSI Setup time before SPCK rises	1.5	–	1.4	–	ns
SPI_8	MOSI Hold time after SPCK rises	1.7	–	1.5	–	ns
SPI_9	SPCK rising to MISO	10	12	8	10.2	ns
SPI_{10}	MOSI Setup time before SPCK falls	1.5	–	1.4	–	ns
SPI_{11}	MOSI Hold time after SPCK falls	1.7	–	1.5	–	ns
SPI_{12}	NPCS0 setup to SPCK rising	4.4	–	4.3	–	ns
SPI_{13}	NPCS0 hold after SPCK falling	1.5	–	1.3	–	ns
SPI_{14}	NPCS0 setup to SPCK falling	3.9	–	3.9	–	ns
SPI_{15}	NPCS0 hold after SPCK rising	0.8	–	0.5	–	ns
SPI_{16}	NPCS0 falling to MISO valid	13.3	–	11.7	–	ns

67.3 196-ball TFBGA Mechanical Characteristics

Figure 67-3: 196-ball TFBGA Package Details



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			TFBGA		
Body Size:	X	E	11.000		
	Y	D	11.000		
Ball Pitch :		e	0.750		
Total Thickness :		A			1.200
Mold Thickness :		M	0.530 Ref.		
Substrate Thickness :		S	0.360 Ref.		
Ball Diameter :			0.300		
Stand Off :		A1	0.160		0.260
Ball Width :		b	0.270		0.370
Package Edge Tolerance :		aaa	0.100		
Mold Parallelism :		bbb	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	196		
Edge Ball Center to Center :	X	E1	9.750		
	Y	D1	9.750		

Table 67-9: 196-ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 67-10: Device and 196-ball TFBGA Package Weight

234.2	mg

Table 67-11: Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

Table 67-12: 196-ball TFBGA Package Information

Ball Land	0.350 mm +/-0.05
Nominal Ball Diameter	0.3 mm
Solder Mask Opening	0.275 mm +/-0.30
Solder Mask Definition	SMD
Solder	OSP

Table 72-3: SAMA5D2 Datasheet Rev. 11267E Revision History

Issue Date	Changes
25-Jul-16	Deleted Section 61. “Security Module”.

Table 72-4: SAMA5D2 Datasheet Rev. 11267D Revision History

Issue Date	Changes
12-May-16	Minor formatting and editorial changes throughout
	“Introduction” Updated listed DDR memories
	“Features” Frequency of digital fractional PLL for audio “11.289 MHz” corrected to “11.2896 MHz” “Two 64-bit, 16-channel DMA controllers” changed to “51 DMA Channels including two 16-channel 64-bit Central DMA Controllers”
	Section 1. “Description” Updated description of Low-power modes
	Section 2. “Configuration Summary” “Class D amplifier” changed to “stereo Class D amplifier” Updated text at end of section
	Section 3. “Block Diagram” Figure 3-1 “SAMA5D2 Series Block Diagram”: added ISC_MSK input; updated description of crystal oscillators; “PWMEXTRIG0-1” renumbered to “PWMEXTRG1–2” Added note “See Section 35. “DMA Controller (XDMAC)” for peripheral connections to DMA.”
	Section 4. “Signal Description” Table 4-1 “Signal Description List”: NRST signal function “Microcontroller Reset” changed to “Microprocessor Reset”; “PWMEXTRG0-1” renumbered to “PWMEXTRG1–2”; “Self-refresh mode” changed to “Backup Self-refresh mode” in DDR_CKE comments
	Section 5. “Package and Pinout” Separated content into Section 5.1 “Packages” and Section 5.2 “Pinouts” Table 5-2 “Pin Description (SAMA5D21, SAMA5D22, SAMA5D24, SAMA5D26, SAMA5D27, SAMA5D28A)”: “ADVREFP” corrected to “ADVREF”; “PWMEXTRG0” and “PWMEXTRG1” renumbered to “PWMEXTRG1” and “PWMEXTRG2”; removed empty function cells for primary signals PA30, PA31, and PB0–PB7; removed “SEC, FILTER” from “Reset State” column header; added footnote on reset states Added Table 5-3 “Pin Description (SAMA5D23 pins different from those in SAMA5D21/SAMA5D22)” and Table 5-4 “Pin Description (SAMA5D28B pins different from those in SAMA5D28A)”
	Section 6. “Power Considerations” Table 6-1 “SAMA5D2 Power Supplies”: updated rows VDDUTMIC, VDDHSIC and VDDOSC Section 6.4.1 “VDDBU Power Architecture”: reworded second paragraph and deleted “typically less than 2 µA”
	Section 7. “Memories” Section 7.2.1 “External Bus Interface”: “The slew rates are determined by programming the SFR_EBICFG bit in SFR registers” changed to “The drive levels are configured with the DRIVEx field in the EBI Configuration Register (SFR_EBICFG)”