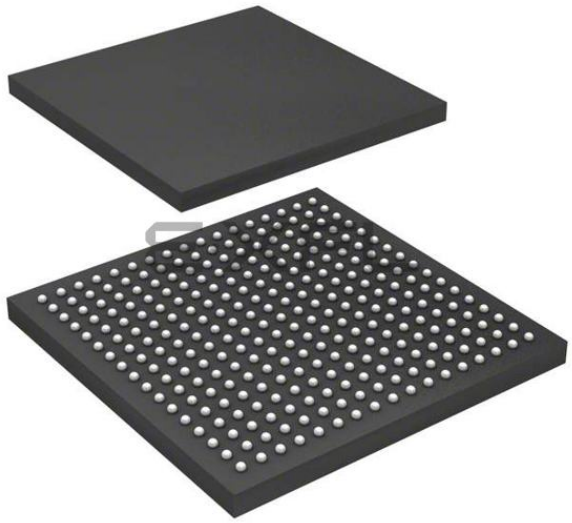

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27b-cu

- 24 KΩ for LPDDR2/LPDDR3
- 23 KΩ for DDR3L
- 22 KΩ for DDR3
- 21 KΩ for DDR2/LPDDR1

The typical value for CZQ is 22 pF.

• LPDDR2 Power Fail Management

The DDR controller (MPDDRC) is used to manage the LPDDR memory when an uncontrolled power off occurs.

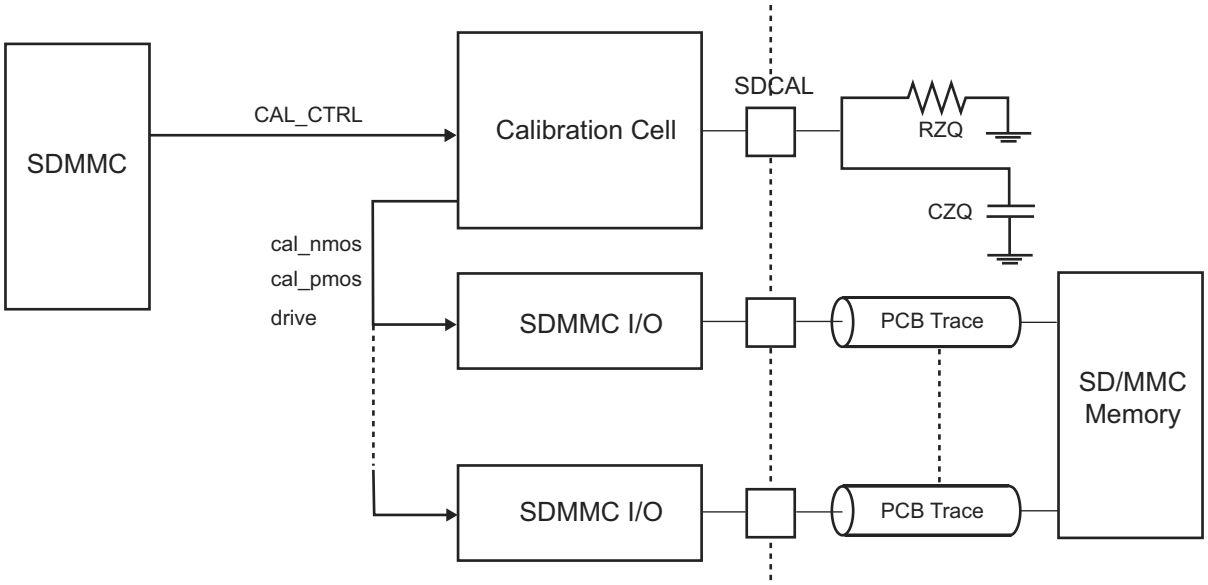
The DDR power rail must be monitored externally and generate an interrupt when a power fail condition is triggered. The interrupt handler must apply the sequence defined in the MPDDRC Low-power register (MPDDRC_LPR) by setting bit LPDDR2_PWOFF (LPDDR2 Power Off bit).

8.2.4.2 SDMMC I/O Calibration

The SAMA5D2 also embeds an SDMMC I/O calibration cell. The purpose of this block is to provide to e.MMC/SD I/Os an output impedance reference to limit the impact of process, voltage and temperature on the drivers output impedance. The impedance control is required at high frequency in order to improve signal quality.

The control and procedure to setup the SDMMC calibration cell is described in Section 51. “Secure Digital MultiMedia Card Controller (SDMMC)”.

Figure 8-3: SDMMC I/O Calibration Cell



The calibration cell provides an input pin SDCAL loaded with a 20 KΩ resistor for 1.8V memories and a 16.9 KΩ resistor for 3.3V memories.

According to the e.MMC specification, the output impedance calibration is mandatory for HS200 mode (1.8V) when it is not for other modes (3.3V).

In addition, according to the SD specification, the output impedance calibration is mandatory for 1.8V signaling when it is not for 3.3V signaling.

Thus, the calibration cell design is oriented to get the highest accuracy under 1.8V.

In case of interfacing which would need to operate under both 1.8V and 3.3V, external devices RZQ and CZQ must get values related to the 1.8V mode. The typical value for CZQ is 22 pF.

Table 18-9: Peripheral Identifiers (Continued)

ID	Peripheral	Security Type	Matrix	MATRIX_SPSELRx Bit	Bit Value in H32MX	Bit Value in H64MX
47	TRNG	PS	H32MX	MATRIX_SPSELR2[15]	UD	1
48	PDMIC	PS	H32MX	MATRIX_SPSELR2[16]	UD	1
49	AIC	Peripheral Always Non-secured (PNS)	H32MX	MATRIX_SPSELR2[17]	1	1
50	SFC	PS	H32MX	MATRIX_SPSELR2[18]	UD	1
51	SECURAM	PAS	H32MX	MATRIX_SPSELR2[19]	0	1
52	QSPI0	PS	H64MX	MATRIX_SPSELR2[20]	1	UD
53	QSPI1	PS	H64MX	MATRIX_SPSELR2[21]	1	UD
54	I2SC0	PS	H32MX	MATRIX_SPSELR2[22]	UD	1
55	I2SC1	PS	H32MX	MATRIX_SPSELR2[23]	UD	1
56	CAN0	PS	H32MX	MATRIX_SPSELR2[24]	UD	1
57	CAN1	PS	H32MX	MATRIX_SPSELR2[25]	UD	1
58	PTC	PS	H32MX	MATRIX_SPSELR2[26]	UD	1
59	CLASSD	PS	H32MX	MATRIX_SPSELR2[27]	UD	1
60	SFR	PS	H32MX	MATRIX_SPSELR2[28]	UD	1
61	SAIC	PAS	H32MX	MATRIX_SPSELR2[29]	0	1
62	AIC	PNS	H32MX	MATRIX_SPSELR2[30]	1	1
63	L2CC	PS	H64MX	MATRIX_SPSELR2[31]	1	UD
64	CAN0	PS	H32MX	MATRIX_SPSELR3[0]	UD	1
65	CAN1	PS	H32MX	MATRIX_SPSELR3[1]	UD	1
66	GMAC	PS	H32MX	MATRIX_SPSELR3[2]	UD	1
67	GMAC	PS	H32MX	MATRIX_SPSELR3[3]	UD	1
68	PIOB	PAS	H32MX	MATRIX_SPSELR3[4]	0	1
69	PIOC	PAS	H32MX	MATRIX_SPSELR3[5]	0	1
70	PIOD	PAS	H32MX	MATRIX_SPSELR3[6]	0	1
71	SDMMC0	PS	H32MX	MATRIX_SPSELR3[7]	UD	1
72	SDMMC1	PS	H32MX	MATRIX_SPSELR3[8]	UD	1
73	–	–	–	–	–	–
74	RTC, RSTC, PMC	PS	H32MX	MATRIX_SPSELR3[9]	UD	1
75	ACC	PS	H32MX	MATRIX_SPSELR3[10]	UD	1
76	RXLP	PS	H32MX	MATRIX_SPSELR3[11]	UD	1
77	SFRBU	PS	H32MX	MATRIX_SPSELR3[12]	UD	1
78	CHIPID	PS	H32MX	MATRIX_SPSELR3[13]	UD	1

The AHB/APB Bridge compares the incoming master request security bit with the required security mode for the selected peripheral, and accepts or denies access. In the last case, its bus error response is internally flagged in the Bus Matrix Master Error Status Register; the offending address is registered in the Master Error Address Registers so that the slave and the targeted protected region are also known.

Table 36-20: Interleaved Mapping DDR-SDRAM Configuration Mapping: 8K Rows /512/1024/2048 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			Row[13:0]													Bk[1:0]	Column[8:0]										M[1:0]	
			Row[13:0]												Bk[1:0]	Column[9:0]										M[1:0]		
		Row[13:0]												Bk[1:0]	Column[10:0]										M[1:0]			

Table 36-21: Sequential Mapping DDR-SDRAM Configuration Mapping: 8K Rows /1024 Columns, 8 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Bk[2:0]			Row[12:0]													Column[9:0]										M[1:0]	

Table 36-22: Interleaved Mapping DDR-SDRAM Configuration Mapping: 8K Rows /1024 Columns, 8 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Row[12:0]													Bk[2:0]			Column[9:0]										M[1:0]	

Table 36-23: Sequential Mapping DDR-SDRAM Configuration Mapping: 16K Rows /1024 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Bk[1:0]		Row[13:0]														Column[9:0]										M[1:0]	

Table 36-24: Interleaved Mapping DDR-SDRAM Configuration Mapping: 16K Rows /1024 Columns, 4 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Row[13:0]														Bk[1:0]		Column[9:0]										M[1:0]	

Table 36-25: Sequential Mapping DDR-SDRAM Configuration Mapping: 16K Rows /1024 Columns, 8 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bk[2:0]			Row[13:0]														Column[9:0]										M[1:0]	

Table 36-26: Interleaved Mapping DDR-SDRAM Configuration Mapping: 16K Rows /1024 Columns, 8 banks

CPU Address Line																												
28	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Row[13:0]														Bk[2:0]			Column[9:0]										M[1:0]	

REP: Use Replication logic to expand RGB color to 24 bits

0: When the selected pixel depth is less than 24 bpp the pixel is shifted and least significant bits are set to 0.

1: When the selected pixel depth is less than 24 bpp the pixel is shifted and the least significant bit replicates the msb.

DSTKEY: Destination Chroma Keying

0: Source Chroma keying is enabled.

1: Destination Chroma keying is used.

GA: Blender Global Alpha

Global alpha blender for the current layer.

39.7.102 High-End Overlay Configuration Register 7

Name: LCDC_HEOCFG7

Address: 0xF00003A8

Access: Read/Write

31	30	29	28	27	26	25	24
UVXSTRIDE							

23	22	21	20	19	18	17	16
UVXSTRIDE							

15	14	13	12	11	10	9	8
UVXSTRIDE							

7	6	5	4	3	2	1	0
UVXSTRIDE							

UVXSTRIDE: UV Horizontal Stride

UVXSTRIDE represents the memory offset, in bytes, between two rows of the image memory.

39.7.110 High-End Overlay Configuration Register 15

Name: LCDC_HEOCFG15

Address: 0xF00003C8

Access: Read/Write

31	30	29	28	27	26	25	24
–	CSCUOFF	CSCGV					

23	22	21	20	19	18	17	16
CSCGV				CSCGU			

15	14	13	12	11	10	9	8
CSCGU						CSCGY	

7	6	5	4	3	2	1	0
CSCGY							

CSCGY: Color Space Conversion Y coefficient for Green Component 1:2:7 format

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

CSCGU: Color Space Conversion U coefficient for Green Component 1:2:7 format

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

CSCGV: Color Space Conversion V coefficient for Green Component 1:2:7 format

Color Space Conversion coefficient format is 1 sign bit, 2 magnitude bits and 7 fractional bits.

CSCUOFF: Color Space Conversion Offset

0: Offset is set to 0

1: Offset is set to 128

Transmitter checksum offload is enabled by setting bit [11] in the DMA Configuration register. When enabled, it will monitor the frame as it is written into the transmitter packet buffer memory to automatically detect the protocol of the frame. Protocol support is identical to the receiver checksum offload.

For transmit checksum generation and substitution to occur, the protocol of the frame must be recognized and the frame must be provided without the FCS field, by making sure that bit [16] of the transmit descriptor word 1 is clear. If the frame data already had the FCS field, this would be corrupted by the substitution of the new checksum fields.

If these conditions are met, the transmit checksum offload engine will calculate the IP, TCP and UDP checksums as appropriate. Once the full packet is completely written into packet buffer memory, the checksums will be valid and the relevant DPRAM locations will be updated for the new checksum fields as per standard IP/TCP and UDP packet structures.

If the transmitter checksum engine is prevented from generating the relevant checksums, bits [22:20] of the transmitter DMA writeback status will be updated to identify the reason for the error. Note that the frame will still be transmitted but without the checksum substitution, as typically the reason that the substitution did not occur was that the protocol was not recognized.

40.6.7 MAC Filtering Block

The filter block determines which frames should be written to the FIFO interface and on to the DMA.

Whether a frame is passed depends on what is enabled in the Network Configuration register, the state of the external matching pins, the contents of the specific address, type and Hash registers and the frame's destination address and type field.

If bit 25 of the Network Configuration register is not set, a frame will not be copied to memory if the GMAC is transmitting in half duplex mode at the time a destination address is received.

Ethernet frames are transmitted a byte at a time, least significant bit first. The first six bytes (48 bits) of an Ethernet frame make up the destination address. The first bit of the destination address, which is the LSB of the first byte of the frame, is the group or individual bit. This is one for multicast addresses and zero for unicast. The all ones address is the broadcast address and a special case of multicast.

The GMAC supports recognition of four specific addresses. Each specific address requires two registers, Specific Address Bottom register and Specific Address Top register. Specific Address Bottom register stores the first four bytes of the destination address and Specific Address Top register contains the last two bytes. The addresses stored can be specific, group, local or universal.

The destination address of received frames is compared against the data stored in the Specific Address registers once they have been activated. The addresses are deactivated at reset or when their corresponding Specific Address Bottom register is written. They are activated when Specific Address Top register is written. If a receive frame address matches an active address, the frame is written to the FIFO interface and on to DMA memory.

Frames may be filtered using the type ID field for matching. Four type ID registers exist in the register address space and each can be enabled for matching by writing a one to the MSB (bit 31) of the respective register. When a frame is received, the matching is implemented as an OR function of the various types of match.

The contents of each type ID register (when enabled) are compared against the length/type ID of the frame being received (e.g., bytes 13 and 14 in non-VLAN and non-SNAP encapsulated frames) and copied to memory if a match is found. The encoded type ID match bits (Word 0, Bit 22 and Bit 23) in the receive buffer descriptor status are set indicating which type ID register generated the match, if the receive checksum offload is disabled.

The reset state of the type ID registers is zero, hence each is initially disabled.

The following example illustrates the use of the address and type ID match registers for a MAC address of 21:43:65:87:A9:CB:

Preamble	55
SFD	D5
DA (Octet 0 - LSB)	21
DA (Octet 1)	43
DA (Octet 2)	65
DA (Octet 3)	87
DA (Octet 4)	A9
DA (Octet 5 - MSB)	CB
SA (LSB)	00(1)

40.8.10 GMAC Interrupt Status Register

Name: GMAC_ISR

Address: 0xF8008024

Access: Read-only

31	30	29	28	27	26	25	24
–	–	TSUTIMCOMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
23	22	21	20	19	18	17	16
PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR	–	–
15	14	13	12	11	10	9	8
–	PFTR	PTZ	PFNZ	HRESP	ROVR	–	–
7	6	5	4	3	2	1	0
TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS

This register indicates the source of the interrupt. In order that the bits of this register read 1, the corresponding interrupt source must be enabled in the mask register. If any bit is set in this register, the GMAC interrupt signal will be asserted in the system.

MFS: Management Frame Sent

The PHY Maintenance Register has completed its operation. Cleared on read.

RCOMP: Receive Complete

A frame has been stored in memory. Cleared on read.

RXUBR: RX Used Bit Read

Set when a receive buffer descriptor is read with its used bit set. Cleared on read.

TXUBR: TX Used Bit Read

Set when a transmit buffer descriptor is read with its used bit set. Cleared on read.

TUR: Transmit Underrun

This interrupt is set if the transmitter was forced to terminate a frame that it has already began transmitting due to further data being unavailable.

This interrupt is set if a transmitter status write back has not completed when another status write back is attempted.

This interrupt is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB not OK response was returned, or because the used bit was read.

RLEX: Retry Limit Exceeded

Transmit error. Cleared on read.

TFC: Transmit Frame Corruption Due to AHB Error

Transmit frame corruption due to AHB error. Set if an error occurs while midway through reading transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame.

TCOMP: Transmit Complete

Set when a frame has been transmitted. Cleared on read.

ROVR: Receive Overrun

Set when the receive overrun status bit is set. Cleared on read.

HRESP: HRESP Not OK

Set when the DMA block sees HRESP not OK. Cleared on read.

PFNZ: Pause Frame with Non-zero Pause Quantum Received

40.8.27 GMAC Specific Address 3 Top Register

Name: GMAC_SAT3

Address: 0xF800809C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

ADDR: Specific Address 3

The most significant bits of the destination address, that is, bits 47:32.

The transmitter can also drive the TK I/O pad continuously or be limited to the current data transfer. The clock output is configured by the SSC_TCMR. The Transmit Clock Inversion (CKI) bits have no effect on the clock outputs. Programming the SSC_TCMR to select TK pin (CKS field) and at the same time Continuous Transmit Clock (CKO field) can lead to unpredictable results.

Figure 45-9: Transmit Clock Management

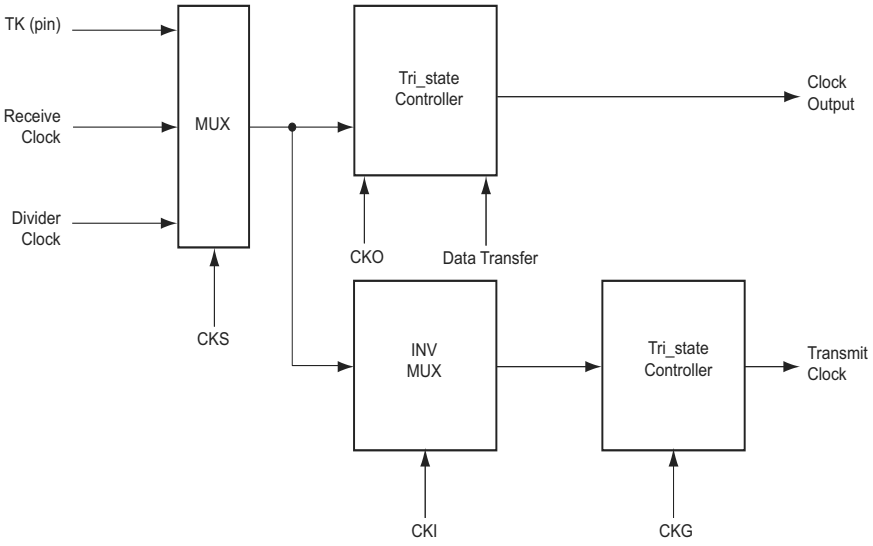


Figure 46-4: Master Write with One Data Byte

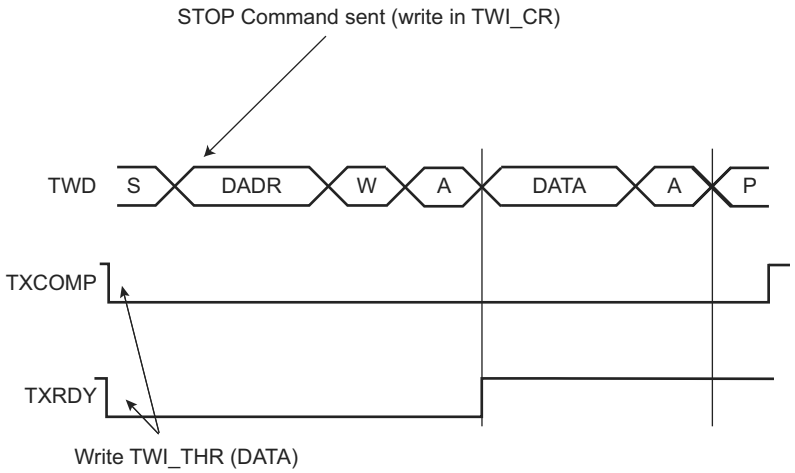


Figure 46-5: Master Write with Multiple Data Bytes

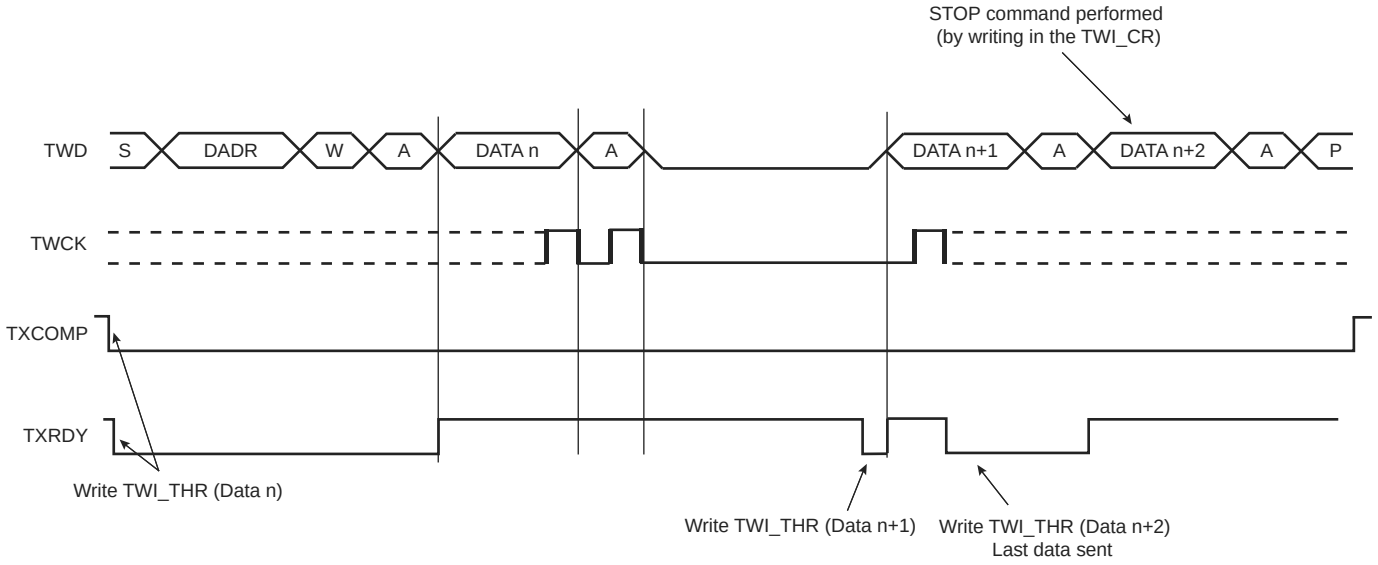
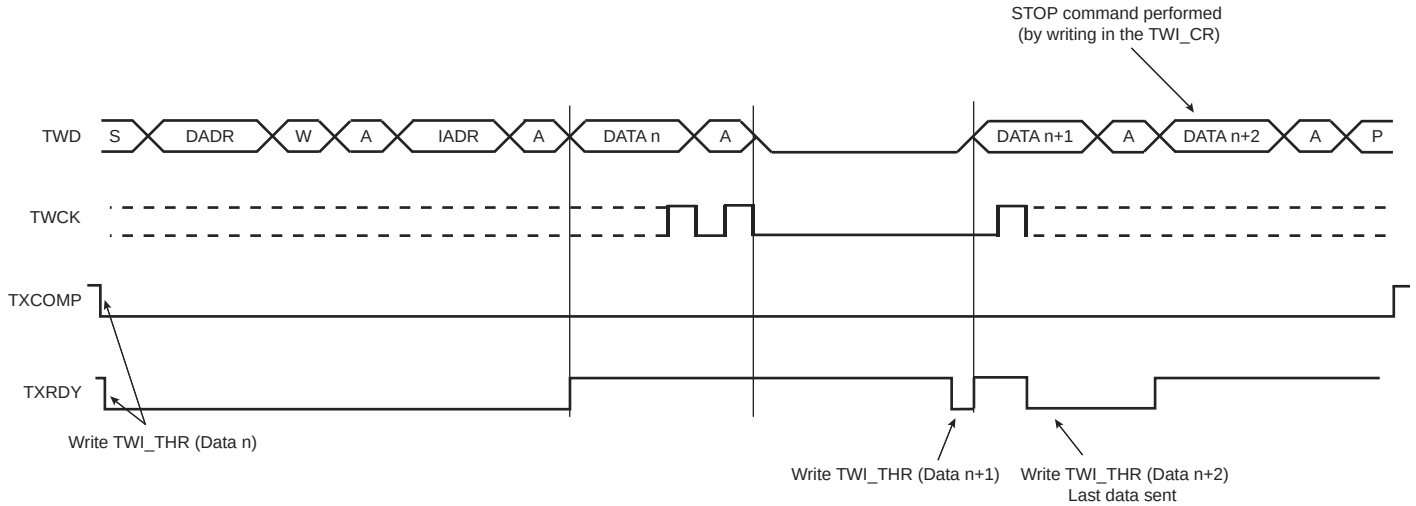


Figure 46-6: Master Write with One-Byte Internal Address and Multiple Data Bytes



47.10.26 USART Transmitter Timeguard Register

Name: FLEX_US_TTGR

Address: 0xF8034228 (0), 0xF8038228 (1), 0xFC010228 (2), 0xFC014228 (3), 0xFC018228 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TG							

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

TG: Timeguard Value

0: The transmitter timeguard is disabled.

1–255: The transmitter timeguard is enabled and TG is timeguard delay / bit period.

- SDMMC Clock Control 2 Register
- SDMMC Retuning Control 1 Register
- SDMMC Retuning Counter Value Register
- SDMMC Retuning Interrupt Status Enable Register
- SDMMC Retuning Interrupt Signal Enable Register
- SDMMC Retuning Interrupt Status Register
- SDMMC Tuning Control Register
- SDMMC Capabilities Control Register (except KEY)
- SDMMC Calibration Control Register (except CALN, CALP)

0: Work

1: Reset

SWRSTCMD: Software reset for CMD line

Only part of a command circuit is reset.

The following registers and bits are cleared by this bit:

“SDMMC Present State Register”

- Command Inhibit (CMD) (CMDINHC)

“SDMMC Normal Interrupt Status Register (SD_SDIO)” and “SDMMC Normal Interrupt Status Register (e.MMC)”

- Command Complete (CMDC)

0: Work

1: Reset

SWRSTDAT: Software reset for DAT line

Only part of a data circuit is reset. The DMA circuit is also reset.

The following registers and bits are cleared by this bit:

“SDMMC Buffer Data Port Register”

- Buffer is cleared and initialized.

“SDMMC Present State Register”

- Buffer Read Enable (BUFRDEN)
- Buffer Write Enable (BUFWREN)
- Read Transfer Active (RTACT)
- Write Transfer Active (WTACT)
- DAT Line Active (DATLL)
- Command Inhibit (DAT) (CMDINHD)

“SDMMC Block Gap Control Register (SD_SDIO)”

- Continue Request (CONTR)
- Stop At Block Gap Request (STPBGR)

“SDMMC Normal Interrupt Status Register (SD_SDIO)”

- Buffer Read Ready (BRDRDY)
- Buffer Write Ready (BWRRDY)
- DMA Interrupt (DMAINT)
- Block Gap Event (BLKGE)

52.6.48 ISC Rounding, Limiting and Packing Configuration Register

Name: ISC_RLP_CFG

Address: 0xF00083D0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ALPHA							

7	6	5	4	3	2	1	0
–	–	–	–	MODE			

MODE: Rounding, Limiting and Packing Mode

Value	Name	Description
0	DAT8	8-bit data
1	DAT9	9-bit data
2	DAT10	10-bit data
3	DAT11	11-bit data
4	DAT12	12-bit data
5	DATY8	8-bit luminance only
6	DATY10	10-bit luminance only
7	ARGB444	12-bit RGB+4-bit Alpha (MSB)
8	ARGB555	15-bit RGB+1-bit Alpha (MSB)
9	RGB565	16-bit RGB
10	ARGB32	24-bits RGB mode+8-bit Alpha
11	YYCC	YCbCr mode (full range, [0–255])
12	YYCC_LIMITED	YCbCr mode (limited range)

ALPHA: Alpha Value for Alpha-enabled RGB Mode

- **R1 Bit 20 BRS: Bit Rate Switch**

0: Frame received without bit rate switching.

1: Frame received with bit rate switching.

Note: Bits ESI, FDF, and BRS are only evaluated when CAN FD operation is enabled (MCAN_CCCR.FDOE = 1). Bit BRS is only evaluated when in addition MCAN_CCCR.BRSE = 1.

- **R1 Bits 19:16 DLC[3:0]: Data Length Code**

0-8: CAN + CAN FD: received frame has 0-8 data bytes.

9-15: CAN: received frame has 8 data bytes.

9-15: CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

- **R1 Bits 15:0 RXTS[15:0]: Rx Timestamp**

Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC.TCP.

- **R2 Bits 31:24 DB3[7:0]: Data Byte 3**
- **R2 Bits 23:16 DB2[7:0]: Data Byte 2**
- **R2 Bits 15:8 DB1[7:0]: Data Byte 1**
- **R2 Bits 7:0 DB0[7:0]: Data Byte 0**
- **R3 Bits 31:24 DB7[7:0]: Data Byte 7**
- **R3 Bits 23:16 DB6[7:0]: Data Byte 6**
- **R3 Bits 15:8 DB5[7:0]: Data Byte 5**
- **R3 Bits 7:0 DB4[7:0]: Data Byte 4**

....

- **Rn Bits 31:24 DBm[7:0]: Data Byte m**
- **Rn Bits 23:16 DBm-1[7:0]: Data Byte m-1**
- **Rn Bits 15:8 DBm-2[7:0]: Data Byte m-2**
- **Rn Bits 7:0 DBm-3[7:0]: Data Byte m-3**

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3 ..17) are used for storage of a CAN message's data field.

53.6.12 MCAN Timeout Counter Value Register

Name: MCAN_TOCV

Address: 0xF805402C (0), 0xFC05002C (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
TOC							
7	6	5	4	3	2	1	0
TOC							

TOC: Timeout Counter (cleared on write)

The Timeout Counter is decremented in multiples of CAN bit times [1…16] depending on the configuration of MCAN_TSCC.TCP. When decremented to zero, interrupt flag MCAN_IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via MCAN_TOCC.TOS.

57.5.2 SFC Mode Register

Name: SFC_MR

Address: 0xF804C004

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	SASEL	–	–	–	MSK

MSK: Mask Data Registers

0: No effect

1: The data registers from SFC_DR20 to SFC_DR23 are always read at 0x00000000.

Note: The MSK bit is set-only. Only a hardware reset can disable fuse masking.

SASEL: Sense Amplifier Selection

0: Comparator type sense amplifier selected

1: Latch type sense amplifier selected

To calculate the initial HMAC values, follow this sequence:

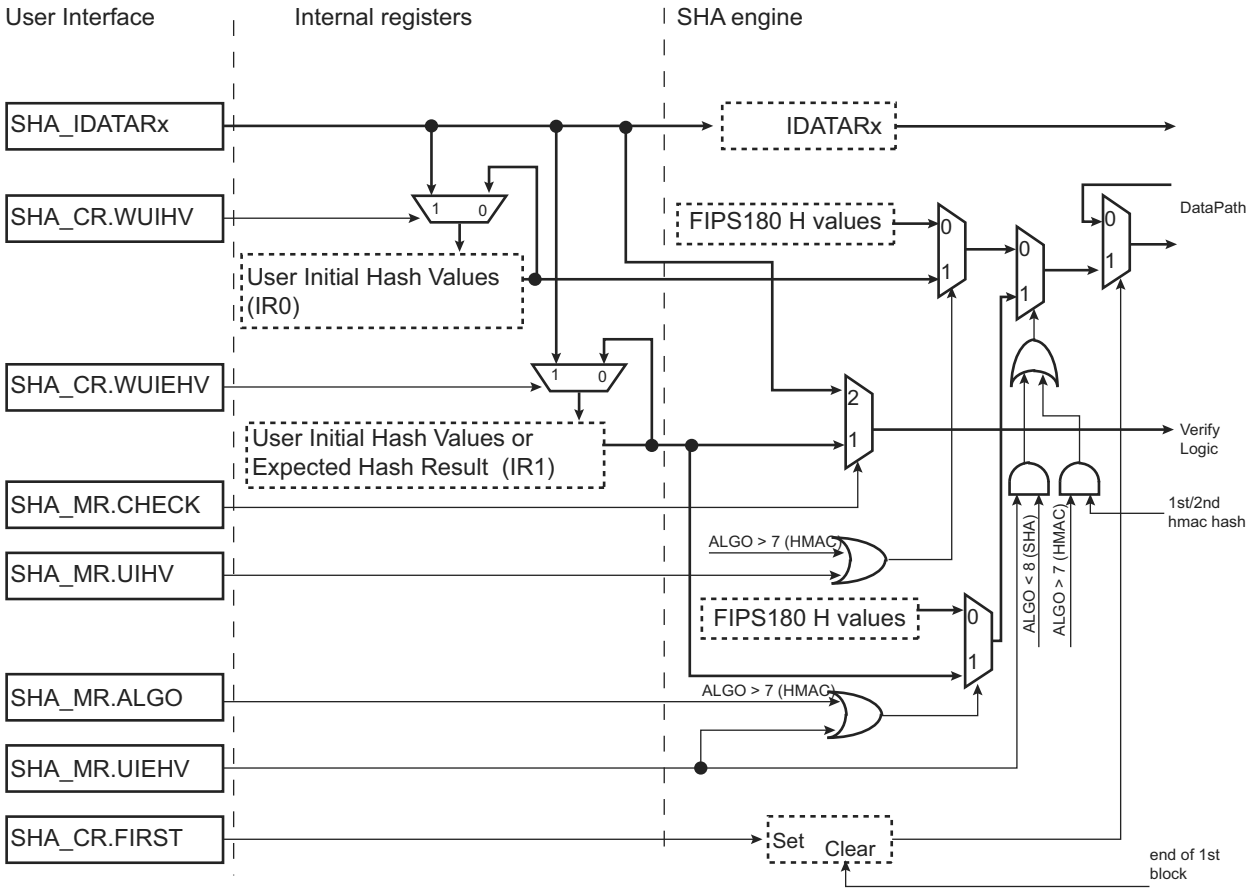
1. Calculate K_0.
2. Calculate $K_0 \oplus$ ipad and $K_0 \oplus$ opad.
3. Perform a hash of the result of $K_0 \oplus$ ipad and $K_0 \oplus$ opad (auto-padding must be disabled for that type of hash).
4. Write h($K_0 \oplus$ ipad) and h($K_0 \oplus$ opad) in IR0 and IR1 respectively.

To write IR0 or IR1, follow this sequence:

1. Set SHA_CR. WUIHV (IR0) or SHA_CR.WUIEHV (IR1).
2. Write the data in SHA_IDATARx. The number of registers to write depends on the type of data (user initial hash values or expected hash result) and on the type of algorithm selected:
   - SHA_IDATAR0 to SHA_IDATAR4 for data used in algorithms based on SHA1
   - SHA_IDATAR0 to SHA_IDATAR7 for data used in algorithms based on SHA256
   - SHA_IDATAR0 to SHA_IDATAR15 for data used in algorithms based on SHA512
   - SHA_IDATAR0 to SHA_IDATAR6 for expected hash result of algorithms based on SHA224
   - SHA_IDATAR0 to SHA_IDATAR11 for expected hash result of algorithms based on SHA384
3. Clear SHA_CR.WUIHV or SHA_CR.WUIEHV.

IR0 and IR1 are automatically selected for HMAC processing if the field ALGO selects HMAC algorithms. If SHA algorithms are selected, the internal registers are selected if the corresponding UIHV or UIEHV bits are set.

Figure 61-1: User Initial Hash Value and Expected Hash Internal Register Access



63.6.2 TRNG Interrupt Enable Register

Name: TRNG_IER

Address: 0xFC01C010

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

DATRDY: Data Ready Interrupt Enable

0: No effect.

1: Enables the corresponding interrupt.

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