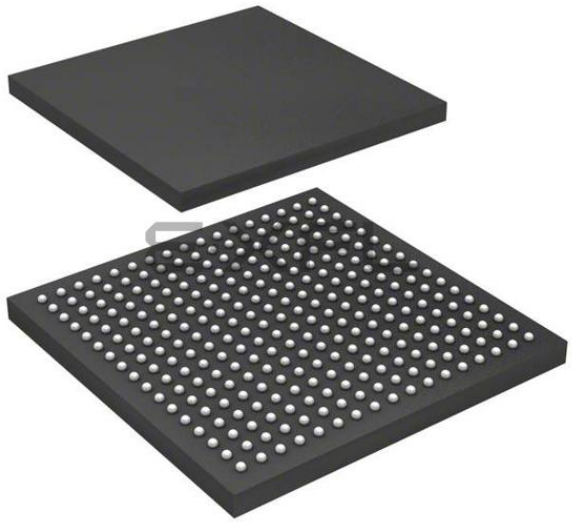

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27b-cur

20.3.3 SFRBU DDR BU Mode Control Register

Name: SFRBU_DDRBUMCR

Address: 0xFC05C010

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	BUMEN

BUMEN: DDR BU Mode Enable

This bit is used to isolate the DDR Pads from the CPU domain (VDDCORE).

It has to be set after enabling the Self-refresh mode on the DDR memory and before doing power-down on VDDCORE.(1)

0 (Reset value): DDR Backup mode disabled. The DDR pads are not isolated from CPU domain.

1: DDR Backup mode enabled. The DDR pads are isolated from CPU domain (IOs are in memory state).

Note 1: To enable Self-refresh mode, refer to MPDDRC Low-power Register (in Multi-port DDR-SDRAM Controller section) and to Self-refresh Backup mode (in Electrical Characteristics section).

21.9.3 AIC Source Vector Register

Name: AIC_SVR

Address: 0xFC020008 (AIC), 0xF803C008 (SAIC)

Access: Read/Write

31	30	29	28	27	26	25	24
VECTOR							

23	22	21	20	19	18	17	16
VECTOR							

15	14	13	12	11	10	9	8
VECTOR							

7	6	5	4	3	2	1	0
VECTOR							

This register can only be written if the WPEN bit is cleared in the AIC Write Protection Mode Register.

VECTOR: Source Vector

The user may store in this register the address of the corresponding handler for the interrupt source selected by INTSEL.

26.6.15 RTC Valid Entry Register

Name: RTC_VER

Address: 0xF80480DC

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	NVCALALR	NVTIMALR	NVCAL	NVTIM

If the RTC is configured in UTC mode, the values returned by this register are not relevant.

NVTIM: Non-valid Time

0: No invalid data has been detected in RTC_TIMR (Time Register).

1: RTC_TIMR has contained invalid data since it was last programmed.

NVCAL: Non-valid Calendar

0: No invalid data has been detected in RTC_CALR (Calendar Register).

1: RTC_CALR has contained invalid data since it was last programmed.

NVTIMALR: Non-valid Time Alarm

0: No invalid data has been detected in RTC_TIMALR (Time Alarm Register).

1: RTC_TIMALR has contained invalid data since it was last programmed.

NVCALALR: Non-valid Calendar Alarm

0: No invalid data has been detected in RTC_CALALR (Calendar Alarm Register).

1: RTC_CALALR has contained invalid data since it was last programmed.

33.22.3 PMC System Clock Status Register

Name: PMC_SCSR

Address: 0xF0014008

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	ISCCK	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	PCK2	PCK1	PCK0
7	6	5	4	3	2	1	0
UDP	UHP	–	–	LCDCK	DDRCK	–	PCK

PCK: Processor Clock Status

0: The Processor clock is disabled.

1: The Processor clock is enabled.

DDRCK: DDR Clock Status

0: The DDR clock is disabled.

1: The DDR clock is enabled.

LCDCK: MCK2x Clock Status

0: The MCK2x clock is disabled.

1: The MCK2x clock is enabled.

Note: MCK2x is selected as LCD Pixel source clock if LCDC_LCDCFG0.CLKSEL = 1.

UHP: USB Host Port Clock Status

0: The UHP48M and UHP12M OHCI clocks are disabled.

1: The UHP48M and UHP12M OHCI clocks are enabled.

UDP: USB Device Port Clock Status

0: The USB Device clock is disabled.

1: The USB Device clock is enabled.

PCKx: Programmable Clock x Output Status

0: The corresponding Programmable Clock output is disabled.

1: The corresponding Programmable Clock output is enabled.

ISCCK: ISC Clock Status

0: The ISC clock is disabled.

1: The ISC clock is enabled.

37.16 Register Write Protection

To prevent any single software error that may corrupt SMC behavior, selected registers can be write-protected by setting the WPEN bit in the Write Protection Mode Register (HSMC_WPMR).

If a write access in a write-protected register is detected, then the WPVS flag in the Write Protection Status Register (HSMC_WPSR) is set and the field WPVSRC indicates in which register the write access has been attempted.

The WPVS flag is automatically reset after reading the HSMC_WPSR.

The following registers can be write-protected:

- Setup Register
- Pulse Register
- Cycle Register
- Timings Register
- Mode Register

37.17 NFC Operations

37.17.1 NFC Overview

The NFC handles all the command, address and data sequences of the NAND low level protocol. An SRAM is used as an internal read/write buffer when data is transferred from or to the NAND.

37.17.2 NFC Control Registers

NAND Flash Read and NAND Flash Program operations can be performed through the NFC Command Registers. In order to minimize CPU intervention and latency, commands are posted in a command buffer. This buffer provides zero wait state latency. The detailed description of the command encoding scheme is explained below.

The NFC handles an automatic transfer between the external NAND Flash and the chip via the NFC SRAM. It is done via NFC Command Registers.

The NFC Command Registers are very efficient to use. When writing to these registers:

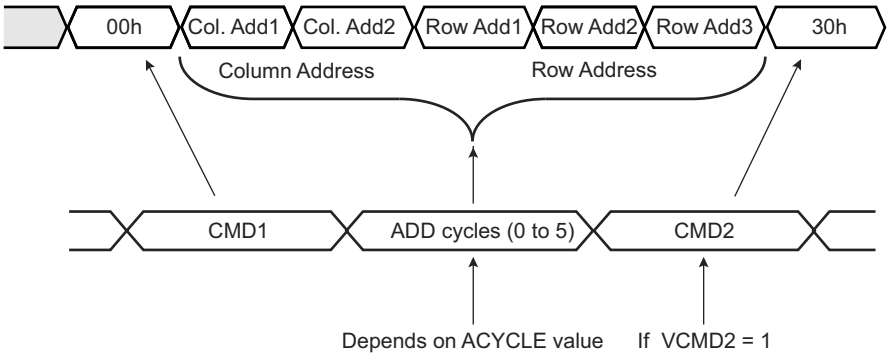
- the address of the register (NFCADDR_CMD) is the command used
- the data of the register (NFCDATA_ADDT) is the address to be sent to the NAND Flash

So, in one single access the command is sent and immediately executed by the NFC. Two commands can even be programmed within a single access (CMD1, CMD2) depending on the VCMD2 value.

The NFC can send up to five address cycles.

Figure 37-31 shows a typical NAND Flash Page Read Command of a NAND Flash Memory and correspondence with NFC Address Command Register.

Figure 37-31: NFC/NAND Flash Access Example



For more details refer to Section 37.17.2.2 “NFC Address Command”.

Reading the NFC Command Register (to any address) will give the status of the NFC. This is especially useful to know if the NFC is busy, for example.

Table 38-3: DMA Channels Definition (XDMAC1) (Continued)

Instance Name	Channel T/R	Interface Number	XDMAC_CCx.CSIZE Required Value
UART0	Transmit	35	0
UART0	Receive	36	
UART1	Transmit	37	0
UART1	Receive	38	
UART2	Transmit	39	0
UART2	Receive	40	
UART3	Transmit	41	0
UART3	Receive	42	
UART4	Transmit	43	0
UART4	Receive	44	
TC0	Receive	45	0
TC1	Receive	46	
CLASSD	Transmit	47	0
QSPI1	Transmit	48	0
QSPI1	Receive	49	
PDMIC	Receive	50	0

6. Program XDMAC_CCx register (see single block transfer configuration).
7. Program XDMAC_CBCx.BLEN with the number of microblocks of data.
8. Clear the following four registers:
   - XDMAC_CNDCx
   - XDMAC_CDS_MSPx
   - XDMAC_CSUSx
   - XDMAC_CDUSx

   This indicates that the linked list is disabled and striding is disabled.
9. Enable the Block interrupt by writing a ‘1’ to XDMAC_CIEx.BIE, enable the Channel x Interrupt Enable bit by writing a ‘1’ to XDMAC_GIEx.IEx.
10. Enable channel x by writing a ‘1’ to the XDMAC_GE.ENx. XDMAC_GS.STx is set by hardware.
11. Once completed, the DMA channel sets XDMAC_CISx.BIS (End of Block Interrupt Status bit) and generates an interrupt. XDMAC_GS.STx is cleared by hardware. The software can either wait for an interrupt or poll the channel status bit.

38.5.4.3 Master Transfer

1. Read the XDMAC_GS register to choose a free channel.
2. Clear the pending Interrupt Status bit by reading the chosen XDMAC_CISx register.
3. Build a linked list of transfer descriptors in memory. The descriptor view is programmable on a per descriptor basis. The linked list items structure must be word aligned. MBR_UBC.NDE must be configured to 0 in the last descriptor to terminate the list.
4. Configure field NDA in the XDMAC Channel x Next Descriptor Address Register (XDMAC_CNDAx) with the first descriptor address and bit XDMAC_CNDAx.NDAIF with the master interface identifier.
5. Configure the XDMAC_CNDCx register:
   a) Set XDMAC_CNDCx.NDE to enable the descriptor fetch.
   b) Set XDMAC_CNDCx.NDSUP to update the source address at the descriptor fetch time, otherwise clear this bit.
   c) Set XDMAC_CNDCx.NDDUP to update the destination address at the descriptor fetch time, otherwise clear this bit.
   d) Configure XDMAC_CNDCx.NDVIEW to define the length of the first descriptor.
6. Enable the End of Linked List interrupt by writing a ‘1’ to XDMAC_CIEx.LIE.
7. Enable channel x by writing a ‘1’ to XDMAC_GE.ENx. XDMAC_GS.STx is set by hardware.
8. Once completed, the DMA channel sets XDMAC_CISx.BIS (End of Block Interrupt Status bit) and generates an interrupt. XDMAC_GS.STx is cleared by hardware. The software can either wait for an interrupt or poll the channel status bit.

38.5.4.4 Disabling A Channel Before Transfer Completion

Under normal operation, the software enables a channel by writing a ‘1’ to XDMAC_GE.ENx, then the hardware disables a channel on transfer completion by clearing bit XDMAC_GS.STx. To disable a channel, write a ‘1’ to bit XDMAC_GD.DIx and poll the XDMAC_GS register.

41.7.12 UDPHS Endpoint Control Disable Register (Isochronous Endpoint)

Name: UDPHS_EPTCTLDISx [x=0..15] (ISOENDPT)

Address: 0xFC02C108 [0], 0xFC02C128 [1], 0xFC02C148 [2], 0xFC02C168 [3], 0xFC02C188 [4], 0xFC02C1A8 [5], 0xFC02C1C8 [6], 0xFC02C1E8 [7], 0xFC02C208 [8], 0xFC02C228 [9], 0xFC02C248 [10], 0xFC02C268 [11], 0xFC02C288 [12], 0xFC02C2A8 [13], 0xFC02C2C8 [14], 0xFC02C2E8 [15]

Access: Write-only

31	30	29	28	27	26	25	24
SHRT_PCKT	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	BUSY_BANK	–	–
15	14	13	12	11	10	9	8
–	ERR_FLUSH	ERR_CRC_NTR	ERR_FL_ISO	TXRDY_TRER	TX_COMPLT	RXRDY_TXKL	ERR_OVFLW
7	6	5	4	3	2	1	0
MDATA_RX	DATAX_RX	–	–	INTDIS_DMA	–	AUTO_VALID	EPT_DISABL

This register view is relevant only if EPT_TYPE = 0x1 in “UDPHS Endpoint Configuration Register” .

For additional information, refer to “UDPHS Endpoint Control Register (Isochronous Endpoint)” .

EPT_DISABL: Endpoint Disable

0: No effect.

1: Disable endpoint.

AUTO_VALID: Packet Auto-Valid Disable

0: No effect.

1: Disable this bit to not automatically validate the current packet.

INTDIS_DMA: Interrupts Disable DMA

0: No effect.

1: Disable the “Interrupts Disable DMA”.

DATAX_RX: DATAx Interrupt Disable (Only for High Bandwidth Isochronous OUT endpoints)

0: No effect.

1: Disable DATAx Interrupt.

MDATA_RX: MDATA Interrupt Disable (Only for High Bandwidth Isochronous OUT endpoints)

0: No effect.

1: Disable MDATA Interrupt.

ERR_OVFLW: Overflow Error Interrupt Disable

0: No effect.

1: Disable Overflow Error Interrupt.

41.7.19 UDPHS Endpoint Status Register (Control, Bulk, Interrupt Endpoints)

Name: UDPHS_EPTSTAx [x=0..15]

Address: 0xFC02C11C [0], 0xFC02C13C [1], 0xFC02C15C [2], 0xFC02C17C [3], 0xFC02C19C [4], 0xFC02C1BC [5], 0xFC02C1DC [6], 0xFC02C1FC [7], 0xFC02C21C [8], 0xFC02C23C [9], 0xFC02C25C [10], 0xFC02C27C [11], 0xFC02C29C [12], 0xFC02C2BC [13], 0xFC02C2DC [14], 0xFC02C2FC [15]

Access: Read-only

31	30	29	28	27	26	25	24
SHRT_PCKT	BYTE_COUNT						

23	22	21	20	19	18	17	16
BYTE_COUNT				BUSY_BANK_STA		CURBK_CTLDIR	

15	14	13	12	11	10	9	8
NAK_OUT	NAK_IN	STALL_SNT	RX_SETUP	TXRDY	TX_COMPLT	RXRDY_TXKL	ERR_OVFLW

7	6	5	4	3	2	1	0
TOGGLESQ_STA		FRCESTALL	–	–	–	–	–

This register view is relevant only if EPT_TYPE = 0x0, 0x2 or 0x3 in “UDPHS Endpoint Configuration Register” .

FRCESTALL: Stall Handshake Request (cleared upon USB reset)

0: No effect.

1: If set a STALL answer will be done to the host for the next handshake.

This bit is reset by hardware upon received SETUP.

TOGGLESQ_STA: Toggle Sequencing (cleared upon USB reset)

Toggle Sequencing:

- **IN endpoint:** It indicates the PID Data Toggle that will be used for the next packet sent. This is not relative to the current bank.
- CONTROL and OUT endpoint:

These bits are set by hardware to indicate the PID data of the current bank:

Value	Name	Description
0	DATA0	DATA0
1	DATA1	DATA1
2	DATA2	Reserved for High Bandwidth Isochronous Endpoint
3	MDATA	Reserved for High Bandwidth Isochronous Endpoint

Note 1: In OUT transfer, the Toggle information is meaningful only when the current bank is busy (Received OUT Data = 1).

2: These bits are updated for OUT transfer:
- A new data has been written into the current bank.
- The user has just cleared the Received OUT Data bit to switch to the next bank.

3: This field is reset to DATA1 by the UDPHS_EPTCLRSTAx register TOGGLESQ bit, and by UDPHS_EPTCTLDISx (disable endpoint).

This bit is 0 whenever the Run/Stop bit is 1. The Host Controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (e.g. internal error).

RCM: Reclamation (read-only)

0: Default.

This is a read-only status bit used to detect any empty asynchronous schedule.

PSS: Periodic Schedule Status (read-only)

0: Default.

The bit reports the current real status of the Periodic Schedule. If this bit is set to 0, then the status of the Periodic Schedule is disabled. If this bit is set to 1, then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the UHPHS_USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).

ASS: Asynchronous Schedule Status (read-only)

0: Default.

The bit reports the current real status of the Asynchronous Schedule. If this bit is set to 0, then the status of the Asynchronous Schedule is disabled. If this bit is set to 1, then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the UHPHS_USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).

The Receive FIFO threshold can be set using the RXFTHRES field in TWIHS_FMR. Each time the Receive FIFO goes from the ‘below threshold’ to the ‘equal or above threshold’ state, the RXFTHF flag in TWIHS_FSR is set. This enables the application to know that the Receive FIFO reached the defined threshold and to read some data before it becomes full.

The TXFTHF and RXFTHF flags can be both configured to generate an interrupt using TWIHS_FIER and TWIHS_FIDR.

- FIFO Flags

FIFOs come with a set of flags which can be configured each to generate an interrupt through TWIHS_FIER and TWIHS_FIDR.

FIFO flags state can be read in TWIHS_FSR. They are cleared on TWIHS_FSR read.

46.6.6 TWIHS Comparison Function on Received Character

The comparison function differs if asynchronous partial wakeup (SleepWalking) is enabled or not.

If asynchronous partial wakeup is disabled (see the section “Power Management Controller (PMC)”), the TWIHS can extend the address matching on up to three slave addresses. The SADR1EN, SADR2EN and SADR3EN bits in TWIHS_SMR enable address matching on additional addresses which can be configured through SADR1, SADR2 and SADR3 fields in the TWIHS_SWMR. The DATAMEN bit in the TWIHS_SMR has no effect.

The SVACC bit is set when there is a comparison match with the received slave address.

NACK used in Slave Read mode:

0: Each data byte has been correctly received by the master.

1: In Read mode, a data byte has not been acknowledged by the master. When NACK is set, the user must not fill TWIHS_THR even if TXRDY is set, because it means that the master stops the data transfer or re-initiate it.

Note: in Slave Write mode, all data are acknowledged by the TWIHS.

ARBLST: Arbitration Lost (cleared on read)

This bit is used in Master mode only.

0: Arbitration won.

1: Arbitration lost. Another master of the TWIHS bus has won the multimaster arbitration. TXCOMP is set at the same time.

SCLWS: Clock Wait State

This bit is used in Slave mode only.

0: The clock is not stretched.

1: The clock is stretched. TWIHS_THR / TWIHS_RHR buffer is not filled / emptied before the transmission / reception of a new character.

SCLWS behavior can be seen in Figure 46-39 and Figure 46-40.

EOSACC: End Of Slave Access (cleared on read)

This bit is used in Slave mode only.

0: A slave access is being performing.

1: The Slave Access is finished. End Of Slave Access is automatically set as soon as SVACC is reset.

EOSACC behavior can be seen in Figure 46-41 and Figure 46-42.

MCACK: Master Code Acknowledge (cleared on read)

MACK used in Slave mode:

0: No Master Code has been received since the last read of TWIHS_SR.

1: A Master Code has been received since the last read of TWIHS_SR.

TOUT: Timeout Error (cleared on read)

0: No SMBus timeout occurred since the last read of TWIHS_SR.

1: An SMBus timeout occurred since the last read of TWIHS_SR.

PECERR: PEC Error (cleared on read)

0: No SMBus PEC error occurred since the last read of TWIHS_SR.

1: An SMBus PEC error occurred since the last read of TWIHS_SR.

SMBDAM: SMBus Default Address Match (cleared on read)

0: No SMBus Default Address received since the last read of TWIHS_SR.

1: An SMBus Default Address was received since the last read of TWIHS_SR.

SMBHHM: SMBus Host Header Address Match (cleared on read)

0: No SMBus Host Header Address received since the last read of TWIHS_SR.

1: An SMBus Host Header Address was received since the last read of TWIHS_SR.

LOCK: TWIHS Lock due to Frame Errors (cleared by writing a one to bit LOCKCLR in TWIHS_CR)

0: The TWIHS is not locked or LOCKCLR command issued in TWIHS_CR.

1: The TWIHS is locked due to frame errors (see Section 46.6.3.13 “Handling Errors in Alternative Command”).

SCL: SCL Line Value

0: SCL line sampled value is ‘0’.

1: SCL line sampled value is ‘1.’

52.6.5 ISC Parallel Front End Configuration 1 Register

Name: ISC_PFE_CFG1

Address: 0xF0008010

Access: Read/Write

31	30	29	28	27	26	25	24
COLMAX							

23	22	21	20	19	18	17	16
COLMAX							

15	14	13	12	11	10	9	8
COLMIN							

7	6	5	4	3	2	1	0
COLMIN							

COLMIN: Column Minimum Limit

Horizontal starting position of the cropping area

COLMAX: Column Maximum Limit

Horizontal ending position of the cropping area

To leave Power-down mode, the application has to turn on the MCAN clocks before clearing CC Control Register flag MCAN_CCCR.CSR. The MCAN will acknowledge this by clearing MCAN_CCCR.CSA. The application can then restart CAN communication by clearing the bit CCCR.INIT.

53.5.1.9 Test Modes

To enable write access to the MCAN Test register (MCAN_TEST) (see Section 53.6.5), bit MCAN_CCCR.TEST must be set. This allows the configuration of the test modes and test functions.

Four output functions are available for the CAN transmit pin CANTX by programming MCAN_TEST.TX. Additionally to its default function – the serial data output – it can drive the CAN Sample Point signal to monitor the MCAN's bit timing and it can drive constant dominant or recessive values. The actual value at pin CANRX can be read from MCAN_TEST.RX. Both functions can be used to check the CAN bus' physical layer.

Due to the synchronization mechanism between CAN clock and system bus clock domain, there may be a delay of several system bus clock periods between writing to MCAN_TEST.TX until the new configuration is visible at output pin CANTX. This applies also when reading input pin CANRX via MCAN_TEST.RX.

Note: Test modes should be used for production tests or self-test only. The software control for pin CANTX interferes with all CAN protocol functions. It is not recommended to use test modes for application.

- External Loop Back Mode

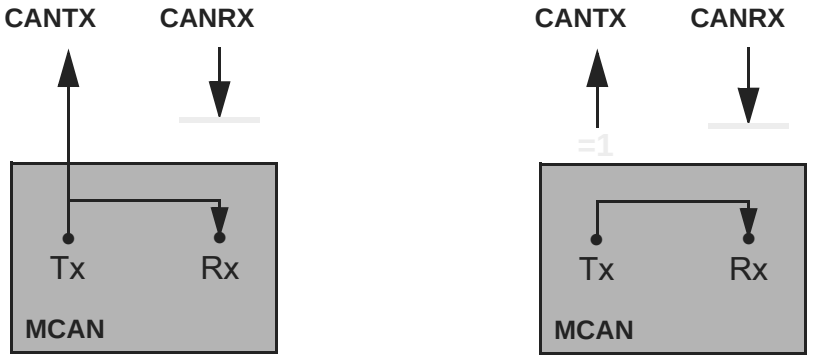
The MCAN can be set in External Loop Back mode by setting the bit MCAN_TEST.LBCK. In Loop Back mode, the MCAN treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into an Rx Buffer or an Rx FIFO. Figure 53-4 shows the connection of signals CANTX and CANRX to the MCAN in External Loop Back mode.

This mode is provided for hardware self-test. To be independent from external stimulation, the MCAN ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop Back mode. In this mode, the MCAN performs an internal feedback from its Tx output to its Rx input. The actual value of the CANRX input pin is disregarded by the MCAN. The transmitted messages can be monitored at the CANTX pin.

- Internal Loop Back Mode

Internal Loop Back mode is entered by setting bits MCAN_TEST.LBCK and MCAN_CCCR.MON. This mode can be used for a "Hot Self-test", meaning the MCAN can be tested without affecting a running CAN system connected to the pins CANTX and CANRX. In this mode, pin CANRX is disconnected from the MCAN, and pin CANTX is held recessive. Figure 53-4 shows the connection of CANTX and CANRX to the MCAN when Internal Loop Back mode is enabled.

Figure 53-4: Pin Control in Loop Back Modes



External Loop Back Mode **Internal Loop Back Mode**

53.5.2 Timestamp Generation

For timestamp generation the MCAN supplies a 16-bit wrap-around counter. A prescaler TSCC.TCP can be configured to clock the counter in multiples of CAN bit times (1…16). The counter is readable via MCAN_TSCV.TSC. A write access to the Timestamp Counter Value register (MCAN_TSCV) resets the counter to zero. When the timestamp counter wraps around, interrupt flag MCAN_IR.TSW is set.

On start of frame reception / transmission the counter value is captured and stored into the timestamp section of an Rx Buffer / Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element.

By programming bit MCAN_TSCC.TSS an external 16-bit timestamp can be used.

54.7.11 TC Interrupt Enable Register

Name: TC_IERx [x=0..2]

Address: 0xF800C024 (0)[0], 0xF800C064 (0)[1], 0xF800C0A4 (0)[2], 0xF8010024 (1)[0], 0xF8010064 (1)[1], 0xF80100A4 (1)[2]

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

COVFS: Counter Overflow

LOVRS: Load Overrun

CPAS: RA Compare

CPBS: RB Compare

CPCS: RC Compare

LDRAS: RA Loading

LDRBS: RB Loading

ETRGS: External Trigger

54.7.19 TC QDEC Interrupt Mask Register

Name: TC_QIMR

Address: 0xF800C0D0 (0), 0xF80100D0 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	MPE	QERR	DIRCHG	IDX

IDX: Index

0: The interrupt on IDX input is disabled.

1: The interrupt on IDX input is enabled.

DIRCHG: Direction Change

0: The interrupt on rotation direction change is disabled.

1: The interrupt on rotation direction change is enabled.

QERR: Quadrature Error

0: The interrupt on quadrature error is disabled.

1: The interrupt on quadrature error is enabled.

MPE: Consecutive Missing Pulse Error

0: The interrupt on the maximum number of consecutive missing pulses specified in MAXCMP is disabled.

1: The interrupt on the maximum number of consecutive missing pulses specified in MAXCMP is enabled.

56.7.3 PWM Disable Register

Name: PWM_DIS

Address: 0xF802C008

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

This register can only be written if bits WPSWS1 and WPHWS1 are cleared in the PWM Write Protection Status Register.

CHIDx: Channel ID

0: No effect.

1: Disable PWM output for channel x.

57.5.5 SFC Interrupt Mask Register

Name: SFC_IMR

Address: 0xF804C018

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	ACE	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	LCHECK	–	–	PGMF	PGMC

The following configuration values are valid for all listed bit names of this register:

0: Corresponding interrupt is not enabled.

1: Corresponding interrupt is enabled.

PGMC: Programming Sequence Completed Interrupt Mask

PGMF: Programming Sequence Failed Interrupt Mask

LCHECK: Live Integrity Checking Error Interrupt Mask

ACE: Area Check Error Interrupt Mask

59.4 Advanced Encryption Standard Bridge (AESB) User Interface

Table 59-3: Register Mapping

Offset	Register	Name	Access	Reset
0x00	Control Register	AESB_CR	Write-only	–
0x04	Mode Register	AESB_MR	Read/Write	0x0
0x08–0x0C	Reserved	–	–	–
0x10	Interrupt Enable Register	AESB_IER	Write-only	–
0x14	Interrupt Disable Register	AESB_IDR	Write-only	–
0x18	Interrupt Mask Register	AESB_IMR	Read-only	0x0
0x1C	Interrupt Status Register	AESB_ISR	Read-only	0x0
0x20	Key Word Register 0	AESB_KEYWR0	Write-only	–
0x24	Key Word Register 1	AESB_KEYWR1	Write-only	–
0x28	Key Word Register 2	AESB_KEYWR2	Write-only	–
0x2C	Key Word Register 3	AESB_KEYWR3	Write-only	–
0x30–0x3C	Reserved	–	–	–
0x40	Input Data Register 0	AESB_IDATAR0	Write-only	–
0x44	Input Data Register 1	AESB_IDATAR1	Write-only	–
0x48	Input Data Register 2	AESB_IDATAR2	Write-only	–
0x4C	Input Data Register 3	AESB_IDATAR3	Write-only	–
0x50	Output Data Register 0	AESB_ODATAR0	Read-only	0x0
0x54	Output Data Register 1	AESB_ODATAR1	Read-only	0x0
0x58	Output Data Register 2	AESB_ODATAR2	Read-only	0x0
0x5C	Output Data Register 3	AESB_ODATAR3	Read-only	0x0
0x60	Initialization Vector Register 0	AESB_IVR0	Write-only	–
0x64	Initialization Vector Register 1	AESB_IVR1	Write-only	–
0x68	Initialization Vector Register 2	AESB_IVR2	Write-only	–
0x6C	Initialization Vector Register 3	AESB_IVR3	Write-only	–
0x70-0xB0	Reserved	–	–	–
0xB4-0xE8	Reserved	–	–	–
0xEC–0xFC	Reserved	–	–	–

Table 72-6: SAMA5D2 Datasheet Rev. 11267B Revision History (Continued)

Issue Date	Changes
13-Nov-15	Section 39. “Audio Class D Amplifier (CLASSD)” Updated Figure 39-1. CLASSD Block Diagram
	Section 41. “Inter-IC Sound Controller (I2SC)” Replaced all instances of “PCKx” with “GCLK” Removed all references to Time Division Multiplexed (TDM) format (not supported) Section 41.1 “Description”: replaced “The I2SC can use either a single DMA Controller channel for both audio channels or one DMA Controller channel per audio channel.” with “The I2SC uses a single DMA Controller channel for both audio channels.”, and updated Section 41.2 “Embedded Characteristics” and Section 41.6.8 “DMA Controller Operation” accordingly Section 41.8.2 “Inter-IC Sound Controller Mode Register”: removed fields RXDMA and TXDMA
	Section 44. “Flexible Serial Communication Controller (FLEXCOM)” Added SPI mode in UART/USART Replaced all instances of ‘PCK’ with ‘GCLK’ Replaced all instances of ‘DMAC/PDC’ with ‘DMAC’ Removed SleepWalking characteristic from UART/USART mode Removed all references to ISO7816 specification Section 44.10.6 “USART Mode Register”updated USCLKS field description Section 44.10.44 “SPI Mode Register”: updated BRSRCCLK and DLYBCS field descriptions Section 44.10.54 “SPI Chip Select Register”: updated CSNAAT, SCBR, DLYBS and DLYBCT field descriptions Section 44.10.64 “TWI Clock Waveform Generator Register”: updated BRSRCCLK and CKSRC field descriptions Updated Figure 44-1 “FLEXCOM Block Diagram” and Figure 44-67 “Master Mode Block Diagram”
	Section 42. “Two-wire Interface (TWIHS)” Replaced all instances of “PMC_PCK” with “GCLK”
	Section 55. “Universal Asynchronous Receiver Transmitter (UART)” Replaced "Processor-Independent Source Clock" with "Processor-Independent Generic Source Clock" and "PCK" with "GCLK"
	Section 48. “Secure Digital Multimedia Card Controller (SDMMC)” Updated revision of supported e.MMC specification (from V4.41 to V4.51)
	Section 51. “Pulse Density Modulation Interface Controller (PDMIC)” Removed all references to PDC Removed Section 1.6.4 “Buffer Structure”
	Section 54. “Secure Fuse Controller (SFC)” Removed all references to lock fuse (not supported) Section 54.4.5.3 “Fuse Masking”: corrected data register names Section 54.5.2 “SFC Mode Register”: updated MSK field description Table 54-1 “Register Mapping”: modified SFC_IER and SFC_IDR access type from “Read/Write” to “Write-only”
	Section 57. “Advanced Encryption Standard (AES)” Updated Figure 57-12 “Generation of an ESP IPSec Frame without ESN” and Figure 57-13 “Generation of an ESP IPSec Frame with ESN”
	Added Section 61. “Security Module”