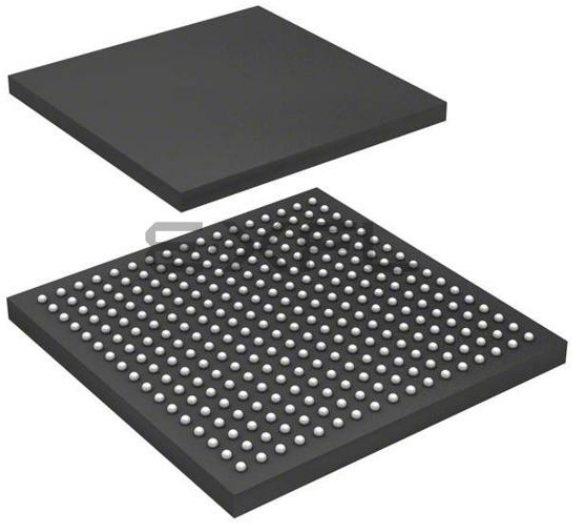

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d28a-cn

14.5.13 L2CC Masked Interrupt Status Register

Name: L2CC_MISR

Address: 0x00A00218

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	DECERR

7	6	5	4	3	2	1	0
SLVERR	ERRRD	ERRRT	ERRWD	ERRWT	PARRD	PARRT	ECNTR

ECNTR: Event Counter 1/0 Overflow Increment

PARRT: Parity Error on L2 Tag RAM, Read

PARRD: Parity Error on L2 Data RAM, Read

ERRWT: Error on L2 Tag RAM, Write

ERRWD: Error on L2 Data RAM, Write

ERRRT: Error on L2 Tag RAM, Read

ERRRD: Error on L2 Data RAM, Read

SLVERR: SLVERR from L3 memory

DECERR: DECERR from L3 memory

0: No interrupt has been generated or the interrupt is masked.

1: The input lines have triggered an interrupt.

25.5.2 PIT Status Register

Name: PIT_SR

Address: 0xF8048034

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	PITS

PITS: Periodic Interval Timer Status

0: The Periodic Interval timer has not reached PIV since the last read of PIT_PIVR.

1: The Periodic Interval timer has reached PIV since the last read of PIT_PIVR.

26.6.5 RTC Calendar Register

Name: RTC_CALR

Address: 0xF80480BC

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	DATE					

23	22	21	20	19	18	17	16
DAY			MONTH				

15	14	13	12	11	10	9	8
YEAR							

7	6	5	4	3	2	1	0
–	CENT						

Note: In UTC mode, values read in this register are not relevant

CENT: Current Century

The range that can be set is 19–20 (Gregorian) or 13–14 (Persian) (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

YEAR: Current Year

The range that can be set is 00–99 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

MONTH: Current Month

The range that can be set is 01–12 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

DAY: Current Day in Current Week

The range that can be set is 1–7 (BCD).

The coding of the number (which number represents which day) is user-defined as it has no effect on the date counter.

DATE: Current Day in Current Month

The range that can be set is 01–31 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

31.6 Functional Description

31.6.1 Description

The analog comparator is enabled by writing a one to the ACEN bit in the ACC Mode Register (ACC_MR) and the polarity of the comparator output can be configured with bit ACC_MR.INV.

The ACC registers are listed in Table 31-2.

31.6.2 Register Write Protection

To prevent any single software error from corrupting ACC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the ACC Write Protection Mode Register (ACC_WPMR).

If a write access to a write-protected register is detected, the WPVS flag in the ACC Write Protection Status Register (ACC_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the ACC_WPSR register.

The following registers can be write-protected:

- ACC Mode Register

33.22.39 PMC Audio PLL Control Register 0

Name: PMC_AUDIO_PLL0

Address: 0xF001414C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	DCO_GAIN		DCO_FILTER			

23	22	21	20	19	18	17	16
–	QDPMC						

15	14	13	12	11	10	9	8
–	ND						

7	6	5	4	3	2	1	0
PLLFLT				RESETN	PMCEN	PADEN	PLLEN

PLLEN: PLL Enable

0: The Audio PLL is disabled.

1: The Audio PLL is enabled

PADEN: Pad Clock Enable

0: The external audio pin CLK_AUDIO is driven low.

1: The external audio pin CLK_AUDIO is driven by AUDIOPINCLK.

PMCEN: PMC Clock Enable

0: The output clock of the audio PLL is not sent to the PMC.

1: The output clock of the audio PLL is sent to the PMC.

RESETN: Audio PLL Reset

0: The audio PLL is in reset state.

1: The audio PLL is in active state.

PLLFLT: PLL Loop Filter Selection

Default value should be 13 (0xD)

ND: Loop Divider Ratio

QDPMC: Output Divider Ratio for PMC Clock

$f_{pmc} = f_{ref} \times ((ND + 1) + FRACR \div 2^{22}) / (QDPMC + 1)$

DCO_FILTER: Digitally Controlled Oscillator Filter Selection

For optimization, the value of this field must be configured to 0.

DCO_GAIN: Digitally Controlled Oscillator Gain Selection

For optimization, the value of this field must be configured to 0.

Table 39-55: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x00000290	Overlay 2 Configuration Register 9	LCDC_OVR2CFG9	Read/ Write	0x00000000
0x00000294–0x0000033C	Reserved	–	–	–
0x00000340	High-End Overlay Channel Enable Register	LCDC_HEOCHER	Write-only	–
0x00000344	High-End Overlay Channel Disable Register	LCDC_HEOCHDR	Write-only	–
0x00000348	High-End Overlay Channel Status Register	LCDC_HEOCHSR	Read-only	0x00000000
0x0000034C	High-End Overlay Interrupt Enable Register	LCDC_HEOIER	Write-only	–
0x00000350	High-End Overlay Interrupt Disable Register	LCDC_HEOIDR	Write-only	–
0x00000354	High-End Overlay Interrupt Mask Register	LCDC_HEOIMR	Read-only	0x00000000
0x00000358	High-End Overlay Interrupt Status Register	LCDC_HEOISR	Read-only	0x00000000
0x0000035C	High-End Overlay DMA Head Register	LCDC_HEOHEAD	Read/ Write	0x00000000
0x00000360	High-End Overlay DMA Address Register	LCDC_HEOADDR	Read/ Write	0x00000000
0x00000364	High-End Overlay DMA Control Register	LCDC_HEOCTRL	Read/ Write	0x00000000
0x00000368	High-End Overlay DMA Next Register	LCDC_HEONEXT	Read/ Write	0x00000000
0x0000036C	High-End Overlay U-UV DMA Head Register	LCDC_HEOUHEAD	Read/ Write	0x00000000
0x00000370	High-End Overlay U-UV DMA Address Register	LCDC_HEOUADDR	Read/ Write	0x00000000
0x00000374	High-End Overlay U-UV DMA Control Register	LCDC_HEOUCTRL	Read/ Write	0x00000000
0x00000378	High-End Overlay U-UV DMA Next Register	LCDC_HEOUNEXT	Read/ Write	0x00000000
0x0000037C	High-End Overlay V DMA Head Register	LCDC_HEOVHEAD	Read/ Write	0x00000000
0x00000380	High-End Overlay V DMA Address Register	LCDC_HEOVADDR	Read/ Write	0x00000000
0x00000384	High-End Overlay V DMA Control Register	LCDC_HEOVCTRL	Read/ Write	0x00000000
0x00000388	High-End Overlay V DMA Next Register	LCDC_HEOVNEXT	Read/ Write	0x00000000
0x0000038C	High-End Overlay Configuration Register 0	LCDC_HEOCFG0	Read/ Write	0x00000000
0x00000390	High-End Overlay Configuration Register 1	LCDC_HEOCFG1	Read/ Write	0x00000000
0x00000394	High-End Overlay Configuration Register 2	LCDC_HEOCFG2	Read/ Write	0x00000000
0x00000398	High-End Overlay Configuration Register 3	LCDC_HEOCFG3	Read/ Write	0x00000000

39.7.133 High-End Overlay Configuration Register 38

Name: LCDC_HEOCFG38

Address: 0xF0000424

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
YPHI5COEFF2							

15	14	13	12	11	10	9	8
YPHI5COEFF1							

7	6	5	4	3	2	1	0
YPHI5COEFF0							

YPHI5COEFF0: Vertical Coefficient for phase 5 tap 0

Coefficient format is 1 sign bit and 7 fractional bits.

YPHI5COEFF1: Vertical Coefficient for phase 5 tap 1

Coefficient format is 1 magnitude bit and 7 fractional bits.

YPHI5COEFF2: Vertical Coefficient for phase 5 tap 2

Coefficient format is 1 sign bit and 7 fractional bits.

Figure 43-7: Treble Filters Response

dB

f_s

43.6.3 De-emphasis Filter Frequency Response

The CLASSD includes a de-emphasis filter which can be enabled for 32, 44.1 or 48 kHz sampling frequencies.

The response and the error generated by the digital approximation of the filter are illustrated in the following figures.

Figure 43-8: De-emphasis Filter: Frequency Response & Error (f_S = 32 kHz)

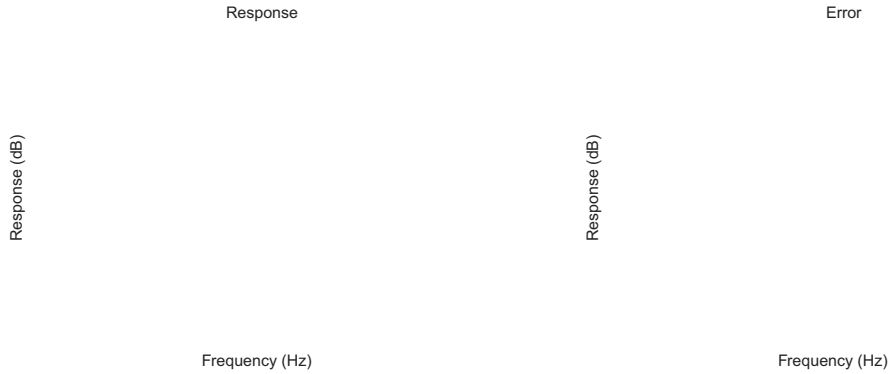


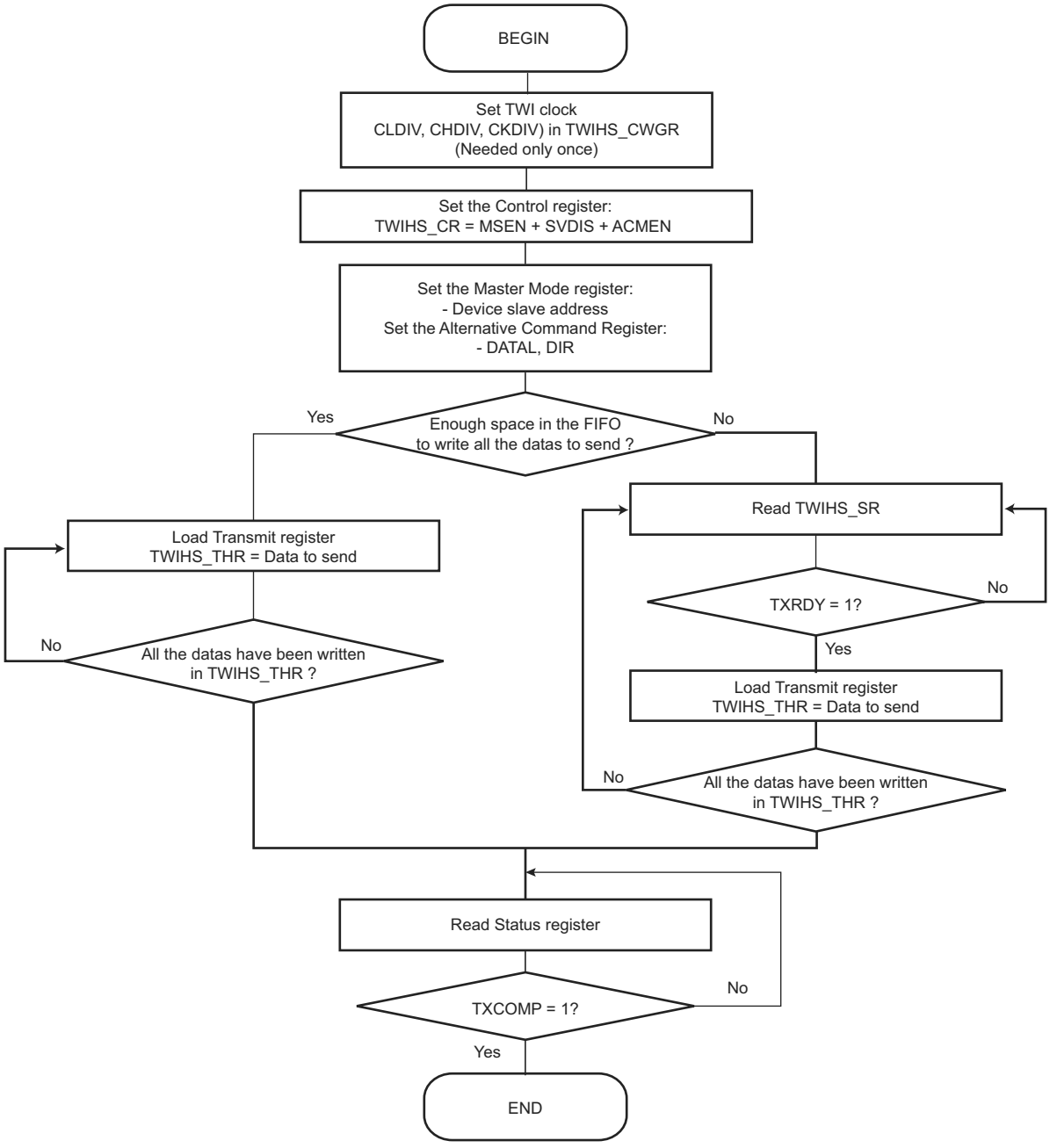
Figure 43-9: De-emphasis Filter: Frequency Response & Error (f_S = 44.1 kHz)

- Sending Data with FIFO Enabled

With the Transmit FIFO enabled, any write access to the TWIHS Transmit Holding Register (TWIHS_THR) brings the written data to the Transmit FIFO. As a consequence, it is not mandatory any more to monitor the TXRDY flag state to send multiple data without DMAC.

Knowing the number of data to send and provided there is enough space in the Transmit FIFO, all the data to send can be written successively in the TWIHS_THR without checking the TXRDY flag between each access. The Transmit FIFO state can be checked reading the TXFL field in the TWIHS FIFO Level Register (TWIHS_FLR).

Figure 46-29: Sending Data with FIFO Flowchart



- Receiving Data with FIFO Enabled

With Receive FIFO enabled, any read access on TWIHS_RHR will pull out a data from the Receive FIFO. As a consequence, it is not mandatory any more to monitor the RXRDY flag when DMAC is not used and there are multiple data to read.

46.7.12 TWIHS Interrupt Enable Register

Name: TWIHS_IER

Address: 0xF8028024 (0), 0xFC028024 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	SMBHHM	SMBDAM	PECERR	TOUT	–	MCACK
15	14	13	12	11	10	9	8
–	–	–	–	EOSACC	SCL_WS	ARBLST	NACK
7	6	5	4	3	2	1	0
UNRE	OVRE	GACC	SVACC	–	TXRDY	RXRDY	TXCOMP

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

TXCOMP: Transmission Completed Interrupt Enable

RXRDY: Receive Holding Register Ready Interrupt Enable

TXRDY: Transmit Holding Register Ready Interrupt Enable

SVACC: Slave Access Interrupt Enable

GACC: General Call Access Interrupt Enable

OVRE: Overrun Error Interrupt Enable

UNRE: Underrun Error Interrupt Enable

NACK: Not Acknowledge Interrupt Enable

ARBLST: Arbitration Lost Interrupt Enable

SCL_WS: Clock Wait State Interrupt Enable

EOSACC: End Of Slave Access Interrupt Enable

MCACK: Master Code Acknowledge Interrupt Enable

TOUT: Timeout Error Interrupt Enable

PECERR: PEC Error Interrupt Enable

SMBDAM: SMBus Default Address Match Interrupt Enable

SMBHHM: SMBus Host Header Address Match Interrupt Enable

46.7.13 TWIHS Interrupt Disable Register

Name: TWIHS_IDR

Address: 0xF8028028 (0), 0xFC028028 (1)

47.10.42 USART Write Protection Status Register

Name: FLEX_US_WPSR

Address: 0xF80342E8 (0), 0xF80382E8 (1), 0xFC0102E8 (2), 0xFC0142E8 (3), 0xFC0182E8 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
WPVSRC							

15	14	13	12	11	10	9	8
WPVSRC							

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPVS

WPVS: Write Protection Violation Status

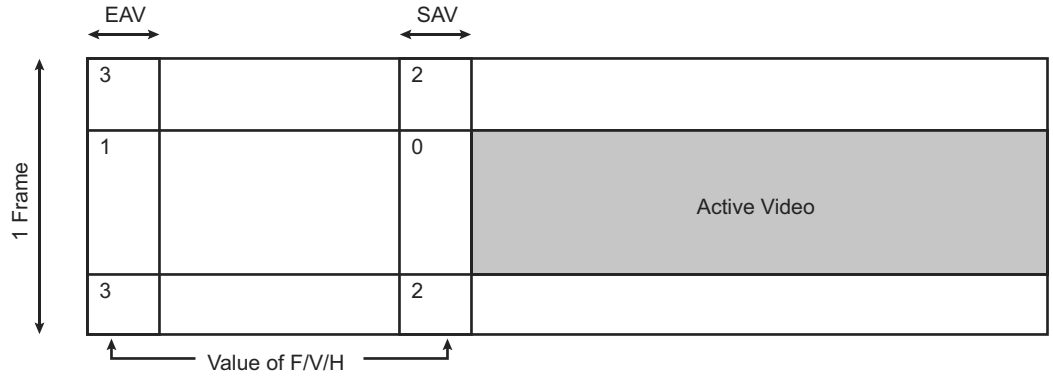
0: No write protection violation has occurred since the last read of FLEX_US_WPSR.

1: A write protection violation has occurred since the last read of FLEX_US_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

WPVSRC: Write Protection Violation Source

When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

Figure 52-13: Frame Timing Relationship for Progressive Systems



52.5.4 Parallel Interface External Sensor Connections

52.5.4.1 YCbCr, 10-bit CCIR656 with Embedded Synchronization

This mode is activated when fields ISC_PFE_CFG0.CCIR656 and ISC_PFE_CFG0.CCIR10_8N are both set.

Interface Bit	First Word	Second Word	Third Word	Fourth Word
isc_data[11](MSB)	1	0	0	1
isc_data[10]	1	0	0	F
isc_data[9]	1	0	0	V
isc_data[8]	1	0	0	H
isc_data[7]	1	0	0	P3
isc_data[6]	1	0	0	P2
isc_data[5]	1	0	0	P1
isc_data[4]	1	0	0	P0
isc_data[3]	1	0	0	0
isc_data[2]	1	0	0	0
isc_data[1]	not used	not used	not used	not used
isc_data[0]	not used	not used	not used	not used

52.5.4.2 YCbCr, 8-bit CCIR656 with Embedded Synchronization

This mode is activated when field ISC_PFE_CFG0.CCIR656 is set and field ISC_PFE_CFG0.CCIR10_8N is cleared.

Interface Bit	First Word	Second Word	Third Word	Fourth Word
isc_data[11](MSB)	1	0	0	1
isc_data[10]	1	0	0	F
isc_data[9]	1	0	0	V
isc_data[8]	1	0	0	H
isc_data[7]	1	0	0	P3
isc_data[6]	1	0	0	P2
isc_data[5]	1	0	0	P1
isc_data[4]	1	0	0	P0

52.6.46 ISC Subsampling 4:4:4 to 4:2:2 Configuration Register

Name: ISC_SUB422_CFG

Address: 0xF00083C8

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	FILTER		–	CCIRMODE		CCIR

CCIR: CCIR656 Input Stream

0: Raw mode

1: CCIR mode

CCIRMODE: CCIR656 Byte Ordering

Value	Name	Description
0	CBY	Byte ordering Cb0, Y0, Cr0, Y1
1	CRY	Byte ordering Cr0, Y0, Cb0, Y1
2	YCB	Byte ordering Y0, Cb0, Y1, Cr0
3	YCR	Byte ordering Y0, Cr0, Y1, Cb0

FILTER: Low Pass Filter Selection

Value	Name	Description
0	FILT0CO	Cosited, {1}
1	FILT1CE	Centered {1, 1}
2	FILT2CO	Cosited {1,2,1}
3	FILT3CE	Centered {1, 3, 3, 1}

52.6.51 ISC DMA Configuration Register

Name: ISC_DCFG

Address: 0xF00083E0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	CMBSIZE	

7	6	5	4	3	2	1	0
–	–	YMBSIZE		–	IMODE		

IMODE: DMA Input Mode Selection

Value	Name	Description
0	PACKED8	8 bits, single channel packed
1	PACKED16	16 bits, single channel packed
2	PACKED32	32 bits, single channel packed
3	YC422SP	32 bits, dual channel
4	YC422P	32 bits, triple channel
5	YC420SP	32 bits, dual channel
6	YC420P	32 bits, triple channel

YMBSIZE: DMA Memory Burst Size Y channel

Value	Name	Description
0	SINGLE	DMA single access
1	BEATS4	4-beat burst access
2	BEATS8	8-beat burst access
3	BEATS16	16-beat burst access

CMBSIZE: DMA Memory Burst Size C channel

Value	Name	Description
0	SINGLE	DMA single access
1	BEATS4	4-beat burst access
2	BEATS8	8-beat burst access
3	BEATS16	16-beat burst access

53.6.47 MCAN Tx Event FIFO Acknowledge

Name: MCAN_TXEFA

Address: 0xF80540F8 (0), 0xFC0500F8 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	EFAI				

EFAI: Event FIFO Acknowledge Index

After the processor has read an element or a sequence of elements from the Tx Event FIFO, it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index MCAN_TXEFS.EFGI to EFAI + 1 and update the FIFO 0 Fill Level MCAN_TXEFS.EFFL.

56.7.14 PWM Interrupt Enable Register 2

Name: PWM_IER2

Address: 0xF802C034

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
CMPU7	CMPU6	CMPU5	CMPU4	CMPU3	CMPU2	CMPU1	CMPU0
15	14	13	12	11	10	9	8
CMPM7	CMPM6	CMPM5	CMPM4	CMPM3	CMPM2	CMPM1	CMPM0
7	6	5	4	3	2	1	0
–	–	–	–	UNRE	–	–	WRDY

WRDY: Write Ready for Synchronous Channels Update Interrupt Enable

UNRE: Synchronous Channels Update Underrun Error Interrupt Enable

CMPMx: Comparison x Match Interrupt Enable

CMPUx: Comparison x Update Interrupt Enable

60.5.10 AES Initialization Vector Register x

Name: AES_IVRx [x=0..3]

Address: 0xF002C060

Access: Write-only

31	30	29	28	27	26	25	24
IV							

23	22	21	20	19	18	17	16
IV							

15	14	13	12	11	10	9	8
IV							

7	6	5	4	3	2	1	0
IV							

IV: Initialization Vector

The four 32-bit Initialization Vector registers set the 128-bit Initialization Vector data block that is used by some modes of operation as an additional initial input.

AES_IVR0 corresponds to the first word of the Initialization Vector, AES_IVR3 to the last one.

These registers are write-only to prevent the Initialization Vector from being read by another application.

For CBC, OFB and CFB modes, the IV input value corresponds to the initialization vector.

For CTR mode, the IV input value corresponds to the initial counter value.

Note: These registers are not used in ECB mode and must not be written.

AUTOBKP: Automatic Backup Mode Enabled (RO)

0: Disabled.

1: Enabled.

SCRAMB: Scrambling Enabled (RO)

0: Disabled.

1: Enabled.

66.22 PDMIC Timings

66.22.1 Timing Conditions

Timings assuming capacitance loads are given in Table 66-86.

Table 66-86: Capacitance Load

Supply	Corner	
	Max	Min
3.3V	30 pF	5 pF
1.8V	20 pF	5 pF

66.22.2 Timing Extraction

Figure 66-39: PDMIC Timing Diagram

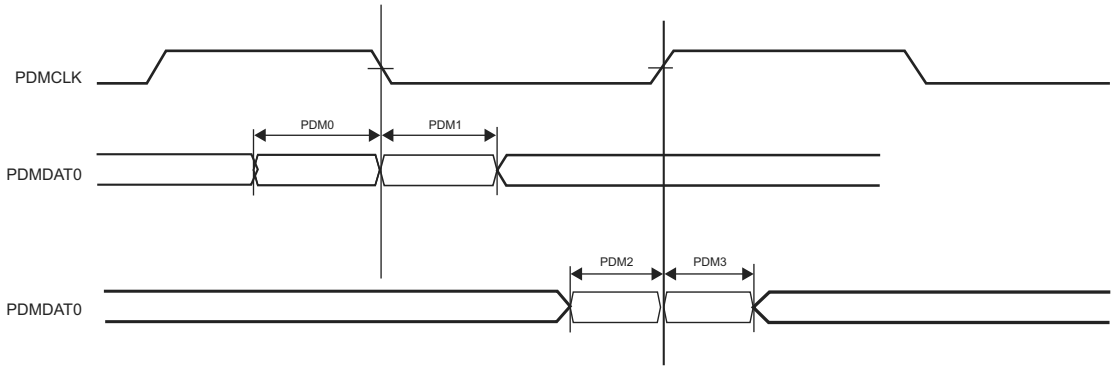


Table 66-87: PDMIC IOSET1 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
$PDMIC_0$	DATA setup time right	3.5	–	3.5	–	ns
$PDMIC_1$	DATA hold time right	3.1	–	3.5	–	ns
$PDMIC_2$	DATA setup time left	3.5	–	3.5	–	ns
$PDMIC_3$	DATA hold time left	3.1	–	3.5	–	ns

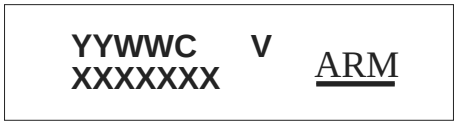
Table 66-88: PDMIC IOSET2 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
$PDMIC_0$	DATA setup time right	4.2	–	4.2	–	ns
$PDMIC_1$	DATA hold time right	2	–	2	–	ns
$PDMIC_2$	DATA setup time left	4.2	–	4.2	–	ns
$PDMIC_3$	DATA hold time left	2	–	2	–	ns

69. Marking

All devices are marked with the company logo and the ordering code.

Additional marking is as follows:



where

- “YY”: Manufactory year
- “WW”: Manufactory week
- “C”: Assembly country code (optional)
- “V”: Revision
- “XXXXXXX”: Lot number