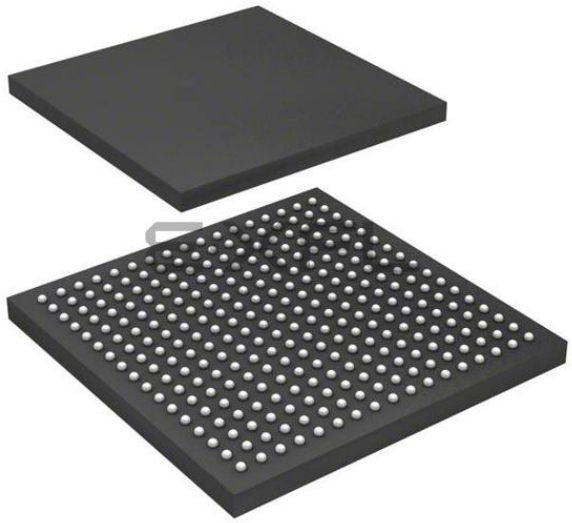

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d28a-cu

19.3.8 UMTI DP/DM Pin Swapping Register

Name: SFR_UTMISWAP

Address: 0xF803003C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	PORT2	PORT1	PORT0

PORTx: PORT x DP/DM Pin Swapping

0 (NORMAL): DP/DM normal pinout.

1 (SWAPPED): DP/DM swapped pinout.

26.6.18 RTC TimeStamp Time Register 1

Name: RTC_TSTR1

Address: 0xF804816C

Access: Read-only

31	30	29	28	27	26	25	24
BACKUP	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	AMPM	HOUR					

15	14	13	12	11	10	9	8
–	MIN						

7	6	5	4	3	2	1	0
–	SEC						

These fields are valid for non-UTC mode only.

RTC_TSTR1 reports the timestamp of the last tamper event.

This register is cleared by reading RTC_TSSR1.

SEC: Seconds of the Tamper

MIN: Minutes of the Tamper

HOUR: Hours of the Tamper

AMPM: AM/PM Indicator of the Tamper

BACKUP: System Mode of the Tamper

0: The state of the system is different from Backup mode when the tamper event occurs.

1: The system is in Backup mode when the tamper event occurs.

33.22.21 PLL Charge Pump Current Register

Name: PMC_PLLICPR

Address: 0xF0014080

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	IVCO_PLLU	

23	22	21	20	19	18	17	16
–	–	–	–	–	–	ICP_PLLU	

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	ICP_PLLA	

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

ICP_PLLA: Charge Pump Current

To optimize clock performance, this field must be programmed as specified in “PLL A Characteristics” in the Electrical Characteristics section.

ICP_PLLU: Charge Pump Current PLL UTMI

Should be written to 0.

IVCO_PLLU: Voltage Control Output Current PLL UTMI

Should be written to 0.

39.7.23 Base DMA Head Register

Name: LCDC_BASEHEAD

Address: 0xF000005C

Access: Read/Write

31	30	29	28	27	26	25	24
HEAD							

23	22	21	20	19	18	17	16
HEAD							

15	14	13	12	11	10	9	8
HEAD							

7	6	5	4	3	2	1	0
HEAD						–	–

HEAD: DMA Head Pointer

The Head Pointer points to a new descriptor.

- If bit 12 is written with a one, the pause quantum will be zero.

After transmission, a pause frame transmitted interrupt will be generated (bit 14 of the Interrupt Status register) and the only the statistics register Pause Frames Transmitted is incremented.

Pause frames can also be transmitted by the MAC using normal frame transmission methods.

40.6.17 MAC PFC Priority-based Pause Frame Support

Note: Refer to the 802.1Qbb standard for a full description of priority-based pause operation.

The following table shows the start of a Priority-based Flow Control (PFC) pause frame.

Table 40-17: Start of a PFC Pause Frame

Address		Type (Mac Control Frame)	Pause Opcode	Priority Enable Vector	Pause Time
Destination	Source				
0x0180C2000001	6 bytes	0x8808	0x1001	2 bytes	8×2 bytes

The GMAC supports PFC priority-based pause transmission and reception. Before PFC pause frames can be received, bit 16 of the Network Control register must be set.

40.6.17.1 PFC Pause Frame Reception

The ability to receive and decode priority-based pause frames is enabled by setting bit 16 of the Network Control register. When this bit is set, the GMAC will match either classic 802.3 pause frames or PFC priority-based pause frames. Once a priority-based pause frame has been received and matched, then from that moment on the GMAC will only match on priority-based pause frames (this is an 802.1Qbb requirement, known as PFC negotiation). Once priority-based pause has been negotiated, any received 802.3x format pause frames will not be acted upon.

If a valid priority-based pause frame is received then the GMAC will decode the frame and determine which, if any, of the eight priorities require to be paused. Up to eight Pause Time registers are then updated with the eight pause times extracted from the frame regardless of whether a previous pause operation is active or not. An interrupt (either bit 12 or bit 13 of the Interrupt Status register) is triggered when a pause frame is received, but only if the interrupt has been enabled (bit 12 and bit 13 of the Interrupt Mask register). Pause frames received with non zero quantum are indicated through the interrupt bit 12 of the Interrupt Status register. Pause frames received with zero quantum are indicated on bit 13 of the Interrupt Status register. The loading of a new pause time only occurs when the GMAC is configured for full duplex operation. If the GMAC is configured for half duplex, the pause time counters will not be loaded, but the pause frame received interrupt will still be triggered. A valid pause frame is defined as having a destination address that matches either the address stored in Specific Address 1 register or if it matches the reserved address of 0x0180C2000001. It must also have the MAC control frame type ID of 0x8808 and have the pause opcode of 0x0101.

Pause frames that have frame check sequence (FCS) or other errors will be treated as invalid and will be discarded. Valid pause frames received will increment the Pause Frames Received Statistic register.

The Pause Time registers decrement every 512 bit times immediately following the PFC frame reception. For test purposes, the retry test bit can be set (bit 12 in the Network Configuration register) which causes the Pause Time register to decrement every GRXCK cycle once transmission has stopped.

The interrupt (bit 13 in the Interrupt Status register) is asserted whenever the Pause Time register decrements to zero (assuming it has been enabled by bit 13 in the Interrupt Mask register). This interrupt is also set when a zero quantum pause frame is received.

40.6.17.2 PFC Pause Frame Transmission

Automatic transmission of pause frames is supported through the transmit priority-based pause frame bit of the Network Control register. If bit 17 of the Network Control register is written with logic 1, a PFC pause frame will be transmitted providing full duplex is selected in the Network Configuration register and the transmit block is enabled in the Network Control register. When bit 17 of the Network Control register is set, the fields of the priority-based pause frame will be built using the values stored in the Transmit PFC Pause register.

Pause frame transmission will happen immediately if transmit is inactive or if transmit is active between the current frame and the next frame due to be transmitted.

Transmitted pause frames comprise the following:

- A destination address of 01-80-C2-00-00-01
- A source address taken from Specific Address 1 register
- A type ID of 88-08 (MAC control frame)
- A pause opcode of 01-01

40.8.21 GMAC Hash Register Top

Name: GMAC_HRT

Address: 0xF8008084

Access: Read-only

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The unicast hash enable (UNIHEN) and the multicast hash enable (MITIHEN) bits in the GMAC Network Configuration Register enable the reception of hash matched frames. See Section 40.6.9 ”Hash Addressing”.

ADDR: Hash Address

Bits 63 to 32 of the Hash Address Register.

40.8.42 GMAC 1588 Timer Second Comparison High Register

Name: GMAC_SCH

Address: 0xF80080E4

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
SEC							

7	6	5	4	3	2	1	0
SEC							

SEC: 1588 Timer Second Comparison Value

Value is compared to the top 16 bits (most significant 16 bits [47:32] of seconds value) of the TSU timer count value.

40.8.69 GMAC Frames Received Register

Name: GMAC_FR

Address: 0xF8008158

Access: Read-only

31	30	29	28	27	26	25	24
FRX							

23	22	21	20	19	18	17	16
FRX							

15	14	13	12	11	10	9	8
FRX							

7	6	5	4	3	2	1	0
FRX							

FRX: Frames Received without Error

Frames received without error. This register counts the number of frames successfully received. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

This bit is set at the end of a microframe in which at least one data bank has been transmitted, if less than the number of transactions per micro-frame banks (UDPHS_EPTCFGx register NB_TRANS) have been validated for transmission inside this microframe.

This bit is reset by UDPHS_EPTRST register EPT_x (reset endpoint) and by UDPHS_EPTCTLDISx (disable endpoint).

ERR_FLUSH: Bank Flush Error (cleared upon USB reset)

– (for High Bandwidth Isochronous IN endpoints)

This bit is set when flushing unsent banks at the end of a microframe.

This bit is reset by UDPHS_EPTRST register EPT_x (reset endpoint) and by EPT_CTL_DISx (disable endpoint).

CURBK: Current Bank (cleared upon USB reset)

– **Current Bank**:

These bits are set by hardware to indicate the number of the current bank.

Value	Name	Description
0	BANK0	Bank 0 (or single bank)
1	BANK1	Bank 1
2	BANK2	Bank 2

Note: The current bank is updated each time the user:
- Sets the TX Packet Ready bit to prepare the next IN transfer and to switch to the next bank.
- Clears the received OUT data bit to access the next bank.

This bit is reset by UDPHS_EPTRST register EPT_x (reset endpoint) and by UDPHS_EPTCTLDISx (disable endpoint).

BUSY_BANK_STA: Busy Bank Number (cleared upon USB reset)

These bits are set by hardware to indicate the number of busy banks.

– **IN endpoint**: It indicates the number of busy banks filled by the user, ready for IN transfer.

– **OUT endpoint**: It indicates the number of busy banks filled by OUT transaction from the Host.

Value	Name	Description
0	0BUSYBANK	All banks are free
1	1BUSYBANK	1 busy bank
2	2BUSYBANKS	2 busy banks
3	3BUSYBANKS	3 busy banks

42.7.13 EHCI: REG00 - Programmable Microframe Base Value

Name: UHPHS_INSNREG00

Access: Read/Write

31	30	29	28	27	26	25	24
–							
23	22	21	20	19	18	17	16
–				Debug			
15	14	13	12	11	10	9	8
Debug		MFC_8		MFC_16			
7	6	5	4	3	2	1	0
MFC_16							En

The Programmable Microframe Base Value is used to change the microframe length value (default is microframe SOF = 125 µs) in order to reduce simulation time.

En: Enable this Register

0: Register disabled (default value).

1: Register enabled.

Note: Do not enable this register for the gate-level netlist.

MFC_16: Microframe Counter with Word Byte Interface

This value is used as the 1-microframe counter with 16-bit interface.

MFC_8: Microframe Counter with Byte Interface

This value is used as the 1-microframe counter with 8-bit interface.

Debug: Debug Purposes

This field is used for debug purposes only.

In Heterogeneous mode, if the per port clock gets out of sync (but still within the ppm limits) of the phy_clk, then the per port SOF counter needs some correction relative to the global SOF counter. The RTL corrects itself if this happens.

This field controls the SOF correction, in case some debugging is required for the correction.

If bit 14 is set to 1, then it enables the RTL to use the value in bits 19:15 to perform the correction.

In normal operating mode, these bits should not be written.

Note:

The “value” in bits [31:1] must be programmed as follows: (value + 32/64) * Clock Period = microframe timer duration
Factor 32 is used for a 16-bit interface and factor 64 is used for an 8-bit interface. For example, for the full (125 µs) microframe duration:

- In 8-bit, 60-MHz mode, the value is h1D0C (=7436), so (7436 + 64) * 16.67 ns = 125 µs
- In 16-bit, 30-MHz mode, the value is hE86 (=3718), so (3718 + 32) * 33.33 ns = 125 µs

For a 50 µs microframe duration:

- In 8-bit, 60-MHz mode, the value is hB77 (=2395), so (2395 + 64) * 16.67 ns = 50 µs
- In 16-bit, 30-MHz mode, the value is h5BC (=1468), so (1468 + 32) * 33.33 ns = 50 µs

Figure 47-81: TDRE in Single Data Mode and TXRDYM = 0

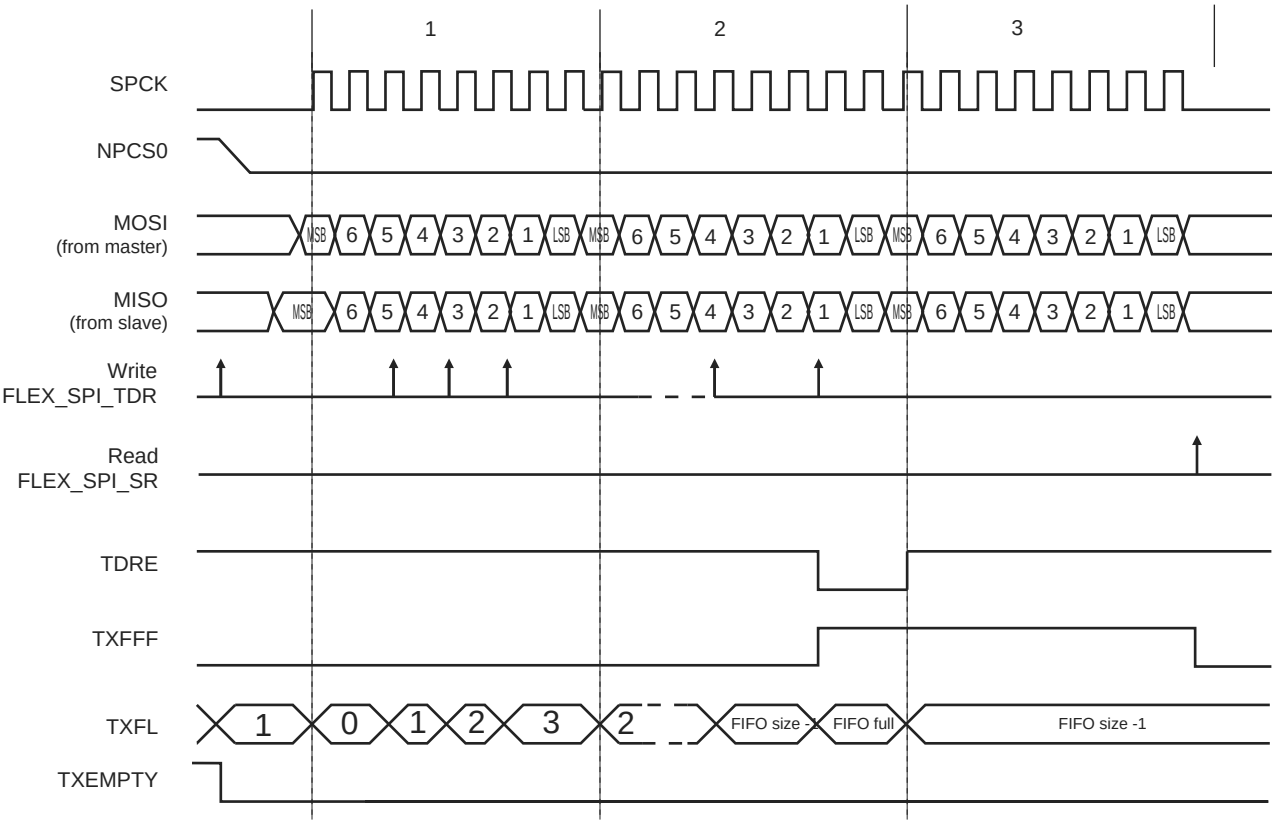
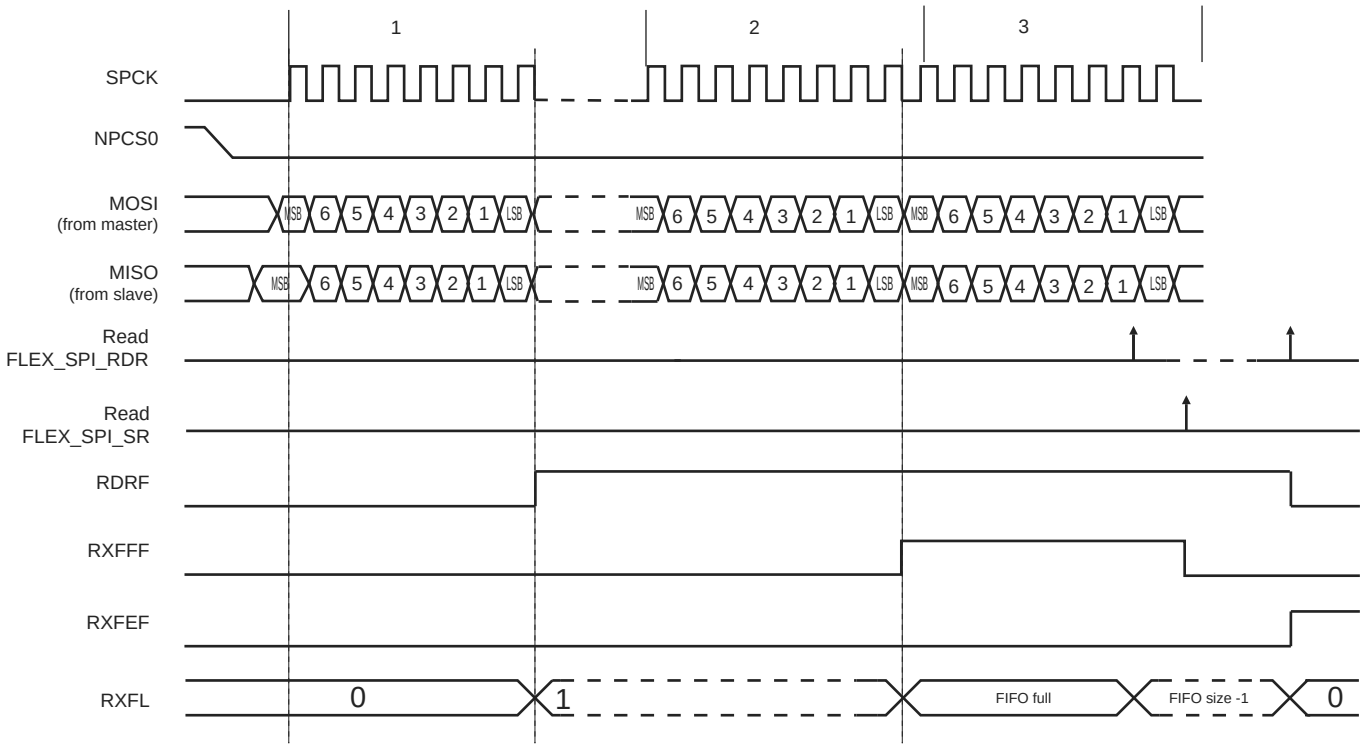


Figure 47-82: RDRF in Single Data Mode and RXRDYM = 0



50.6.5.3 Read Memory Transfer

The user can access the data of the serial memory by sending an instruction with QSPI_IFR.DATAEN = 1 and QSPI_IFR.TFRTYP = 1.

In this mode, the QSPI is able to read data at random address into the serial Flash memory, allowing the CPU to execute code directly from it (XIP execute-in-place).

In order to fetch data, the user must first configure the instruction frame by writing the QSPI_IFR. Then data can be read at any address in the QSPI address space mapping. The address of the system bus read accesses match the address of the data inside the serial Flash memory.

When Fetch mode is enabled, several instruction frames can be sent before writing QSPI_CR.LASTXFR. Each time the system bus read accesses become nonsequential (addresses are not consecutive), a new instruction frame is sent with the corresponding address.

50.6.5.4 Continuous Read Mode

The QSPI is compatible with the Continuous Read mode which is implemented in some serial Flash memories.

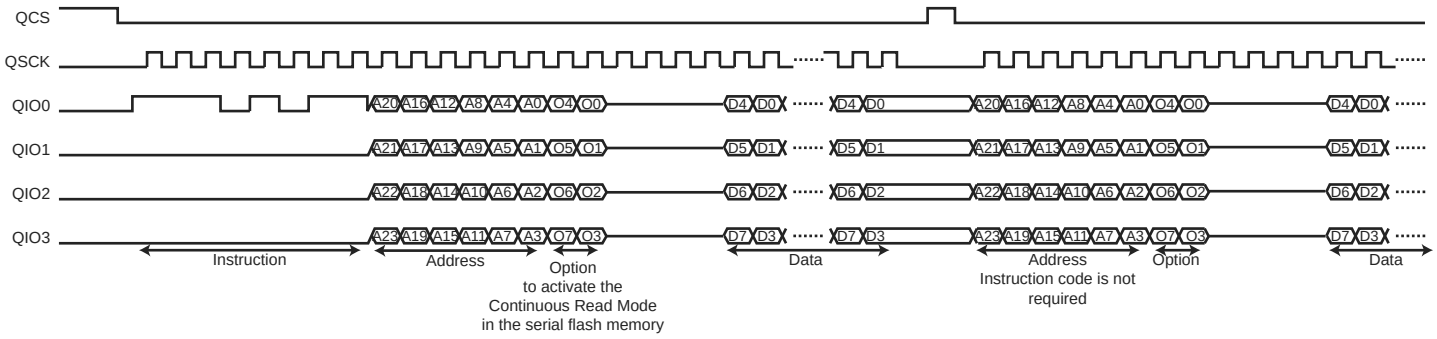
In Continuous Read mode, the instruction overhead is reduced by excluding the instruction code from the instruction frame. When the Continuous Read mode is activated in a serial Flash memory by a specific option code, the instruction code is stored in the memory. For the next instruction frames, the instruction code is not required as the memory uses the stored one.

In the QSPI, Continuous Read mode is used when reading data from the memory (QSPI_IFR.TFRTYP = 1). The addresses of the system bus read accesses are often nonsequential and this leads to many instruction frames that have the same instruction code. By disabling the send of the instruction code, the Continuous Read mode reduces the access time of the data.

To be functional, this mode must be enabled in both the QSPI and the serial Flash memory. The Continuous Read mode is enabled in the QSPI by writing CRM to ‘1’ in the QSPI_IFR (TFRTYP must equal 1). The Continuous Read mode is enabled in the serial Flash memory by sending a specific option code.

CAUTION: If the Continuous Read mode is not supported by the serial Flash memory or disabled, CRM bit must not be written to ‘1’, otherwise data read out of the serial Flash memory is unpredictable.

Figure 50-10: Continuous Read Mode



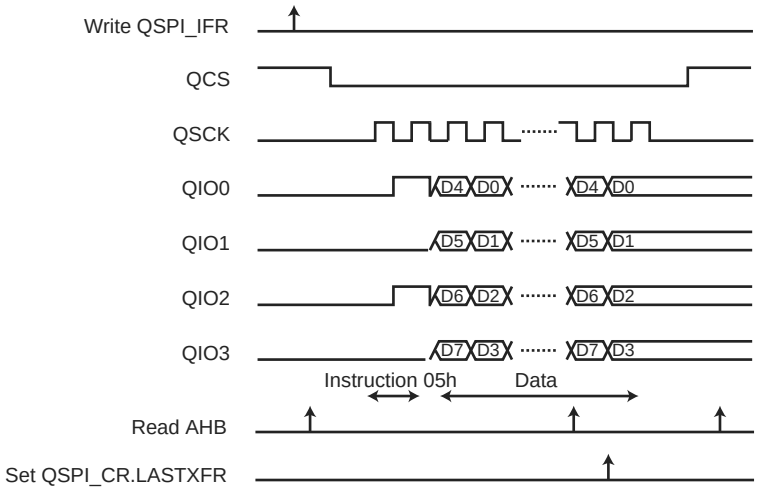
Example 9:

Instruction in Quad SPI, without address, without option, with data read in Quad SPI, without dummy cycles, without fetch.

Command: HIGH-SPEED READ (05h)

- Write 0x0000_0005 in QSPI_ICR.
- Write 0x0000_0096 in QSPI_IFR.
- Read QSPI_IFR (dummy read) to synchronize system bus accesses.
- Read data in the QSPI system bus memory space (0x9000_00000-0x9800_00000/0XD000_0000--0XD800_0000). Fetch is disabled.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 50-19: Instruction Transmission Waveform 9



50.7.2 QSPI Mode Register

Name: QSPI_MR

Address: 0xF0020004 (0), 0xF0024004 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
DLYCS							
23	22	21	20	19	18	17	16
DLYBCT							
15	14	13	12	11	10	9	8
–	–	–	–	NBBITS			
7	6	5	4	3	2	1	0
–	–	CSMODE		SMRM	WDRBT	LLB	SMM

This register can only be written if bit WPEN is cleared in the QSPI Write Protection Mode Register.

SMM: Serial Memory Mode

0 (SPI): The QSPI is in SPI mode.

1 (MEMORY): The QSPI is in Serial Memory mode.

LLB: Local Loopback Enable

0 (DISABLED): Local loopback path disabled.

1 (ENABLED): Local loopback path enabled.

LLB controls the local loopback on the data serializer for testing in SPI mode only. (MISO is internally connected on MOSI).

WDRBT: Wait Data Read Before Transfer

0 (DISABLED): No effect. In SPI mode, a transfer can be initiated whatever the state of the QSPI_RDR is.

1 (ENABLED): In SPI mode, a transfer can start only if the QSPI_RDR is empty, i.e., does not contain any unread data. This mode prevents overrun error in reception.

SMRM: Serial Memory Register Mode

0: Serial Memory registers are written via AHB access. See **Section 50.6.5.2 “Instruction Frame Transmission”** for details.

1: Serial Memory registers are written via APB access. See **Section 50.6.5.2 “Instruction Frame Transmission”** for details.

CSMODE: Chip Select Mode

The CSMODE field determines how the chip select is deasserted

Note: This field is forced to LASTXFER when SMM is written to ‘1’.

Value	Name	Description
0	NOT_RELOADED	The chip select is deasserted if QSPI_TDR.TD has not been reloaded before the end of the current transfer.
1	LASTXFER	The chip select is deasserted when the bit LASTXFER is written to ‘1’ and the character written in QSPI_TDR.TD has been transferred.
2	SYSTEMATICALLY	The chip select is deasserted systematically after each transfer.

NBBITS: Number Of Bits Per Transfer

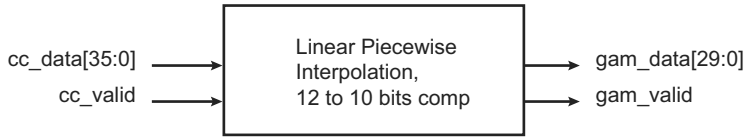
Value	Name	Description
0	8_BIT	8 bits for transfer
8	16_BIT	16 bits for transfer

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} RRGAIN & RGGAIN & RBGAIN \\ GRGAIN & GGGAIN & GBGAIN \\ BRGAIN & BGGAIN & BBGAIN \end{bmatrix} \times \begin{bmatrix} cfa\_data[35:24] \\ cfa\_data[23:12] \\ cfa\_data[11:0] \end{bmatrix} + \begin{bmatrix} ROFST \\ GOFST \\ BOFST \end{bmatrix}$$

52.5.9 Gamma Curve (GAM) Module

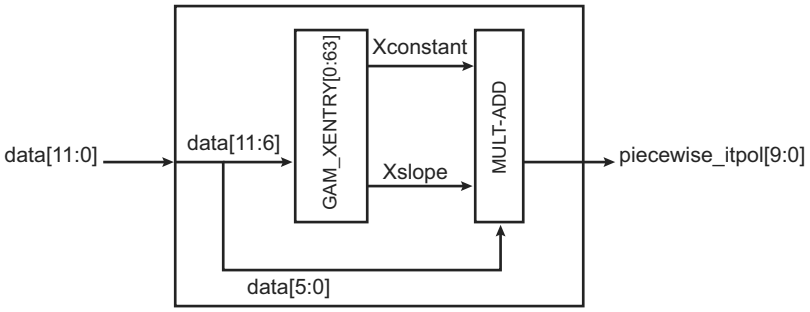
The GAM module samples the cc_data[35:0] bus when cc_valid is asserted, and generates gam_data[29:0] 30-bit width data along with the validity signal gam_valid. Imaging devices have non-linear characteristics, but the transfer function is approximated by a power function. The intensity of each of the linear RGB components is transformed to a non-linear signal through the use of the gamma correction submodule. The power function is linearly interpolated using 64 breakpoints. This also performs a 12-bit to 10-bit compression. The polynomial for the linear interpolation between breakpoints is ***i*** and ***i*** +1. Consequently, for each breakpoint, two values are required: constant and slope. The table values are programmable through the user interface when the gamma correction module is disabled (ISC_GAM_CTRL.ENABLE is cleared). ISC_GAM_RENTRY is used for Red gamma correction. ISC_GAM_GENTRY is used for Green gamma correction. ISC_GAM_BENTRY is used for Blue gamma correction. Each table entry is composed of a 10-bit (signed) slope and a 10-bit constant.

Figure 52-23: GAM Block Diagram



ISC_GAM_CTRL.ENABLE	ISC_GAM_CTRL.XLUT	GAM_DATA Slice	Value
0	0	gam_data[29:0]	cc_data[29:0]
1	0	gam_data[29:20]	cc_data[35:26]
		gam_data[19:10]	cc_data[23:14]
		gam_data[9:0]	cc_data[11:2]
1	1	gam_data[29:20]	R=piecewise_itpol(cc_data_r[35:24])
		gam_data[19:10]	G=piecewise_itpol(cc_data_r[23:12])
		gam_data[9:0]	B=piecewise_itpol(cc_data_r[11:0])

Figure 52-24: Piecewise Linear Interpolation Block Diagram



The interpolation consists of three tables that store the function values GAM_XENTRY[0:63] where X stands for R, G and B. The input of the table has six bits. It outputs a slope and a constant. The slope is later multiplied by the data lsb (6-bit) and added to a constant. The final value is the gamma-corrected value of the input. This module performs a 12-to-10 compression.

52.6.31 ISC Gamma Correction Blue Entry Register

Name: ISC_GAM_BENTRYx[x=0...63]

Address: 0xF0008098

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	BCONSTANT	

23	22	21	20	19	18	17	16
BCONSTANT							

15	14	13	12	11	10	9	8
–	–	–	–	–	–	BSLOPE	

7	6	5	4	3	2	1	0
BSLOPE							

BSLOPE: Blue Color Slope for Piecewise Interpolation (signed 10 bits 1:3:6)

BCONSTANT: Blue Color Constant for Piecewise Interpolation (unsigned 10 bits 0:10:0)

64.6.6 SECUMOD PIO Backup Register x

Name: SECUMOD_PIOBUx

Address: 0xFC040018

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
SWITCH	SCHEDULE	PULLUP		–	PIO_PDS	PIO_SOD	OUTPUT

7	6	5	4	3	2	1	0
PIOBU_RFV				PIOBU_AFV			

Note: The FILTER3_5 and DYNSTAT fields only exist for even PIOBUs.

PIOBU_AFV: PIOBU Alarm Filter Value

This field is used to define the filter value prior to generating an alarm.

PIOBU_AFV	Maximum Counter Value
0	0 (No static protection)
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512

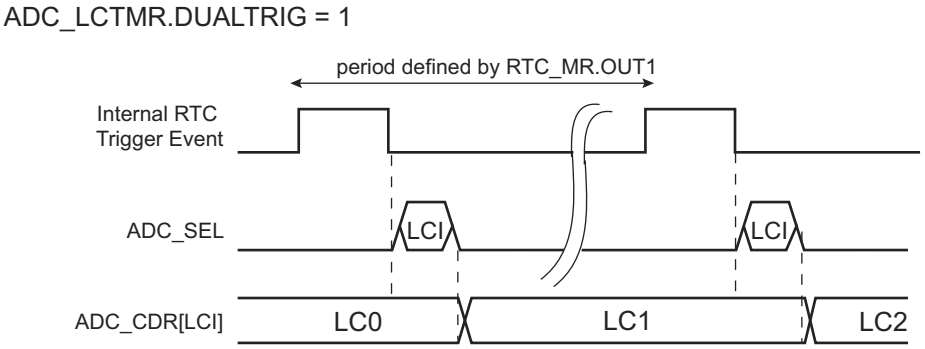
This field must be set to 0 when Dynamic Intrusion is selected.

PIOBU_RFV: PIOBUx Reset Filter Value

This field is used to define the number of consecutive valid states to be reached before resetting the AFV counter.

PIOBU_RFV	Maximum Counter Value
0	0 (No static protection)
1	2
2	4
3	8
4	16
5	32

Figure 65-10: Only Last Channel Measurement Triggered at Low Speed (ADC_CHSR[LCI] = 0 and ADC_TRGR.TRGMOD = 0)



Notes: ADC_SEL: Command to the ADC analog cell
LCx: Last channel value
LCI: Last channel index

65.6.13 Enhanced Resolution Mode and Digital Averaging Function

65.6.13.1 Enhanced Resolution Mode

The Enhanced Resolution mode is enabled if the OSR field is configured to 1 or 2 in ADC_EMR. The enhancement is based on a digital averaging function.

There is no averaging on the last index channel if the measure is triggered by an RTC event.

In this mode, the ADC Controller will trade off conversion speed against accuracy by averaging multiple samples, thus providing a digital low-pass filter function.

The selected oversampling ratio applies to all enabled channels when triggered by an RTC event.

$$\text{ADC\_LCDR.LDATA} = \frac{1}{M} \times \sum_{k=0}^{k=N-1} \text{ADC}(k)$$

where N and M are given in the table below.

Table 65-5: Digital Averaging Function Configuration versus OSR Values

ADC_EMR.OSR Value	ADC_LCDR.LDATA Length	N Value	M Value	Full Scale Value	Maximum Value
0	12 bits	1	1	4095	4095
1	13 bits	4	2	8191	8190
2	14 bits	16	4	16383	16381

The average result is valid in ADC_CDRx (x corresponds to the index of the channel) only if the EOCn flag is set in ADC_ISR and if the OVREn flag is cleared in ADC_OVER. The average result for all channels is valid in ADC_LCDR only if DRDY is set and GOVRE is cleared in ADC_ISR.

Note that ADC_CDRs are not buffered. Therefore, when an averaging sequence is ongoing, the value in these registers changes after each averaging sample. However, overrun flags in ADC_OVER rise as soon as the first sample of an averaging sequence is received. Thus the previous averaged value is not read, even if the new averaged value is not ready.

Consequently, when an overrun flag rises in ADC_OVER, it means that the previous unread data is lost but it does not mean that this data has been overwritten by the new averaged value as the averaging sequence concerning this channel can still be ongoing.

65.7.16 ADC Extended Mode Register

Name: ADC_EMR

Address: 0xFC030040

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	ADCMODE		–	SIGNMODE		TAG
23	22	21	20	19	18	17	16
–	–	SRCCLK	ASTE	–	–	OSR	
15	14	13	12	11	10	9	8
–	–	CMPFILTER		–	–	CMPALL	–
7	6	5	4	3	2	1	0
CMPSEL				–	CMPTYPE	CMPMODE	

This register can only be written if the WPEN bit is cleared in the ADC Write Protection Mode Register.

CMPMODE: Comparison Mode

Value	Name	Description
0	LOW	When the converted data is lower than the low threshold of the window, generates the COMPE flag in ADC_ISR or, in Partial Wakeup mode, defines the conditions to exit system from Wait mode.
1	HIGH	When the converted data is higher than the high threshold of the window, generates the COMPE flag in ADC_ISR or, in Partial Wakeup mode, defines the conditions to exit system from Wait mode.
2	IN	When the converted data is in the comparison window, generates the COMPE flag in ADC_ISR or, in Partial Wakeup mode, defines the conditions to exit system from Wait mode.
3	OUT	When the converted data is out of the comparison window, generates the COMPE flag in ADC_ISR or, in Partial Wakeup mode, defines the conditions to exit system from Wait mode.

CMPTYPE: Comparison Type

Value	Name	Description
0	FLAG_ONLY	Any conversion is performed and comparison function drives the COMPE flag.
1	START_CONDITIO N	Comparison conditions must be met to start the storage of all conversions until the CMPRST bit is set.

CMPSEL: Comparison Selected Channel

If CMPALL = 0: CMPSEL indicates which channel has to be compared.

If CMPALL = 1: No effect.

CMPALL: Compare All Channels

0: Only channel indicated in CMPSEL field is compared.

1: All channels are compared.

CMPFILTER: Compare Event Filtering

Number of consecutive compare events necessary to raise the flag = CMPFILTER+1

When programmed to 0, the flag rises as soon as an event occurs.

See Section 65.6.9 “Comparison Window” when using filtering option (CMPFILTER > 0).

Table 72-6: SAMA5D2 Datasheet Rev. 11267B Revision History (Continued)

Issue Date	Changes
13-Nov-15	Section 39. “Audio Class D Amplifier (CLASSD)” Updated Figure 39-1. CLASSD Block Diagram
	Section 41. “Inter-IC Sound Controller (I2SC)” Replaced all instances of “PCKx” with “GCLK” Removed all references to Time Division Multiplexed (TDM) format (not supported) Section 41.1 “Description”: replaced “The I2SC can use either a single DMA Controller channel for both audio channels or one DMA Controller channel per audio channel.” with “The I2SC uses a single DMA Controller channel for both audio channels.”, and updated Section 41.2 “Embedded Characteristics” and Section 41.6.8 “DMA Controller Operation” accordingly Section 41.8.2 “Inter-IC Sound Controller Mode Register”: removed fields RXDMA and TXDMA
	Section 44. “Flexible Serial Communication Controller (FLEXCOM)” Added SPI mode in UART/USART Replaced all instances of ‘PCK’ with ‘GCLK’ Replaced all instances of ‘DMAC/PDC’ with ‘DMAC’ Removed SleepWalking characteristic from UART/USART mode Removed all references to ISO7816 specification Section 44.10.6 “USART Mode Register”updated USCLKS field description Section 44.10.44 “SPI Mode Register”: updated BRSRCCLK and DLYBCS field descriptions Section 44.10.54 “SPI Chip Select Register”: updated CSNAAT, SCBR, DLYBS and DLYBCT field descriptions Section 44.10.64 “TWI Clock Waveform Generator Register”: updated BRSRCCLK and CKSRC field descriptions Updated Figure 44-1 “FLEXCOM Block Diagram” and Figure 44-67 “Master Mode Block Diagram”
	Section 42. “Two-wire Interface (TWIHS)” Replaced all instances of “PMC_PCK” with “GCLK”
	Section 55. “Universal Asynchronous Receiver Transmitter (UART)” Replaced "Processor-Independent Source Clock" with "Processor-Independent Generic Source Clock" and "PCK" with "GCLK"
	Section 48. “Secure Digital Multimedia Card Controller (SDMMC)” Updated revision of supported e.MMC specification (from V4.41 to V4.51)
	Section 51. “Pulse Density Modulation Interface Controller (PDMIC)” Removed all references to PDC Removed Section 1.6.4 “Buffer Structure”
	Section 54. “Secure Fuse Controller (SFC)” Removed all references to lock fuse (not supported) Section 54.4.5.3 “Fuse Masking”: corrected data register names Section 54.5.2 “SFC Mode Register”: updated MSK field description Table 54-1 “Register Mapping”: modified SFC_IER and SFC_IDR access type from “Read/Write” to “Write-only”
	Section 57. “Advanced Encryption Standard (AES)” Updated Figure 57-12 “Generation of an ESP IPSec Frame without ESN” and Figure 57-13 “Generation of an ESP IPSec Frame with ESN”
	Added Section 61. “Security Module”