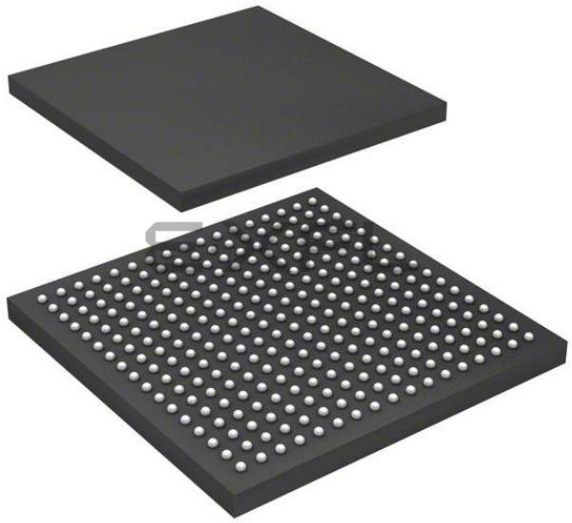

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Understanding Embedded - Microprocessors

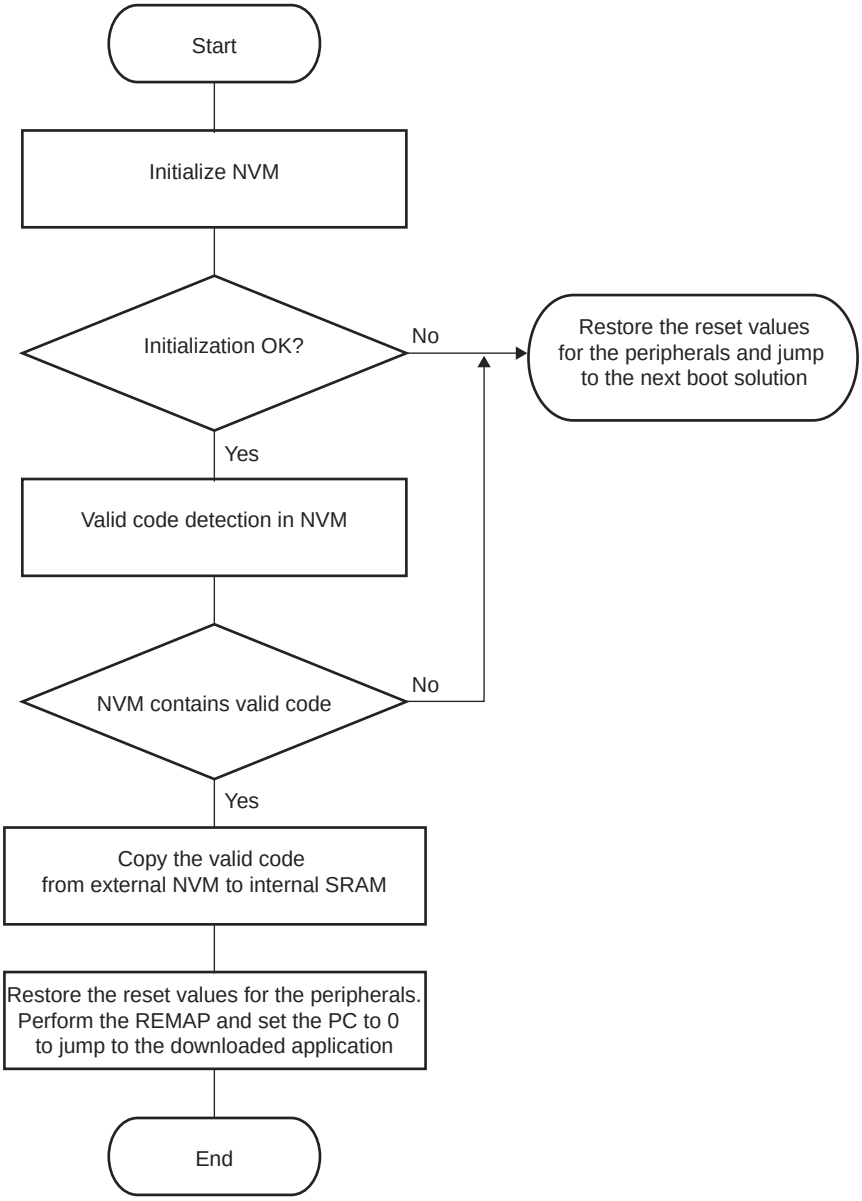
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d28b-cn

Figure 16-5: NVM Boot Diagram



22.5.3 Watchdog Timer Status Register

Name: WDT_SR

Address: 0xF8048048

Access Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	–	WDERR	WDUNF

WDUNF: Watchdog Underflow (cleared on read)

0: No watchdog underflow occurred since the last read of WDT_SR.

1: At least one watchdog underflow occurred since the last read of WDT_SR.

WDERR: Watchdog Error (cleared on read)

0: No watchdog error occurred since the last read of WDT_SR.

1: At least one watchdog error occurred since the last read of WDT_SR.

23.4 Functional Description

23.4.1 Reset Controller Overview

The Reset Controller is made up of an NRST Manager, a Startup Counter and a Reset State Manager. It runs at Slow Clock and generates the following reset signals:

- Processor Reset: resets the processor and the whole set of embedded peripherals.
- Backup Reset: resets all the peripherals powered by VDDBU.

These reset signals are asserted by the Reset Controller, either on external events or on software action. The Reset State Manager controls the generation of reset signals.

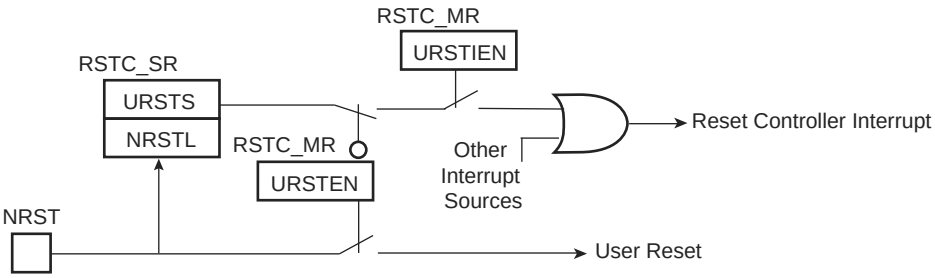
The startup counter waits for the complete crystal oscillator startup. The wait delay is given by the crystal oscillator startup time maximum value that can be found under “Crystal Oscillator Characteristics” in the “Electrical Characteristics” section.

The Reset Controller Mode Register (RSTC_MR), used to configure the reset controller, is powered with VDDBU, so that its configuration is saved as long as VDDBU is on.

23.4.2 NRST Manager

The NRST Manager samples the NRST input pin and drives this pin low when required by the Reset State Manager. Figure 23-2 shows the block diagram of the NRST Manager.

Figure 23-2: NRST Manager



23.4.2.1 NRST Signal or Interrupt

The NRST Manager samples the NRST pin at Slow Clock speed. When the line is detected low, a User Reset is reported to the Reset State Manager.

However, the NRST Manager can be programmed to not trigger a reset when an assertion of NRST occurs. Writing a zero to the URSTEN bit in the RSTC_MR disables the User Reset trigger.

The level of the pin NRST can be read at any time in the bit NRSTL (NRST level) in the Reset Controller Status Register (RSTC_SR). As soon as the pin NRST is asserted, the bit URSTS in the RSTC_SR is set. This bit clears only when RSTC_SR is read.

The reset controller can also be programmed to generate an interrupt instead of generating a reset. To do so, the bit URSTIEN in the RSTC_MR must be set.

23.4.3 Reset States

The Reset State Manager handles the different reset sources and generates the internal reset signals. It reports the reset status in the field RSTTYP of the RSTC_SR. The update of the field RSTTYP is performed when the processor reset is released.

23.4.3.1 General Reset

A general reset occurs when VDDBU and VDDCORE are powered on. The backup supply POR cell output rises and is filtered with a Startup Counter, which operates at Slow Clock. The purpose of this counter is to make sure the Slow Clock oscillator is stable before starting up the device. The length of startup time is hardcoded to comply with the Slow Clock Oscillator startup time.

After this time, the processor clock is released at Slow Clock and all the other signals remain valid for 2 cycles for proper processor and logic reset. Then, all the reset signals are released and the field RSTTYP in the RSTC_SR reports a General Reset.

When VDDBU is detected low by the backup supply POR cell, all resets signals are immediately asserted, even if the main supply POR cell does not report a main supply shutdown.

VDDBU only activates the Backup Reset signal.

Backup Reset must be released so that any other reset can be generated by VDDCORE (main supply POR output).

38.9.24 XDMAC Channel x [x = 0..15] Next Descriptor Address Register

Name: XDMAC_CNDAx [x = 0..15]

Address: 0xF0004068 (1)[0], 0xF00040A8 (1)[1], 0xF00040E8 (1)[2], 0xF0004128 (1)[3], 0xF0004168 (1)[4], 0xF00041A8 (1)[5], 0xF00041E8 (1)[6], 0xF0004228 (1)[7], 0xF0004268 (1)[8], 0xF00042A8 (1)[9], 0xF00042E8 (1)[10], 0xF0004328 (1)[11], 0xF0004368 (1)[12], 0xF00043A8 (1)[13], 0xF00043E8 (1)[14], 0xF0004428 (1)[15], 0xF0010068 (0)[0], 0xF00100A8 (0)[1], 0xF00100E8 (0)[2], 0xF0010128 (0)[3], 0xF0010168 (0)[4], 0xF00101A8 (0)[5], 0xF00101E8 (0)[6], 0xF0010228 (0)[7], 0xF0010268 (0)[8], 0xF00102A8 (0)[9], 0xF00102E8 (0)[10], 0xF0010328 (0)[11], 0xF0010368 (0)[12], 0xF00103A8 (0)[13], 0xF00103E8 (0)[14], 0xF0010428 (0)[15]

Access: Read/Write

31	30	29	28	27	26	25	24
NDA							

23	22	21	20	19	18	17	16
NDA							

15	14	13	12	11	10	9	8
NDA							

7	6	5	4	3	2	1	0
NDA						–	NDAIF

NDAIF: Channel x Next Descriptor Interface

0: The channel descriptor is retrieved through the system interface 0.

1: The channel descriptor is retrieved through the system interface 1.

NDA: Channel x Next Descriptor Address

The 30-bit width of the NDA field represents the next descriptor address range 31:2. The descriptor is word-aligned and the two least significant register bits 1:0 are ignored.

39.7.101 High-End Overlay Configuration Register 6

Name: LCDC_HEOCFG6

Address: 0xF00003A4

Access: Read/Write

31	30	29	28	27	26	25	24
PSTRIDE							

23	22	21	20	19	18	17	16
PSTRIDE							

15	14	13	12	11	10	9	8
PSTRIDE							

7	6	5	4	3	2	1	0
PSTRIDE							

PSTRIDE: Pixel Stride

PSTRIDE represents the memory offset, in bytes, between two pixels of the image memory.

40.8.5 GMAC DMA Configuration Register

Name: GMAC_DCFGR

Address: 0xF8008010

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	DDRP

23	22	21	20	19	18	17	16
DRBS							

15	14	13	12	11	10	9	8
–	–	–	–	TXCOEN	TXPBMS	RXBMS	

7	6	5	4	3	2	1	0
ESPA	ESMA	–	FBLDO				

FBLDO: Fixed Burst Length for DMA Data Operations:

Selects the burst length to attempt to use on the AHB when transferring frame data. Not used for DMA management operations and only used where space and data size allow. Otherwise SINGLE type AHB transfers are used.

One-hot priority encoding enforced automatically on register writes as follows, where ‘x’ represents don’t care:

Value	Name	Description
0	–	Reserved
1	SINGLE	00001: Always use SINGLE AHB bursts
2	–	Reserved
4	INCR4	001xx: Attempt to use INCR4 AHB bursts (Default)
8	INCR8	01xxx: Attempt to use INCR8 AHB bursts
16	INCR16	1xxxx: Attempt to use INCR16 AHB bursts

ESMA: Endian Swap Mode Enable for Management Descriptor Accesses

When set, selects swapped endianism for AHB transfers. When clear, selects little endian mode.

ESPA: Endian Swap Mode Enable for Packet Data Accesses

When set, selects swapped endianism for AHB transfers. When clear, selects little endian mode.

RXBMS: Receiver Packet Buffer Memory Size Select

The default receive packet buffer size is 4 Kbytes. The table below shows how to configure this memory to FULL, HALF, QUARTER or EIGHTH of the default size.

Value	Name	Description
0	EIGHTH	4/8 Kbyte Memory Size
1	QUARTER	4/4 Kbytes Memory Size
2	HALF	4/2 Kbytes Memory Size
3	FULL	4 Kbytes Memory Size

Indicates a valid pause has been received that has a non-zero pause quantum field. Cleared on read.

PTZ: Pause Time Zero

Set when either the Pause Time register at address 0x38 decrements to zero, or when a valid pause frame is received with a zero pause quantum field. Cleared on read.

PFTR: Pause Frame Transmitted

Indicates a pause frame has been successfully transmitted after being initiated from the Network Control register. Cleared on read.

DRQFR: PTP Delay Request Frame Received

Indicates a PTP delay_req frame has been received. Cleared on read.

SFR: PTP Sync Frame Received

Indicates a PTP sync frame has been received. Cleared on read.

DRQFT: PTP Delay Request Frame Transmitted

Indicates a PTP delay_req frame has been transmitted. Cleared on read.

SFT: PTP Sync Frame Transmitted

Indicates a PTP sync frame has been transmitted. Cleared on read.

PDRQFR: PDelay Request Frame Received

Indicates a PTP pdelay_req frame has been received. Cleared on read.

PDRSFR: PDelay Response Frame Received

Indicates a PTP pdelay_resp frame has been received. Cleared on read.

PDRQFT: PDelay Request Frame Transmitted

Indicates a PTP pdelay_req frame has been transmitted. Cleared on read.

PDRSFT: PDelay Response Frame Transmitted

Indicates a PTP pdelay_resp frame has been transmitted. Cleared on read.

SRI: TSU Seconds Register Increment

Indicates the register has incremented. Cleared on read.

RXLPISBC: Receive LPI indication Status Bit Change

Receive LPI indication status bit change. Cleared on read.

WOL: Wake On LAN

WOL interrupt. Indicates a WOL event has been received.

TSUTIMCOMP: TSU Timer Comparison

Indicates when TSU timer count value is equal to programmed value. Cleared on read.

40.8.112 GMAC Receive Buffer Queue Base Address Register Priority Queue x

Name: GMAC_RBQBAPQx[x=1..2]

Address: 0xF8008480

Access: Read/Write

31	30	29	28	27	26	25	24
RXBQBA							

23	22	21	20	19	18	17	16
RXBQBA							

15	14	13	12	11	10	9	8
RXBQBA							

7	6	5	4	3	2	1	0
RXBQBA						–	–

These registers hold the start address of the receive buffer queues (receive buffers descriptor lists) for the additional queues and must be initialized to the address of valid descriptors, even if the priority queues are not used.

RXBQBA: Receive Buffer Queue Base Address

Written with the address of the start of the receive queue.

41.7.3 UDPHS Interrupt Enable Register

Name: UDPHS_IEN

Address: 0xFC02C010

Access: Read/Write

31	30	29	28	27	26	25	24
DMA_7	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	–
23	22	21	20	19	18	17	16
EPT_15	EPT_14	EPT_13	EPT_12	EPT_11	EPT_10	EPT_9	EPT_8
15	14	13	12	11	10	9	8
EPT_7	EPT_6	EPT_5	EPT_4	EPT_3	EPT_2	EPT_1	EPT_0
7	6	5	4	3	2	1	0
UPSTR_RES	ENDOFRSM	WAKE_UP	ENDRESET	INT_SOF	MICRO_SOF	DET_SUSPD	–

DET_SUSPD: Suspend Interrupt Enable (cleared upon USB reset)

0: Disable Suspend Interrupt.

1: Enable Suspend Interrupt.

MICRO_SOF: Micro-SOF Interrupt Enable (cleared upon USB reset)

0: Disable Micro-SOF Interrupt.

1: Enable Micro-SOF Interrupt.

INT_SOF: SOF Interrupt Enable (cleared upon USB reset)

0: Disable SOF Interrupt.

1: Enable SOF Interrupt.

ENDRESET: End Of Reset Interrupt Enable (cleared upon USB reset)

0: Disable End Of Reset Interrupt.

1: Enable End Of Reset Interrupt. Automatically enabled after USB reset.

WAKE_UP: Wake Up CPU Interrupt Enable (cleared upon USB reset)

0: Disable Wakeup CPU Interrupt.

1: Enable Wakeup CPU Interrupt.

ENDOFRSM: End Of Resume Interrupt Enable (cleared upon USB reset)

0: Disable Resume Interrupt.

1: Enable Resume Interrupt.

UPSTR_RES: Upstream Resume Interrupt Enable (cleared upon USB reset)

0: Disable Upstream Resume Interrupt.

1: Enable Upstream Resume Interrupt.

EPT_x: Endpoint x Interrupt Enable (cleared upon USB reset)

0: Disable the interrupts for this endpoint.

1: Enable the interrupts for this endpoint.

DMA_x: DMA Channel x Interrupt Enable (cleared upon USB reset)

0: Disable the interrupts for this channel.

1: Enable the interrupts for this channel.

42.7.6 UHPHS USB Interrupt Enable Register

Name: UHPHS_USBINTR

Access: Read/Write

31	30	29	28	27	26	25	24
–							
23	22	21	20	19	18	17	16
–							
15	14	13	12	11	10	9	8
–							
7	6	5	4	3	2	1	0
–		IAAE	HSEE	FLRE	PCIE	USBEIE	USBIE

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the UHPHS_USBSTS to allow the software to poll for events.

Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism.

For all enable register bits, 1= Enabled, 0= Disabled.

USBIE: USB Interrupt Enable

When this bit is set to 1, and the USBINT bit in the UHPHS_USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

USBEIE: USB Error Interrupt Enable

When this bit is set to 1, and the USBERRINT bit in the UHPHS_USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.

PCIE: Port Change Interrupt Enable

When this bit is set to 1, and the Port Change Detect bit in the UHPHS_USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.

FLRE: Frame List Rollover Enable

When this bit is set to 1, and the Frame List Rollover bit in the UHPHS_USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.

HSEE: Host System Error Enable

When this bit is set to 1, and the Host System Error Status bit in the UHPHS_USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.

IAAE: Interrupt on Async Advance Enable

When this bit is set to 1, and the Interrupt on Async Advance bit in the UHPHS_USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.

45.9 Synchronous Serial Controller (SSC) User Interface

Table 45-5: Register Mapping

Offset	Register	Name	Access	Reset
0x0	Control Register	SSC_CR	Write-only	–
0x4	Clock Mode Register	SSC_CMR	Read/Write	0x0
0x8–0xC	Reserved	–	–	–
0x10	Receive Clock Mode Register	SSC_RCMR	Read/Write	0x0
0x14	Receive Frame Mode Register	SSC_RFMR	Read/Write	0x0
0x18	Transmit Clock Mode Register	SSC_TCMR	Read/Write	0x0
0x1C	Transmit Frame Mode Register	SSC_TFMR	Read/Write	0x0
0x20	Receive Holding Register	SSC_RHR	Read-only	0x0
0x24	Transmit Holding Register	SSC_THR	Write-only	–
0x28–0x2C	Reserved	–	–	–
0x30	Receive Sync. Holding Register	SSC_RSHR	Read-only	0x0
0x34	Transmit Sync. Holding Register	SSC_TSHR	Read/Write	0x0
0x38	Receive Compare 0 Register	SSC_RC0R	Read/Write	0x0
0x3C	Receive Compare 1 Register	SSC_RC1R	Read/Write	0x0
0x40	Status Register	SSC_SR	Read-only	0x000000CC
0x44	Interrupt Enable Register	SSC_IER	Write-only	–
0x48	Interrupt Disable Register	SSC_IDR	Write-only	–
0x4C	Interrupt Mask Register	SSC_IMR	Read-only	0x0
0x50–0xE0	Reserved	–	–	–
0xE4	Write Protection Mode Register	SSC_WPMR	Read/Write	0x0
0xE8	Write Protection Status Register	SSC_WPSR	Read-only	0x0
0xEC–0xFC	Reserved	–	–	–
0x100–0x124	Reserved	–	–	–

The TWIHS slave in High-speed mode requires that the peripheral clock runs at a minimum of 14 MHz if slave clock stretching is enabled (SCLWSDIS bit at ‘0’). If slave clock stretching is disabled (SCLWSDIS bit at ‘1’), the peripheral clock must run at a minimum of 11 MHz (assuming the system has no latency).

Note: When slave clock stretching is disabled, the TWIHS_RHR must always be read before receiving the next data (MASTER write frame). It is strongly recommended to use either the polling method on the RXRDY flag in TWIHS_SR, or the DMA. If the receive is managed by an interrupt, the TWIHS interrupt priority must be set to the right level and its latency minimized to avoid receive overrun.

Note: When slave clock stretching is disabled, the TWIHS_THR must be filled with the first data to send before the beginning of the frame (MASTER read frame). It is strongly recommended to use either the polling method on the TXRDY flag in TWIHS_SR, or the DMA. If the transmit is managed by an interrupt, the TWIHS interrupt priority must be set to the right level and its latency minimized to avoid transmit underrun.

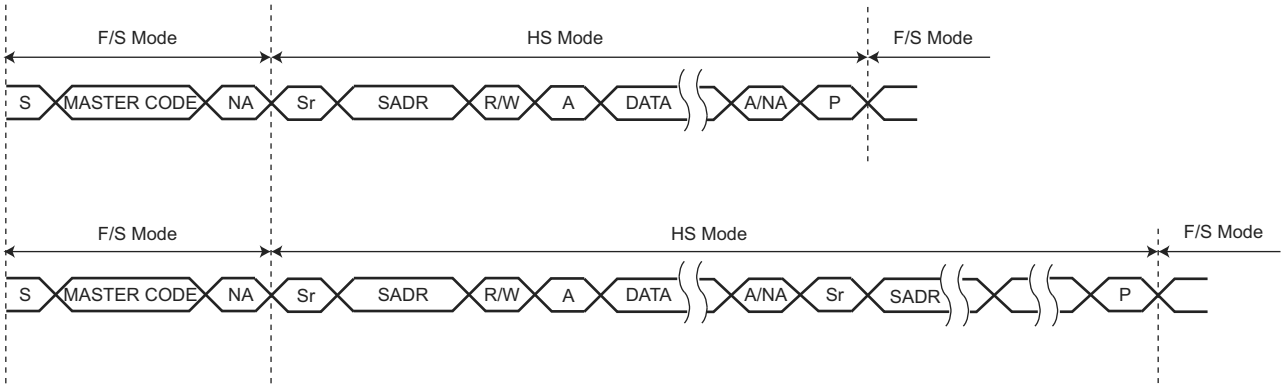
- Read/Write Operation

A TWIHS high-speed frame always begins with the following sequence:

1. START condition (S)
2. Master Code (0000 1XXX)
3. Not-acknowledge (NACK)

When the TWIHS is programmed in Slave mode and TWIHS High-speed mode is activated, master code matching is activated and internal timings are set to match the TWIHS High-speed mode requirements.

Figure 46-43: High-Speed Mode Read/Write



- Usage

TWIHS High-speed mode usage is the same as the standard TWIHS (See Section 46.6.3.14 “Read/Write Flowcharts”).

46.6.5.8 Alternative Command

In Slave mode, Alternative Command mode is useful when SMBus mode is enabled to send or check the PEC byte.

Alternative Command mode is enabled by setting the ACMEN bit of the TWIHS Control Register and the transfer is configured in TWIHS_ACR.

For a combined transfer with PEC, only the NPEC bit in TWIHS_ACR must be set as the PEC byte is sent once at the end of the frame.

See Section 46.6.5.10 “Slave Read Write Flowcharts” for detailed flowcharts.

46.6.5.9 Asynchronous Partial Wakeup (SleepWalking)

The TWIHS includes an asynchronous start condition detector. It is capable of waking the device up from a Sleep mode upon an address match (and optionally an additional data match), including Sleep modes where the TWIHS peripheral clock is stopped.

After detecting the START condition on the bus, the TWIHS stretches TWCK until the TWIHS peripheral clock has started. The time required for starting the TWIHS depends on which Sleep mode the device is in. After the TWIHS peripheral clock has started, the TWIHS releases its TWCK stretching and receives one byte of data (slave address) on the bus. At this time, only a limited part of the device, including the TWIHS module, receives a clock, thus saving power. If the address phase causes a TWIHS address match (and, optionally, if the first data byte causes data match as well), the entire device is woken up and normal TWIHS address matching actions are performed. Normal TWIHS transfer then follows. If the TWIHS is not addressed (or if the optional data match fails), the TWIHS peripheral clock is automatically stopped and the device returns to its original Sleep mode.

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	SMBHHM	SMBDAM	PECERR	TOUT	–	MCACK

15	14	13	12	11	10	9	8
–	–	–	–	EOSACC	SCL_WS	ARBLST	NACK

7	6	5	4	3	2	1	0
UNRE	OVRE	GACC	SVACC	–	TXRDY	RXRDY	TXCOMP

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

TXCOMP: Transmission Completed Interrupt Disable

RXRDY: Receive Holding Register Ready Interrupt Disable

TXRDY: Transmit Holding Register Ready Interrupt Disable

SVACC: Slave Access Interrupt Disable

GACC: General Call Access Interrupt Disable

OVRE: Overrun Error Interrupt Disable

UNRE: Underrun Error Interrupt Disable

NACK: Not Acknowledge Interrupt Disable

ARBLST: Arbitration Lost Interrupt Disable

SCL_WS: Clock Wait State Interrupt Disable

EOSACC: End Of Slave Access Interrupt Disable

MCACK: Master Code Acknowledge Interrupt Disable

TOUT: Timeout Error Interrupt Disable

PECERR: PEC Error Interrupt Disable

SMBDAM: SMBus Default Address Match Interrupt Disable

SMBHHM: SMBus Host Header Address Match Interrupt Disable

47.10.4 USART Control Register

Name: FLEX_US_CR

Address: 0xF8034200 (0), 0xF8038200 (1), 0xFC010200 (2), 0xFC014200 (3), 0xFC018200 (4)

Access: Write-only

31	30	29	28	27	26	25	24
FIFODIS	FIFOEN	–	REQCLR	–	TXFLCLR	RXFCLR	TXFCLR
23	22	21	20	19	18	17	16
–	–	LINWKUP	LINABT	RTSDIS	RTSEN	–	–
15	14	13	12	11	10	9	8
RETTO	RSTNACK	RSTIT	SENDA	STTTO	STPBRK	STTBRK	RSTSTA
7	6	5	4	3	2	1	0
TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX	–	–

For SPI control, see Section 47.10.5 ”USART Control Register (SPI_MODE)”.

RSTRX: Reset Receiver

0: No effect.

1: Resets the receiver.

RSTTX: Reset Transmitter

0: No effect.

1: Resets the transmitter.

RXEN: Receiver Enable

0: No effect.

1: Enables the receiver, if RXDIS is 0.

RXDIS: Receiver Disable

0: No effect.

1: Disables the receiver.

TXEN: Transmitter Enable

0: No effect.

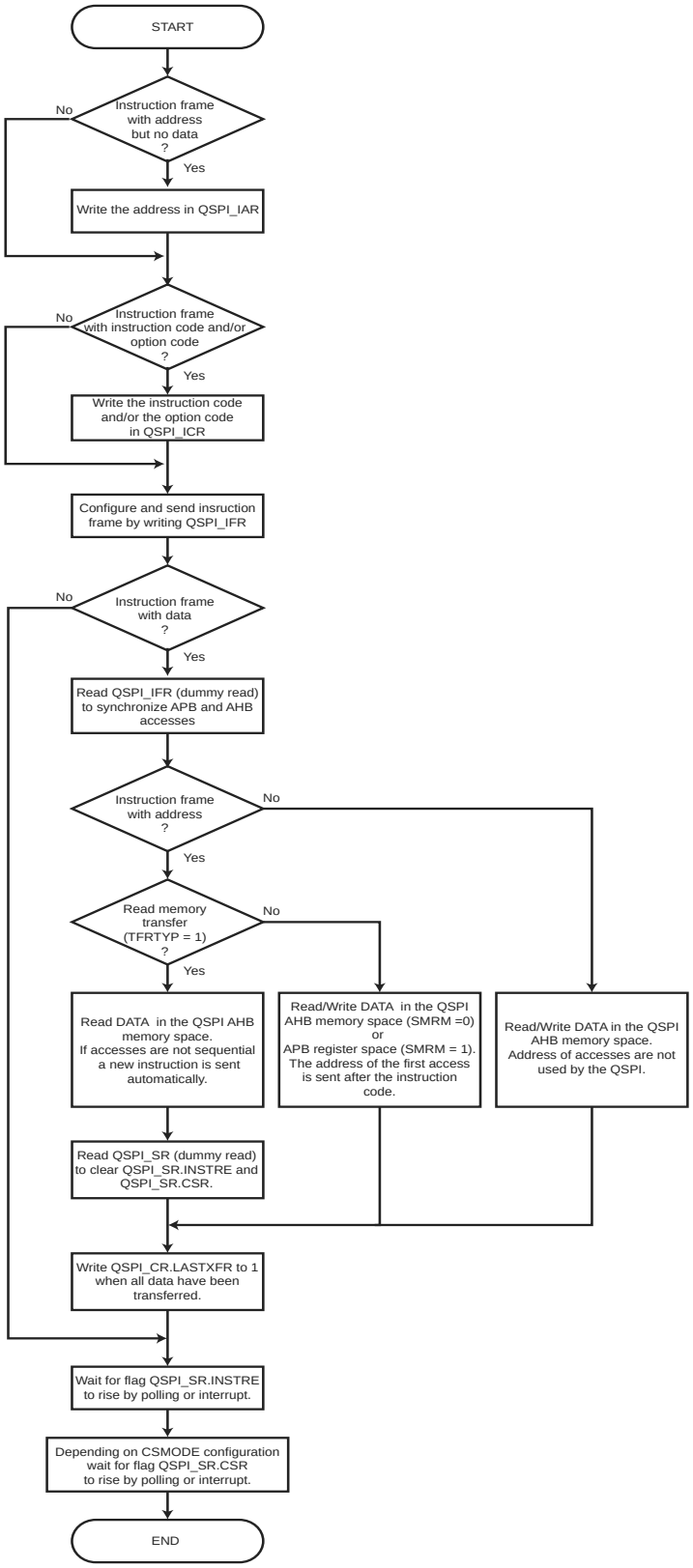
1: Enables the transmitter if TXDIS is 0.

TXDIS: Transmitter Disable

0: No effect.

1: Disables the transmitter.

Figure 50-9: Instruction Transmission Flow Diagram



53.6.2 MCAN Endian Register

Name: MCAN_ENDN

Address: 0xF8054004 (0), 0xFC050004 (1)

Access: Read-only

31	30	29	28	27	26	25	24
ETV							
23	22	21	20	19	18	17	16
ETV							
15	14	13	12	11	10	9	8
ETV							
7	6	5	4	3	2	1	0
ETV							

ETV: Endianness Test Value

The endianness test value is 0x87654321.

61.5.9 SHA Input Data x Register

Name: SHA_IDATARx [x=0..15]

Address: 0xF0028040

Access: Write-only

31	30	29	28	27	26	25	24
IDATA							

23	22	21	20	19	18	17	16
IDATA							

15	14	13	12	11	10	9	8
IDATA							

7	6	5	4	3	2	1	0
IDATA							

IDATA: Input Data

The 32-bit Input Data registers allow to load the data block used for hash processing.

These registers are write-only to prevent the input data from being read by another application.

SHA_IDATAR0 corresponds to the first word of the block, SHA_IDATAR15 to the last word of the last block in case SHA algorithm is set to SHA1, SHA224, SHA256 or SHA_IODATA15R to the last word of the block if SHA algorithm is SHA384 or SHA512 (see Section 61.5.10 “SHA Input/Output Data Register x”).

66.22 PDMIC Timings

66.22.1 Timing Conditions

Timings assuming capacitance loads are given in Table 66-86.

Table 66-86: Capacitance Load

Supply	Corner	
	Max	Min
3.3V	30 pF	5 pF
1.8V	20 pF	5 pF

66.22.2 Timing Extraction

Figure 66-39: PDMIC Timing Diagram

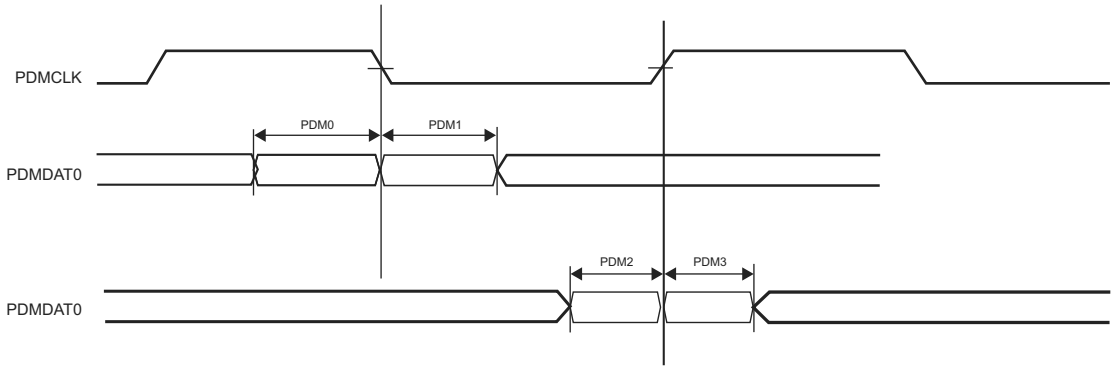


Table 66-87: PDMIC IOSET1 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
$PDMIC_0$	DATA setup time right	3.5	–	3.5	–	ns
$PDMIC_1$	DATA hold time right	3.1	–	3.5	–	ns
$PDMIC_2$	DATA setup time left	3.5	–	3.5	–	ns
$PDMIC_3$	DATA hold time left	3.1	–	3.5	–	ns

Table 66-88: PDMIC IOSET2 Timings

Symbol	Power Supply / Parameter	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
$PDMIC_0$	DATA setup time right	4.2	–	4.2	–	ns
$PDMIC_1$	DATA hold time right	2	–	2	–	ns
$PDMIC_2$	DATA setup time left	4.2	–	4.2	–	ns
$PDMIC_3$	DATA hold time left	2	–	2	–	ns

Table 68-1: Power Supply Connections (Continued)

Signal Name	Recommended Pin Connection	Description
VDDFUSE	2.25V to 2.75V Decoupling capacitor (100 nF)(1)(2)	Powers the fuse box for programming. VDDFUSE must not be left floating.
VDDAUDIOPLL	3.0V to 3.6V Decoupling capacitor (100 nF)(1)(2)	Powers the Audio PLL.
GNDCORE	Core Chip ground	GNDCORE pins are common to VDDCORE pins. GNDCORE pins should be connected as shortly as possible to the system ground plane.
GNDPLLA	PLLA cell ground	GNDPLL pin is provided for VDDPLLA pins. GNDPLL pin should be connected as shortly as possible to the system ground plane.
GNDIODDR	DDR2/LPDDR1/LPDDR2/DDR3/LPDDR3 interface I/O lines ground	GNDIODDR pins should be connected as shortly as possible to the system ground plane.
GNDISC	VDDISC ground	GNDISC pins are common to VDDISC pins. GNDISC pins should be connected as shortly as possible to the system ground plane.
GNDIOP0,1,2	Peripherals and ISC I/O lines ground	GNDIOPx pins are common to VDDIOPx pins. GNDIOP pins should be connected as shortly as possible to the system ground plane.
GNDBU	Backup ground	GNDBU pin is provided for VDDBU pins. GNDBU pin should be connected as shortly as possible to the system ground plane.
GNDUTMIC	VDDUTMIC and VDDHSIC ground	GNDUTMIC pins are common to VDDUTMIC and VDDHSIC pins. GNDUTMIC pins should be connected as shortly as possible to the system ground plane.
GNDUTMII	UDPHS and UHPHS UTMI+ Core and Interface, and PLL UTMI ground	GNDUTMII pins are common to VDDUTMII and VDDUTMIC pins. GNDUTMII pins should be connected as shortly as possible to the system ground plane.
GNDOSC	Oscillator ground	GNDOSC pin is provided for VDDOSC pins. GNDOSC pin should be connected as shortly as possible to the system ground plane.
GNDSDMMC	SDMMC ground	SDMMC pins are common to VDDSDMMC pins. GNDSDMMC pins should be connected as shortly as possible to the system ground plane.
GNDANA	Analog ground	GNDANA pins are common to VDDANA pins. GNDANA pins should be connected as shortly as possible to the system ground plane.
GNDFUSE	Fuse box ground	GNDFUSE pins are common to VDDFUSE pins. GNDFUSE pins should be connected as shortly as possible to the system ground plane.