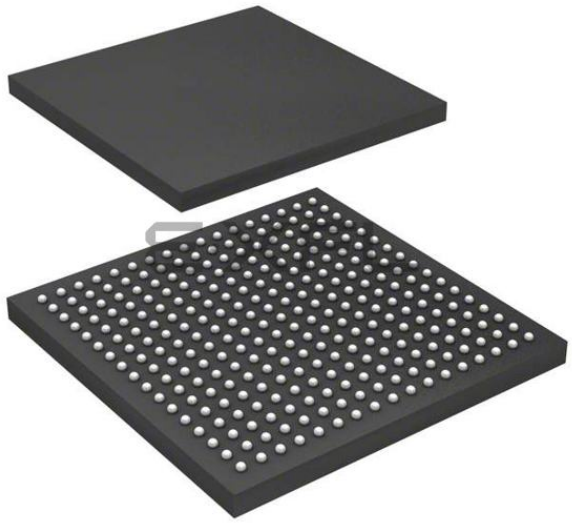

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d28b-cnr

Value	Name	Description
0x4	RESERVED	Reserved
0x5	RESERVED	Reserved
0x6	RESERVED	Reserved
0x7	RESERVED	Reserved

EMBEN: Event Monitor Bus Enable

0: Disabled. This is the default value.

1: Enabled.

PEN: Parity Enable

0: Disabled. This is the default value.

1: Enabled.

SAOEN: Shared Attribute Override Enable

0: Treats shared accesses. This is the default value.

1: Shared attribute is internally ignored.

FWA: Force Write Allocate

0: The L2 Cache controller uses AWCACHE attributes for WA. This is the default value.

1: User forces no allocate, WA bit must be set to 0.

2: User overrides AWCACHE attributes, WA bit must be set to 1. All cacheable write misses become write allocated.

3: The write allocation is internally mapped to 00.

CRPOL: Cache Replacement Policy

0: Pseudo-random replacement using the LFSR algorithm.

1: Round-robin replacement. This is always the default value.

NSLEN: Non-Secure Lockdown Enable

0: Lockdown registers cannot be modified using non-secure accesses. This is the default value.

1: Non-secure accesses can write to the lockdown registers.

NSIAC: Non-Secure Interrupt Access Control

0: Interrupt Clear Register and Interrupt Mask Register can only be modified or read with secure accesses. This is the default value.

1: Interrupt Clear Register and Interrupt Mask Register can be modified or read with secure or non-secure accesses.

DPEN: Data Prefetch Enable

0: Data prefetching is disabled. This is the default value.

1: Data prefetching is enabled.

IPEN: Instruction Prefetch Enable

0: Instruction prefetching is disabled. This is the default value.

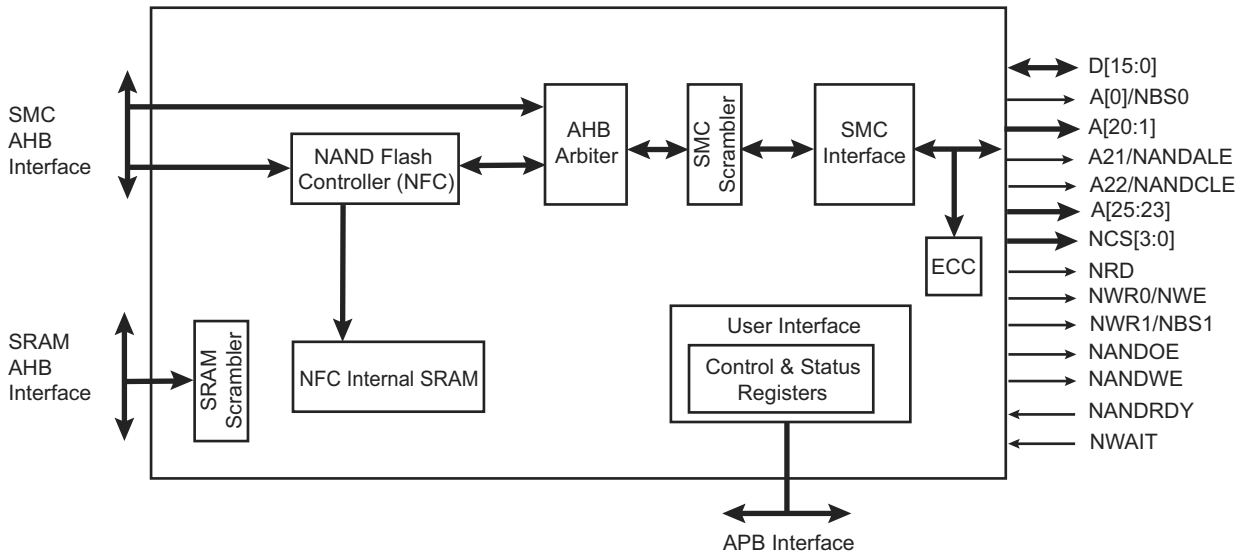
1: Instruction prefetching is enabled.

37.2 Embedded Characteristics

- 64-Mbyte Address Space per Chip Select
- 8- or 16-bit Data Bus
- Word, Halfword, Byte Transfers
- Byte Write or Byte Select Lines
- Programmable Setup, Pulse and Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse and Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- External Data Bus Scrambling/Unscrambling Function
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Hardware Configurable Number of Chip Selects from 1 to 4
- Programmable Timing on a per Chip Select Basis
- NAND Flash Controller Supporting NAND Flash with Multiplexed Data/Address Buses
- Supports SLC and MLC NAND Flash Technology
- Supports NAND Flash Devices with 8 or 16-bit Data Paths
- Multibit Error Correcting Code (ECC) supporting NAND Flash devices with 8-bit only Data Path
- ECC Algorithm Based on Binary Shortened Bose, Chaudhuri and Hocquenghem (BCH) Codes
- Programmable Error Correcting Capability: 2, 4, 8, 12, 24 and 32 bits of Errors per Block
- 9 Kbytes NFC SRAM
- Programmable Block Size: 512 bytes or 1024 bytes
- Programmable Number of Block per Page: 1, 2, 4 or 8 Blocks of Data per Page
- Programmable Spare Area Size up to 512 bytes
- Supports Spare Area ECC Protection
- Supports 8 Kbytes Page Size Using 1024 bytes/block and 4 Kbytes Page Size Using 512 bytes/block
- Multibit Error Detection Is Interrupt Driven
- Provides Hardware Acceleration for Determining Roots of Polynomials Defined over a Finite Field
- Programmable Finite Field GF(2^13) or GF(2^14)
- Finds Roots of Error-locator Polynomial
- Programmable Number of Roots
- Register Write Protection

37.3 Block Diagram

Figure 37-1: Block Diagram



38.9.19 XDMAC Channel x [x = 0..15] Interrupt Disable Register

Name: XDMAC_CIDx [x = 0..15]

Address: 0xF0004054 (1)[0], 0xF0004094 (1)[1], 0xF00040D4 (1)[2], 0xF0004114 (1)[3], 0xF0004154 (1)[4], 0xF0004194 (1)[5], 0xF00041D4 (1)[6], 0xF0004214 (1)[7], 0xF0004254 (1)[8], 0xF0004294 (1)[9], 0xF00042D4 (1)[10], 0xF0004314 (1)[11], 0xF0004354 (1)[12], 0xF0004394 (1)[13], 0xF00043D4 (1)[14], 0xF0004414 (1)[15], 0xF0010054 (0)[0], 0xF0010094 (0)[1], 0xF00100D4 (0)[2], 0xF0010114 (0)[3], 0xF0010154 (0)[4], 0xF0010194 (0)[5], 0xF00101D4 (0)[6], 0xF0010214 (0)[7], 0xF0010254 (0)[8], 0xF0010294 (0)[9], 0xF00102D4 (0)[10], 0xF0010314 (0)[11], 0xF0010354 (0)[12], 0xF0010394 (0)[13], 0xF00103D4 (0)[14], 0xF0010414 (0)[15]

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	ROID	WBEID	RBEID	FID	DID	LID	BID

BID: End of Block Interrupt Disable Bit

0: No effect.

1: Disables end of block interrupt.

LID: End of Linked List Interrupt Disable Bit

0: No effect.

1: Disables end of linked list interrupt.

DID: End of Disable Interrupt Disable Bit

0: No effect.

1: Disables end of disable interrupt.

FID: End of Flush Interrupt Disable Bit

0: No effect.

1: Disables end of flush interrupt.

RBEID: Read Bus Error Interrupt Disable Bit

0: No effect.

1: Disables bus error interrupt.

WBEID: Write Bus Error Interrupt Disable Bit

0: No effect.

1: Disables bus error interrupt.

ROID: Request Overflow Error Interrupt Disable Bit

0: No effect.

1: Disables request overflow error interrupt.

39.7.73 Overlay 2 Configuration Register 7

Name: LCDC_OVR2CFG7

Address: 0xF0000288

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
RKEY							

15	14	13	12	11	10	9	8
GKEY							

7	6	5	4	3	2	1	0
BKEY							

RKEY: Red Color Component Chroma Key

Reference Red chroma key used to match the Red color of the current overlay.

GKEY: Green Color Component Chroma Key

Reference Green chroma key used to match the Green color of the current overlay.

BKEY: Blue Color Component Chroma Key

Reference Blue chroma key used to match the Blue color of the current overlay.

39.7.100 High-End Overlay Configuration Register 5

Name: LCDC_HEOCFG5

Address: 0xF00003A0

Access: Read/Write

31	30	29	28	27	26	25	24
XSTRIDE							

23	22	21	20	19	18	17	16
XSTRIDE							

15	14	13	12	11	10	9	8
XSTRIDE							

7	6	5	4	3	2	1	0
XSTRIDE							

XSTRIDE: Horizontal Stride

XSTRIDE represents the memory offset, in bytes, between two rows of the image memory.

3: The index range for the following registers is from 1 to 2:
- GMAC_ISRPQ
- GMAC_TBQBAPQ
- GMAC_RBQBAPQ
- GMAC_RBSRPQ
- GMAC_IERPQ (cont'd.)
- GMAC_IDRPQ
- GMAC_IMRPQ

4: The index for GMAC_ST1RPQ registers ranges from 0 to 3.

5: The index for GMAC_ST2RPQ registers ranges from 0 to 7.

6: The index for GMAC_ST2ER registers ranges from 0 to 3.

7: The index for GMAC_ST2CW0 and GMAC_ST2CW1 registers ranges from 0 to 23.

42.7 USB Host High Speed Port (UHPHS) User Interface

The Enhanced USB Host Controller contains two sets of software-accessible hardware registers – Memory-mapped Host Controller Registers and optional PCI configuration registers. Note that the PCI configuration registers are only needed for PCI devices that implement the Host Controller.

- Memory-mapped USB Host Controller Registers. This block of registers is memory-mapped into non-cacheable memory. This memory space must begin on a DWord (32-bit) boundary. This register space is divided into two sections: a set of read-only capability registers and a set of read/write operational registers. Table 42-1 describes each register space.

Table 42-1: Enhanced Interface Register Sets

Offset	Register Set	Explanation
0 to N-1	Capability Registers	The capability registers specify the limits, restrictions, and capabilities of a host controller implementation. These values are used as parameters to the host controller driver.
N to N+M-1	Operational Registers	The operational registers are used by system software to control and monitor the operational state of the host controller.

Note: Host controllers are not required to support exclusive-access mechanisms (such as PCI LOCK) for accesses to the memory-mapped register space. Therefore, if software attempts exclusive-access mechanisms to the host controller memory-mapped register space, the results are undefined.

- PCI Configuration Registers (for PCI devices). In addition to the normal PCI header, power management, and device-specific registers, two registers are needed in the PCI configuration space to support USB. The normal PCI header and device-specific registers are beyond the scope of this document (the UHPHS_CLASSC register is shown in this document). Note that HCD does not interact with the PCI configuration space. This space is used only by the PCI enumerator to identify the USB Host Controller, and assign the appropriate system resources.

Table 42-2: Register Mapping

Offset	Register	Name	Access	Reset
Host Controller Capability Registers				
0x00	UHPHS Host Controller Capability Register	UHPHS_HCCAPBASE	Read-only	0x0100 0010
0x04	UHPHS Host Controller Structural Parameters Register	UHPHS_HCSPARAMS	Read-only	0x0000 1116
0x08	UHPHS Host Controller Capability Parameters Register	UHPHS_HCCPARAMS	Read-only	0x0000 A010
0x0C	Reserved	–	–	–
Host Controller Operational Registers				
0x10	UHPHS USB Command Register	UHPHS_USBCMD	Read/Write(1)	0x0008 0000 or 0x0008 0B00(2)
0x14	UHPHS USB Status Register	UHPHS_USBSTS	Read/Write(1)	0x0000 1000
0x18	UHPHS USB Interrupt Enable Register	UHPHS_USBINTR	Read/Write	0x0000 0000
0x1C	UHPHS USB Frame Index Register	UHPHS_FRINDEX	Read/Write	0x0000 0000
0x20	UHPHS Control Data Structure Segment Register	UHPHS_CTRLDSSEGMENT	Read/Write	0x0000 0000
0x24	UHPHS Periodic Frame List Base Address Register	UHPHS_PERIODICLISTBASE	Read/Write	0x0000 0000
0x28	UHPHS Asynchronous List Address Register	UHPHS_ASYNCLISTADDR	Read/Write	0x0000 0000
0x2C - 0x4F	Reserved	–	–	–

47.10.30 USART Manchester Configuration Register

Name: FLEX_US_MAN

Address: 0xF8034250 (0), 0xF8038250 (1), 0xFC010250 (2), 0xFC014250 (3), 0xFC018250 (4)

Access: Read/Write

31	30	29	28	27	26	25	24
RXIDLEV	DRIFT	ONE	RX_MPOL	–	–	RX_PP	

23	22	21	20	19	18	17	16
–	–	–	–	RX_PL			

15	14	13	12	11	10	9	8
–	–	–	TX_MPOL	–	–	TX_PP	

7	6	5	4	3	2	1	0
–	–	–	–	TX_PL			

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

TX_PL: Transmitter Preamble Length

0: The transmitter preamble pattern generation is disabled

1–15: The preamble length is TX_PL × Bit Period

TX_PP: Transmitter Preamble Pattern

The following values assume that TX_MPOL field is not set:

Value	Name	Description
0	ALL_ONE	The preamble is composed of ‘1’s
1	ALL_ZERO	The preamble is composed of ‘0’s
2	ZERO_ONE	The preamble is composed of ‘01’s
3	ONE_ZERO	The preamble is composed of ‘10’s

TX_MPOL: Transmitter Manchester Polarity

0: Logic zero is coded as a zero-to-one transition, Logic one is coded as a one-to-zero transition.

1: Logic zero is coded as a one-to-zero transition, Logic one is coded as a zero-to-one transition.

RX_PL: Receiver Preamble Length

0: The receiver preamble pattern detection is disabled

1–15: The detected preamble length is RX_PL × Bit Period

RX_PP: Receiver Preamble Pattern detected

The following values assume that RX_MPOL field is not set:

Value	Name	Description
0	ALL_ONE	The preamble is composed of ‘1’s
1	ALL_ZERO	The preamble is composed of ‘0’s
2	ZERO_ONE	The preamble is composed of ‘01’s
3	ONE_ZERO	The preamble is composed of ‘10’s

RX_MPOL: Receiver Manchester Polarity

FSDIS: Frame Slot Mode Disable

0: The Frame Slot mode is enabled.

1: The Frame Slot mode is disabled.

WKUPTYP: Wakeup Signal Type

0: Setting the LINWKUP bit in the control register sends a LIN 2.0 wakeup signal.

1: Setting the LINWKUP bit in the control register sends a LIN 1.3 wakeup signal.

DLC: Data Length Control

0–255: Defines the response data length if DLM = 0,in that case the response data length is equal to DLC+1 bytes.

PDCM: DMAC Mode

0: The LIN mode register FLEX_US_LINMR is not written by the DMAC.

1: The LIN mode register FLEX_US_LINMR (excepting that flag) is written by the DMAC.

SYNCDIS: Synchronization Disable

0: The synchronization procedure is performed in LIN slave node configuration.

1: The synchronization procedure is not performed in LIN slave node configuration.

BITS: Bits Per Transfer

(See “Note” following the register table in Section 49.8.12 “SPI Chip Select Register”.)

The BITS field determines the number of data bits transferred. Reserved values should not be used.

Value	Name	Description
0	8_BIT	8 bits for transfer
1	9_BIT	9 bits for transfer
2	10_BIT	10 bits for transfer
3	11_BIT	11 bits for transfer
4	12_BIT	12 bits for transfer
5	13_BIT	13 bits for transfer
6	14_BIT	14 bits for transfer
7	15_BIT	15 bits for transfer
8	16_BIT	16 bits for transfer
9	–	Reserved
10	–	Reserved
11	–	Reserved
12	–	Reserved
13	–	Reserved
14	–	Reserved
15	–	Reserved

SCBR: Serial Clock Bit Rate

In Master mode, the SPI Interface uses a modulus counter to derive the SPCK bit rate from the clock defined by SPI_MR.BRSRCCLK bit. The bit rate is selected by writing a value from1 to 255 in the SCBR field. The following equations determine the SPCK bit rate:

If SPI_MR.BRSRCCLK = 0: SCBR = $f_{peripheral\ clock}$ / SPCK Bit Rate

If SPI_MR.BRSRCCLK = 1: SCBR = f_{GCLK} / SPCK Bit Rate

Programming the SCBR field to 0 is forbidden. Triggering a transfer while SCBR is at 0 can lead to unpredictable results.

If BRSRCCLK = 1 in SPI_MR, SCBR must be programmed with a value greater than 1.

At reset, SCBR is 0 and the user has to program it at a valid value before performing the first transfer.

Note: If one of the SCBR fields in SPI_CSRx is set to 1, the other SCBR fields in SPI_CSRx must be set to 1 as well, if they are used to process transfers. If they are not used to transfer data, they can be set at any value.

DLYBS: Delay Before SPCK

This field defines the delay from NPCS falling edge (activation) to the first valid SPCK transition.

When DLYBS = 0, the delay is half the SPCK clock period.

Otherwise, the following equations determine the delay:

If SPI_MR.BRSRCCLK = 0: DLYBS = Delay Before SPCK × $f_{peripheral\ clock}$

If SPI_MR.BRSRCCLK = 1: DLYBS = Delay Before SPCK × f_{GCLK}

DLYBCT: Delay Between Consecutive Transfers

This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT = 0, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers.

Otherwise, the following equations determine the delay:

FCD: e.MMC Force Card Detect

When using e.MMC, the user can set this bit to 1 to bypass the card detection procedure using the SDMMC_CD signal.

0(DISABLED): e.MMC Forced Card Detect is disabled. The SDMMC_CD signal is used and debounce timing is applied.

1(ENABLED): e.MMC Forced Card Detect is enabled.

52. Image Sensor Controller (ISC)

52.1 Description

The Image Sensor Controller (ISC) system manages incoming data from a parallel sensor. It supports a single active interface. The parallel interface protocol can use a free-running clock or a gated clock strategy. It supports the ITU-R BT 656/1120 422 protocol with a data width of 8 bits or 10 bits and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12 bits to 10 bits compression, programmable color space conversion, horizontal and vertical chrominance subsampling module. The module also integrates a triple channel direct memory access controller master interface.

52.2 Embedded Characteristics

- Parallel 12-bit Interface for Raw Bayer, YCbCr, Monochrome and JPEG Compressed Sensor Interface
- BT.601/656/1120 Video Interface Supported
- Progressive Systems and Segmented Frame Systems
- Raw Bayer, YCbCr, Luminance (Black and White) Pixel Format Supported
- Resolution up to 2592 x 1944
- Input Pixel Clock up to 96 MHz
- Output Master Clock Generation
- Cropping
- Adjustable White Balance
- Raw Bayer Color Filter Array Interpolation
- Color Correction
- Gamma Correction
- Color Space Conversion
- Contrast and Brightness Control
- 4:4:4 to 4:2:2 Subsampler
- 4:2:2 to 4:2:0 Subsampler
- Rounding, Limiting and Packing unit
- Histogram Generation
- System Interface: Direct Memory Access Interface with Packed, Semi Planar and Planar output format
- Output Memory Format: 16 bpp RGB, 32 bpp RGB, 16 bpp, YCbCr 444, YCbCr 422, YCbCr 420, up to 12-bit raw Bayer

52.6.41 ISC Contrast And Brightness Control Register

Name: ISC_CBC_CTRL

Address: 0xF00083B4

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

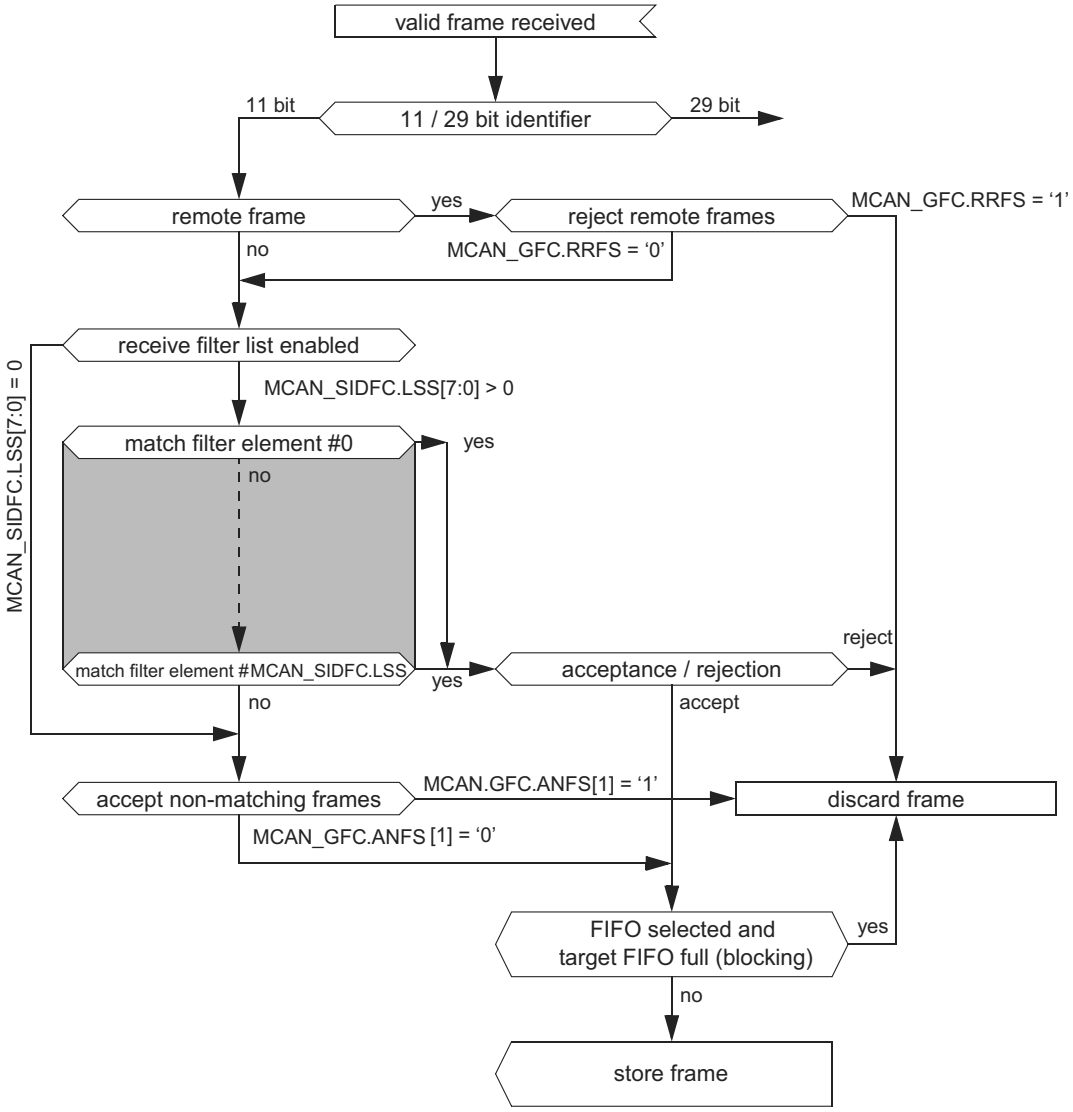
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ENABLE

ENABLE: Contrast and Brightness Control Enable

0: Contrast and brightness control is disabled.

1: Contrast and brightness control is enabled.

Figure 53-5: Standard Message ID Filter Path



54.7.7 TC Register A

Name: TC_RAx [x=0..2]

Address: 0xF800C014 (0)[0], 0xF800C054 (0)[1], 0xF800C094 (0)[2], 0xF8010014 (1)[0], 0xF8010054 (1)[1], 0xF8010094 (1)[2]

Access: Read-only if TC_CMRx.WAVE = 0, Read/Write if TC_CMRx.WAVE = 1

31	30	29	28	27	26	25	24
RA							

23	22	21	20	19	18	17	16
RA							

15	14	13	12	11	10	9	8
RA							

7	6	5	4	3	2	1	0
RA							

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

RA: Register A

RA contains the Register A value in real time.

60.5.9 AES Output Data Register x

Name: AES_ODATARx [x=0..3]

Address: 0xF002C050

Access: Read-only

31	30	29	28	27	26	25	24
ODATA							

23	22	21	20	19	18	17	16
ODATA							

15	14	13	12	11	10	9	8
ODATA							

7	6	5	4	3	2	1	0
ODATA							

ODATA: Output Data

The four 32-bit Output Data registers contain the 128-bit data block that has been encrypted/decrypted.

AES_ODATAR0 corresponds to the first word, AES_ODATAR3 to the last one.

65.5.2 Interrupt Sources

The ADC interrupt line is connected on one of the internal sources of the Interrupt Controller. Using the ADC interrupt requires the interrupt controller to be programmed first.

Table 65-2: Peripheral IDs

Instance	ID
ADC	40

65.5.3 I/O Lines

The digital input ADTRG is multiplexed with digital functions on the I/O line and the selection of ADTRG is made using the PIO controller.

The analog inputs ADC_ADx are multiplexed with digital functions on the I/O lines. ADC_ADx inputs are selected as inputs of the ADCC when writing a one in the corresponding CHx bit of ADC_CHER and the digital functions are not selected.

Table 65-3: I/O Lines

Instance	Signal	I/O Line	Peripheral
ADC	ADTRG	PD31	A
ADC	AD0	PD19	X1
ADC	AD1	PD20	X1
ADC	AD2	PD21	X1
ADC	AD3	PD22	X1
ADC	AD4	PD23	X1
ADC	AD5	PD24	X1
ADC	AD6	PD25	X1
ADC	AD7	PD26	X1
ADC	AD8	PD27	X1
ADC	AD9	PD28	X1
ADC	AD10	PD29	X1
ADC	AD11	PD30	X1

65.5.4 Hardware Triggers

The ADC can use internal signals to start conversions. See the ADC_MR.TRGSEL field description in **Section 65.7.2 “ADC Mode Register”** for exact wiring of internal triggers.

65.5.5 Fault Output

The ADC Controller has the FAULT output connected to the FAULT input of PWM. See Section 65.6.18 “Fault Event” and section “Pulse Width Modulation Controller (PWM)”.

When TSMODE = 1 or 3, each trigger event adds two half-words in the buffer (assuming TSAV = 0), first half-word being XPOS of ADC_XPOSR then YPOS of ADC_YPOSR. If TSAV/TSFREQ ≠ 0, the data structure remains unchanged. Not all trigger events add data to the buffer.

When TSMODE = 2, each trigger event adds four half-words to the buffer (assuming TSAV = 0), first half-word being XPOS of ADC_XPOSR followed by YPOS of ADC_YPOSR and finally Z1 followed by Z2, both located in ADC_PRESSR.

When TAG is set (ADC_EMR), the CHNB field (four most significant bits of ADC_LCDR) is cleared when XPOS is transmitted and set when YPOS is transmitted, allowing an easier post-processing of the buffer or a better checking of the buffer integrity. In case 4-wire with Pressure mode is selected, Z1 value is transmitted to the buffer along with tag set to 2 and Z2 is tagged with value 3.

XSCALE and YSCALE (calibration values) are not transmitted to the buffer because they are supposed to be constant and moreover only measured at the very first startup of the controller or upon user request.

There is no change in buffer structure whatever the value of PENDET bit configuration in ADC_TSMR but it is recommended to use the pen detection function for buffer post-processing (see Section 65.6.17.4 “Pen Detection Status”).

Table 66-84: SSC1 IOSET1 Timings

Symbol	Power supply / Parameter	Conditions	1.8V Min	1.8V Max	3.3V Min	3.3V Max	Unit
Transmitter							
SSC_0	TK edge to TF/TD (TK output, TF output) (1)	–	0	2.6	0	2.7	ns
SSC_1	TK edge to TF/TD (TK input, TF output) (1)	–	3.6	12.7	3	10.9	ns
SSC_2	TF setup time before TK edge (TK output)	–	13.4	–	11.2	–	ns
SSC_3	TF hold time after TK edge (TK output)	–	0	–	0	–	ns
SSC_4	TK edge to TF/TD (TK output, TF input) (1)	–	0	2.1	0	2	ns
		STTDLY = 0 START = 4, 5 or 7	$2 \times t_{CPMCK}$	2.1 + $(2 \times t_{CPMCK})$	$2 \times t_{CPMCK}$	2 + $(2 \times t_{CPMCK})$	ns
SSC_5	TF setup time before TK edge (TK input)	–	0	–	0	–	
SSC_6	TF hold time after TK edge (TK input)	–	t_{CPMCK}	–	t_{CPMCK}	–	
SSC_7	TK edge to TF/TD (TK input, TF input) (1)	–	3.6	12.2	3	10.2	
		STTDLY = 0 START = 4, 5 or 7	3.6 + $(3 \times t_{CPMCK})$	12.2 + $(3 \times t_{CPMCK})$	3 + $(3 \times t_{CPMCK})$	10.2 + $(3 \times t_{CPMCK})$	
Receiver							
SSC_8	RF/RD setup time before RK edge (RK input)	–	0	–	0	–	ns
SSC_9	RF/RD hold time after RK edge (RK input)	–	t_{CPMCK}	–	t_{CPMCK}	–	ns
SSC_{10}	RK edge to RF (RK input) (1)	–	3.4	11.8	2.7	9.9	ns
SSC_{11}	RF/RD setup time before RK edge (RK output)	–	12.2 - t_{CPMCK}	–	10.3 - t_{CPMCK}	–	ns
SSC_{12}	RF/RD hold time after RK edge (RK output)	–	t_{CPMCK}	–	t_{CPMCK}	–	ns
SSC_{13}	RK edge to RF (RK output) (1)	–	0	3.3	0	3.4	ns

Note 1: For output signals (TF, TD, RF), minimum and maximum access times are defined. The minimum access time is the time between the TK (or RK) edge and the signal change. The maximum access time is the time between the TK edge and the signal stabilization. Figure 66-38 illustrates the minimum and maximum accesses for SSC_0. The same applies for SSC_1, SSC_4, SSC_7, SSC_{10} and SSC_{13}.

71. Errata

Errata is described in the following sections:

- Section 71.1 “Errata - SAMA5D2 MRL C Parts”
- Section 71.2 “Errata - SAMA5D2 MRL B Parts”
- Section 71.3 “Errata - SAMA5D2 MRL A Parts”

71.1 Errata - SAMA5D2 MRL C Parts

This section describes errata relevant to the devices listed in Table 71-2.

Table 71-1: SAMA5D2 MRL C Parts

Device Name
ATSAMA5D21C
ATSAMA5D22C
ATSAMA5D23C
ATSAMA5D24C
ATSAMA5D26C
ATSAMA5D27C
ATSAMA5D28C

71.1.1 GMAC Timestamps and PTP packets

Issue: Bad association of timestamps and the PTP packets

An issue in the association mechanism between event registers and queued PTP packets may lead to timestamps incorrectly associated with these packets.

Even if it is highly unlikely to queue consecutive packets of the same type, there is no way to know to which frame the content of the PTP event registers refers.

Workaround: None

71.1.2 SDMMC software ‘Reset for All’ Command

Issue: Software ‘Reset for All’ command is not guaranteed

The software ‘Reset for All’ command is not guaranteed, and some registers of the host controller may not properly reset. The setting of the different registers must be checked before reinitializing the SD card.

Workaround: None

71.1.3 FLEXCOM SMBUS

Issue: FLEXCOM SMBUS alert signalling is not functional

The TWI function embedded in the FLEXCOM does not support SMBUS alert signal management.

Workaround: If this signal is mandatory in the application, the user can use one of the standalone TWIs (TWIHS0, TWIHS1) supporting the SMBUS alert signaling.