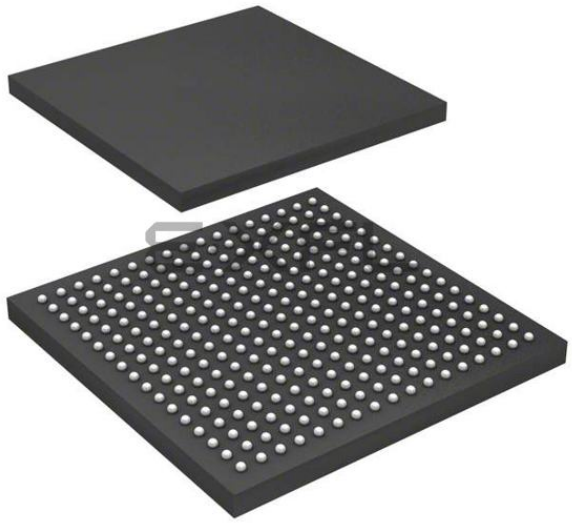

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d28b-cu

18.12.2 Security of APB Slaves

The security type of an APB slave is set at hardware design among the following:

- Peripheral Always Secured (PAS)
- Peripheral Always Non-secured (PNS)
- Peripheral Securable (PS)

To configure the security mode required for accessing a particular APB slave connected to the AHB/APB Bridge, the Bus Matrix features three 32-bit Security Peripheral Select x Registers. Some of these bits may have been set to a Secured or a Non-secured value by design, whereas others are programmed by software (see Section 18.13.15 “Security Peripheral Select x Registers”).

Peripheral security state, “Secure” or “Non-secure” is an AND operation between H32MX MATRIX_SPSELRx and H64MX MATRIX_SPSELRx for the bit corresponding to the peripheral.

As a general rule:

- The peripheral security state is applied to the corresponding peripheral interrupt line. Exceptions may occur on some peripherals (PIO Controller, etc.). In such case, refer to the peripheral description.
- The peripheral security state is applied to the peripheral master part, if any. Exceptions may occur on some peripherals. In such case, refer to the peripheral description. See Section 18.12.3 “Security Types of AHB Master Peripherals”.

MATRIX_SPSELRx bits in the H32MX or H64MX user interface are respectively read/write or read-only to ‘1’ depending on whether the peripheral is connected or not, on the Matrix.

All bit values in Table 18-9 except those marked ‘UD’ (User Defined) are read-only and cannot be changed. Values marked ‘UD’ can be changed. Refer to the following examples.

- Example for GMAC, Peripheral ID 5, which is connected to the H32MX Matrix
  - H64MX MATRIX_SPSELR1[5] = 1 (read-only); no influence on the security configuration
  - H32MX MATRIX_SPSELR1[5] can be written by user to program the security.
- Example for LCDC, Peripheral ID 45, which is connected to the H64MX Matrix
  - H64MX MATRIX_SPSELR2[13] can be written by user to program the security.
  - H32MX MATRIX_SPSELR2[13] = 1 (read-only); no influence on the security configuration
- Example for AIC, Peripheral ID 49, which is connected to the H32MX Matrix
  - H64MX MATRIX_SPSELR2[17] = 1 (read-only); sets the peripheral as Non-secure by hardware, also called “Peripheral Always Non-secured”
  - H32MX MATRIX_SPSELR2[17] = 1 (read-only); no influence on the security configuration
- Example for SAIC, Peripheral ID 0, which is connected to the H32MX Matrix
  - H64MX MATRIX_SPSELR1[0] = 1 (read-only); no influence on the security configuration
  - H32MX MATRIX_SPSELR1[0] = 0 (read-only); sets the peripheral as Secure by hardware, also called “Peripheral Always Secured”

Table 18-9: Peripheral Identifiers

ID	Peripheral	Security Type	Matrix	MATRIX_SPSELRx Bit	Bit Value in H32MX	Bit Value in H64MX
0	SAIC	Peripheral Always Secured (PAS)	–	MATRIX_SPSELR1[0]	0	1
1	–	–	–	–	–	–
2	ARM	Peripheral Securable (PS)	H64MX	MATRIX_SPSELR1[2]	1	UD
3	PIT	PS	H32MX	MATRIX_SPSELR1[3]	UD	1
4	WDT	PS	H32MX	MATRIX_SPSELR1[4]	UD	1
5	GMAC	PS	H32MX	MATRIX_SPSELR1[5]	UD	1
6	XDMAC0	PS	H64MX	MATRIX_SPSELR1[6]	1	UD
7	XDMAC1	PS	H64MX	MATRIX_SPSELR1[7]	1	UD
8	ICM	PS	H32MX	MATRIX_SPSELR1[8]	UD	1
9	AES	PS	H64MX	MATRIX_SPSELR1[9]	1	UD
10	AESB	PS	H64MX	MATRIX_SPSELR1[10]	1	UD

19.3.2 OHCI Interrupt Configuration Register

Name: SFR_OHCIICR

Address: 0xF8030010

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	HSIC_SEL	–	–	–
23	22	21	20	19	18	17	16
UDPPUDIS	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	SUSPEND_C	SUSPEND_B	SUSPEND_A
7	6	5	4	3	2	1	0
–	–	APPSTART	ARIE	–	RES2	RES1	RES0

RESx: USB PORTx RESET

0: Resets USB Port.

1: Usable USB Port.

ARIE: OHCI Asynchronous Resume Interrupt Enable

0: Interrupt disabled.

1: Interrupt enabled.

APPSTART: Reserved

0: Must write 0.

SUSPEND_A: USB PORT A

0: Suspends controlled by EHCI-OCHO.

1: Forces the suspend for PORTA.

SUSPEND_B: USB PORT B

0: Suspend controlled by EHCI-OCHO.

1: Forces the suspend for PORTB.

SUSPEND_C: USB PORT C

0: Suspends controlled by EHCI-OCHO.

1: Forces the suspend for PORTC.

UDPPUDIS: USB DEVICE PULLUP DISABLE

0: USB device pullup connection is enabled.

1: USB device pullup connection is disabled.

HSIC_SEL: Reserved

0: Must write 0.

19.3.12 AIC Interrupt Redirection Register

Name: SFR_AICREDIR

Address: 0xF8030054

Access: Read/Write

31	30	29	28	27	26	25	24
AICREDIRKEY							
23	22	21	20	19	18	17	16
AICREDIRKEY							
15	14	13	12	11	10	9	8
AICREDIRKEY							
7	6	5	4	3	2	1	0
AICREDIRKEY							NSAIC

NSAIC: Interrupt Redirection to Non-Secure AIC

0: Interrupts are managed by the AIC corresponding to the Secure State of the peripheral (secure AIC or non-secure AIC).

1: All interrupts are managed by the non-secure AIC.

AICREDIRKEY: Unlock Key

Value is a XOR between 0xb6d81c4d and SN1[31:0] but only field [31:1] of the result must be written in this field. In case of set in Secure mode by fuse configuration, this register is read_only 0 (it is not possible to redirect secure interrupts on non-secure AIC for products set in secure mode for security reasons).

Note: After three tries, entering a wrong key results in locking the NSAIC bit. A reset is needed.

38.5 Functional Description

38.5.1 Basic Definitions

Source Peripheral: Slave device, memory mapped on the interconnection network, from where the XDMAC reads data. The source peripheral teams up with a destination peripheral to form a channel. A data read operation is scheduled when the peripheral transfer request is asserted.

Destination Peripheral: Slave device, memory mapped on the interconnection network, to which the XDMAC writes. A write data operation is scheduled when the peripheral transfer request is asserted.

Channel: The data movement between source and destination creates a logical channel.

Transfer Type: The transfer is hardware-synchronized when it is paced by the peripheral hardware request, otherwise the transfer is self-triggered (memory to memory transfer).

38.5.2 Transfer Hierarchy Diagram

XDMAC Master Transfer: The Master Transfer is composed of a linked list of blocks. The channel address, control and configuration registers can be modified at the inter block boundary. The descriptor structure modifies the channel registers conditionally. Interrupts can be generated on a per block basis or when the end of linked list event occurs.

XDMAC Block: An XDMAC block is composed of a programmable number of microblocks. The channel configuration registers remain unchanged at the inter microblock boundary. The source and destination addresses are conditionally updated with a programmable signed number.

XDMAC Microblock: The microblock is composed of a programmable number of data. The channel configuration registers remain unchanged at the data boundary. The data address may be fixed (a FIFO location, a peripheral transmit or receive register), incrementing (a memory-mapped area) by a programmable signed number.

XDMAC Burst and Incomplete Burst: In order to improve the overall performance when accessing dynamic external memory, burst access is mandatory. Each data of the microblock is considered as a part of a memory burst. The programmable burst value indicates the largest memory burst allowed on a per channel basis. When the microblock length is not an integral multiple of the burst size, an incomplete burst is performed to read or write the last trailing bytes.

XDMAC Chunk and Incomplete Chunk: When a peripheral synchronized transfer is activated, the microblock splits into a number of data chunks. The chunk size is programmable. The larger the chunk is, the better the performance is. When the transfer size is not a multiple of the chunk size, the last chunk may be incomplete.

Figure 38-2: XDMAC Memory Transfer Hierarchy

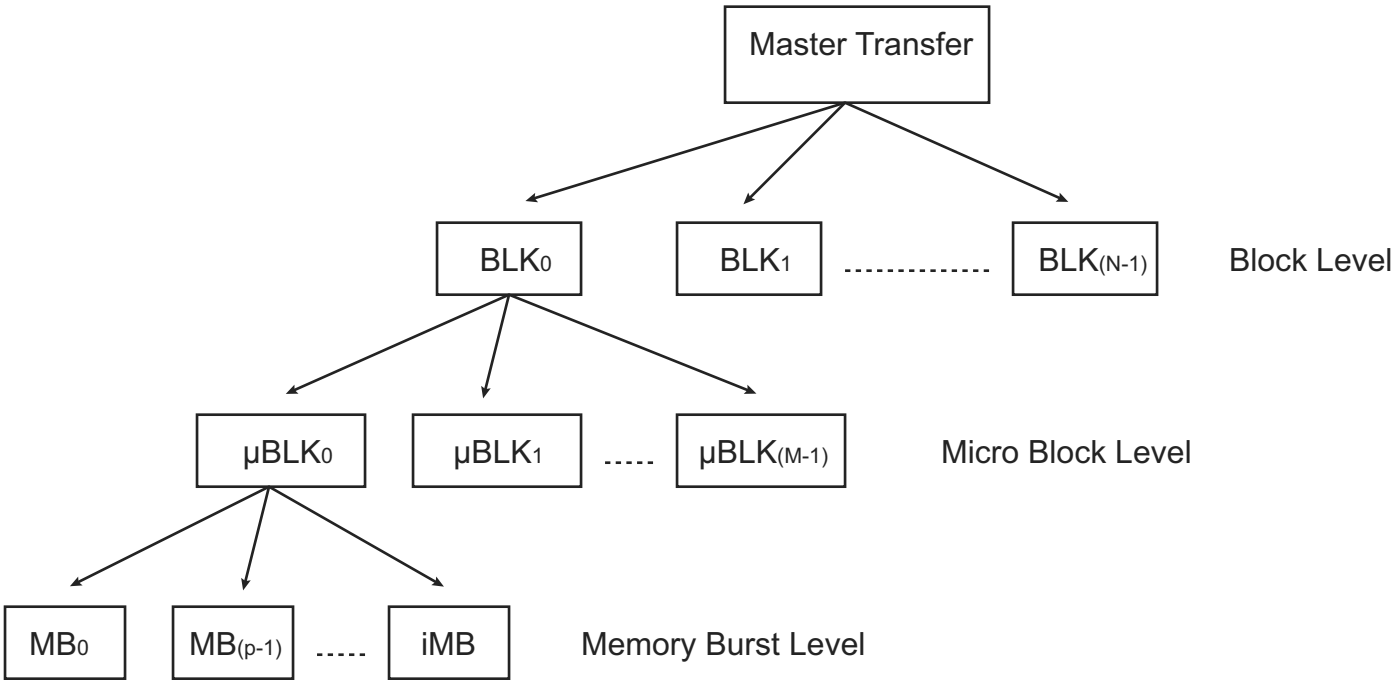


Table 39-43: 4:2:0 Planar Mode Luminance Memory Mapping, Little Endian Organization for Byte 0x4, 0x5, 0x6, 0x7

Mem addr	0x7								0x6								0x5								0x4							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 12 bpp	Y7[7:0]								Y6[7:0]								Y5[7:0]								Y4[7:0]							

Table 39-44: 4:2:0 Planar Mode Chrominance Memory Mapping, Little Endian Organization for Byte 0x0, 0x1, 0x2, 0x3

Mem addr	0x3								0x2								0x1								0x0							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 12 bpp	C3[7:0]								C2[7:0]								C1[7:0]								C0[7:0]							

Table 39-45: 4:2:0 Planar Mode Chrominance Memory Mapping, Little Endian Organization for Byte 0x4, 0x5, 0x6, 0x7

Mem addr	0x7								0x6								0x5								0x4							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 12 bpp	C7[7:0]								C6:[7:0]								C5[7:0]								C4[7:0]							

39.6.5.6 4:2:0 Semiplanar Frame Buffer Memory Mapping

Table 39-46: 4:2:0 Semiplanar Mode Luminance Memory Mapping, Little Endian Organization

Mem addr	0x7								0x6								0x5								0x4							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 12 bpp	Y3[7:0]								Y2[7:0]								Y1[7:0]								Y0[7:0]							

Table 39-47: 4:2:0 Semiplanar Mode Chrominance Memory Mapping, Little Endian Organization

Mem addr	0x3								0x2								0x1								0x0							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 12 bpp	Cb1[7:0]								Cr1[7:0]								Cb0[7:0]								Cr0[7:0]							

39.6.6 Chrominance Upsampling Unit

Both the 4:2:2 and the 4:2:0 input formats are supported by the LCD module. In 4:2:2, the two chrominance components are sampled at half the luminance sample rate. The horizontal chrominance resolution is halved. When this input format is selected, the chrominance upsampling unit uses two chrominances to interpolate the missing component.

In 4:2:0, Cr and Cb components are subsampled at a factor of two vertically and horizontally. When this input mode is selected, the chrominance upsampling unit uses two and four chroma components to generate the missing horizontal and vertical components.

REP: Use Replication logic to expand RGB color to 24 bits

0: When the selected pixel depth is less than 24 bpp the pixel is shifted and least significant bits are set to 0.

1: When the selected pixel depth is less than 24 bpp the pixel is shifted and the least significant bit replicates the msb.

DSTKEY: Destination Chroma Keying

0: Source Chroma keying is enabled.

1: Destination Chroma keying is used.

GA: Blender Global Alpha

Global alpha blender for the current layer.

40.8.48 GMAC Octets Transmitted High Register

Name: GMAC_OTHI

Address: 0xF8008104

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TXO							

7	6	5	4	3	2	1	0
TXO							

When reading the Octets Transmitted and Octets Received Registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

TXO: Transmitted Octets

Transmitted octets in frame without errors [47:32]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames.

Figure 46-21: TWIHS Read Operation with Single Data Byte without Internal Address

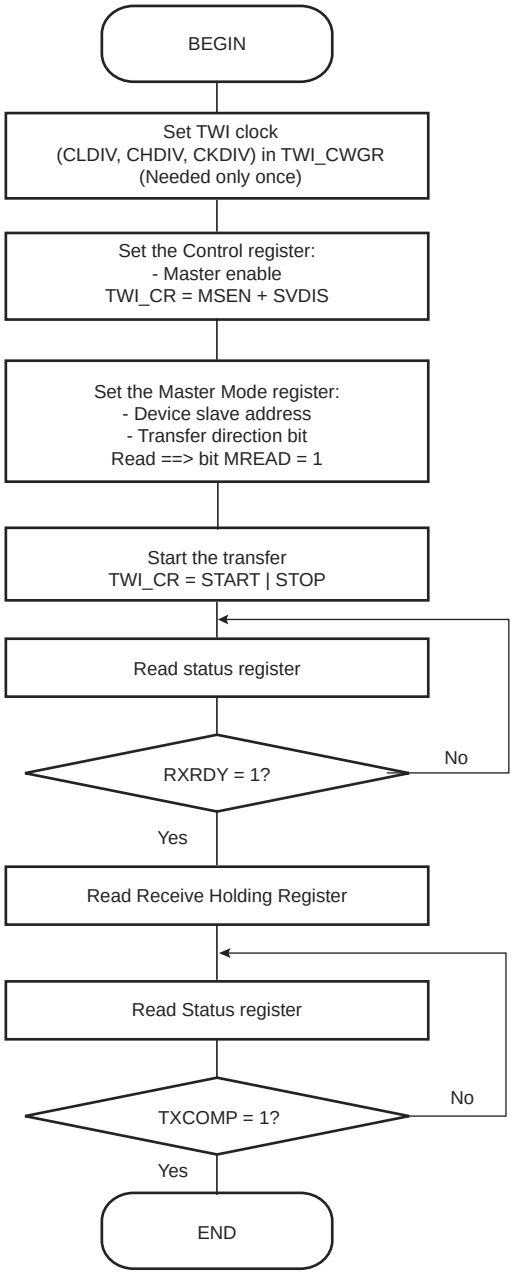
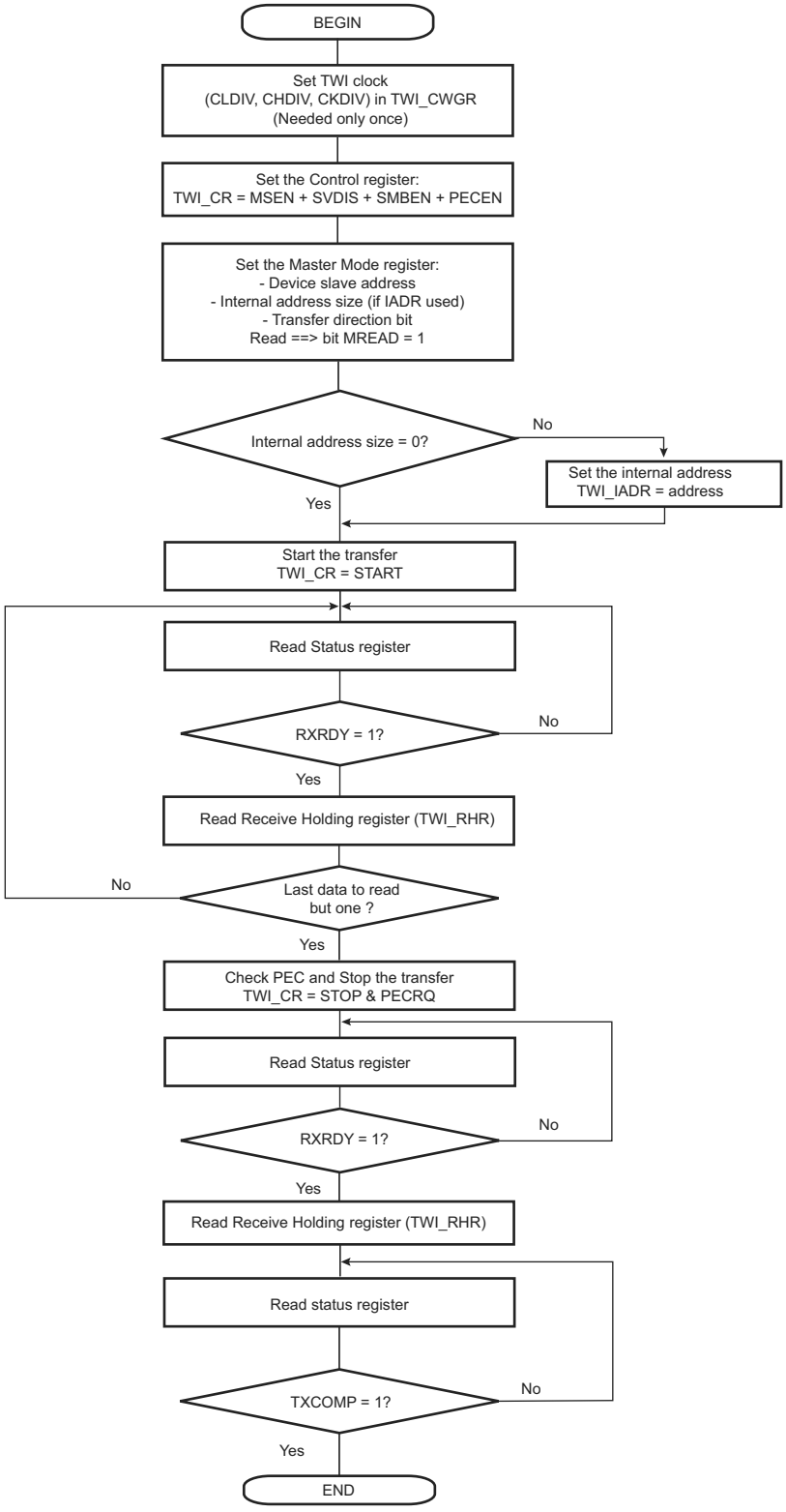


Figure 46-24: TWIHS Read Operation with Multiple Data Bytes with or without Internal Address with PEC



47.10.68 TWI Interrupt Enable Register

Name: FLEX_TWI_IER

Address: 0xF8034624 (0), 0xF8038624 (1), 0xFC010624 (2), 0xFC014624 (3), 0xFC018624 (4)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	SMBHHM	SMBDAM	PECERR	TOUT	–	MCACK
15	14	13	12	11	10	9	8
TXBUFE	RXBUFF	ENDTX	ENDRX	EOSACC	SCL_WS	ARBLST	NACK
7	6	5	4	3	2	1	0
UNRE	OVRE	GACC	SVACC	–	TXRDY	RXRDY	TXCOMP

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

TXCOMP: Transmission Completed Interrupt Enable

RXRDY: Receive Holding Register Ready Interrupt Enable

TXRDY: Transmit Holding Register Ready Interrupt Enable

SVACC: Slave Access Interrupt Enable

GACC: General Call Access Interrupt Enable

OVRE: Overrun Error Interrupt Enable

UNRE: Underrun Error Interrupt Enable

NACK: Not Acknowledge Interrupt Enable

ARBLST: Arbitration Lost Interrupt Enable

SCL_WS: Clock Wait State Interrupt Enable

EOSACC: End Of Slave Access Interrupt Enable

ENDRX: End of Receive Buffer Interrupt Enable

ENDTX: End of Transmit Buffer Interrupt Enable

RXBUFF: Receive Buffer Full Interrupt Enable

TXBUFE: Transmit Buffer Empty Interrupt Enable

MCACK: Master Code Acknowledge Interrupt Enable

TOUT: Timeout Error Interrupt Enable

PECERR: PEC Error Interrupt Enable

SMBDAM: SMBus Default Address Match Interrupt Enable

SMBHHM: SMBus Host Header Address Match Interrupt Enable

EXTUN: Execute Tuning

This bit is set to 1 to start the tuning procedure and is automatically cleared when the tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select (SCLKSEL). The tuning procedure is aborted by writing 0. Refer to Figure 2.29 in the “SD Host Controller Simplified Specification V3.00” .

0: Not tuned or tuning completed.

1: Execute tuning.

SCLKSEL: Sampling Clock Select

The SDMMC uses this bit to select the sampling clock to receive CMD and DAT.

This bit is set by the tuning procedure and is valid after completion of tuning (when EXTUN is cleared). Setting 1 means that tuning is completed successfully and setting 0 means that tuning has failed.

Writing 1 to this bit is meaningless and ignored. A tuning circuit is reset by writing to 0. This bit can be cleared by setting EXTUN to 1. Once the tuning circuit is reset, it takes time to complete the tuning sequence. Therefore, the user should keep this bit to 1 to perform a retuning sequence to complete a retuning sequence in a short time. Changing this bit is not allowed while the SDMMC is receiving a response or a read data block. Refer to Figure 2.29 in the “SD Host Controller Simplified Specification V3.00” .

0: The fixed clock is used to sample data.

1: The tuned clock is used to sample data.

ASINTEN: Asynchronous Interrupt Enable

This bit can be set to 1 if a card support asynchronous interrupts and Asynchronous Interrupt Support (ASINTSUP) is set to 1 in SDMMC_CA0R. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode. If this bit is set to 1, the user can stop the SDCLK during the asynchronous interrupt period to save power. During this period, the SDMMC continues to deliver the Card Interrupt to the host when it is asserted by the card.

0: Disabled

1: Enabled

PVALEN: Preset Value Enable

As the operating SDCLK frequency and I/O driver strength depend on the system implementation, it is difficult to determine these parameters in the standard host driver. When Preset Value Enable (PVALEN) is set to 1, automatic SDCLK frequency generation and driver strength selection are performed without considering system-specific conditions. This bit enables the functions defined in SDMMC_PVR.

if this bit is set to 0, SDCLKFSEL, CLKGSEL in SDMMC_CCR and DRVSEL in SDMMC_HC2R are set by the user.

if this bit is set to 1, SDCLKFSEL, CLKGSEL in SDMMC_CCR and DRVSEL in SDMMC_HC2R are set by the SDMMC as specified in SDMMC_PVR.

0: SDCLK and Driver strength are controlled by the user.

1: Automatic selection by Preset Value is enabled.

Table 52-18: Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x198	Gamma Correction Green Entry 0	ISC_GAM_GENTRY0	Read/Write	0x00000000
...	...	...	...	...
0x294	Gamma Correction Green Entry 63	ISC_GAM_GENTRY63	Read/Write	0x00000000
0x298	Gamma Correction Red Entry 0	ISC_GAM_RENTRY0	Read/Write	0x00000000
...	...	...	...	...
0x394	Gamma Correction Red Entry 63	ISC_GAM_RENTRY63	Read/Write	0x00000000
0x398	Color Space Conversion Control Register	ISC_CSC_CTRL	Read/Write	0x00000000
0x39C	Color Space Conversion YR, YG Register	ISC_CSC_YR_YG	Read/Write	0x00000000
0x3A0	Color Space Conversion YB, OY Register	ISC_CSC_YB_OY	Read/Write	0x00000000
0x3A4	Color Space Conversion CBR CBG Register	ISC_CSC_CBR_CBG	Read/Write	0x00000000
0x3A8	Color Space Conversion CBB OCB Register	ISC_CSC_CBB_OCB	Read/Write	0x00000000
0x3AC	Color Space Conversion CRR CRG Register	ISC_CSC_CRR_CRG	Read/Write	0x00000000
0x3B0	Color Space Conversion CRB OCR Register	ISC_CSC_CRB_OCR	Read/Write	0x00000000
0x3B4	Contrast and Brightness Control Register	ISC_CBC_CTRL	Read/Write	0x00000000
0x3B8	Contrast and Brightness Configuration Register	ISC_CBC_CFG	Read/Write	0x00000000
0x3BC	Contrast and Brightness, Brightness Register	ISC_CBC_BRIGHT	Read/Write	0x00000000
0x3C0	Contrast and Brightness, Contrast Register	ISC_CBC_CONTRAST	Read/Write	0x00000000
0x3C4	Subsampling 4:4:4 to 4:2:2 Control Register	ISC_SUB422_CTRL	Read/Write	0x00000000
0x3C8	Subsampling 4:4:4 to 4:2:2 Configuration Register	ISC_SUB422_CFG	Read/Write	0x00000000
0x3CC	Subsampling 4:2:2 to 4:2:0 Control Register	ISC_SUB420_CTRL	Read/Write	0x00000000
0x3D0	Rounding, Limiting and Packing Configuration Register	ISC_RLP_CFG	Read/Write	0x00000000
0x3D4	Histogram Control Register	ISC_HIS_CTRL	Read/Write	0x00000000
0x3D8	Histogram Configuration Register	ISC_HIS_CFG	Read/Write	0x00000000
0x3DC	Reserved	–	–	–
0x3E0	DMA Configuration Register	ISC_DCFG	Read/Write	0x00000000
0x3E4	DMA Control Register	ISC_DCTRL	Read/Write	0x00000000
0x3E8	DMA Descriptor Address Register	ISC_DNDA	Read/Write	0x00000000
0x3EC	DMA Address 0 Register	ISC_DAD0	Read/Write	0x00000000
0x3F0	DMA Stride 0 Register	ISC_DST0	Read/Write	0x00000000
0x3F4	DMA Address 1 Register	ISC_DAD1	Read/Write	0x00000000
0x3F8	DMA Stride 1 Register	ISC_DST1	Read/Write	0x00000000
0x3FC	DMA Address 2 Register	ISC_DAD2	Read/Write	0x00000000
0x400	DMA Stride 2 Register	ISC_DST2	Read/Write	0x00000000
0x404–0x40C	Reserved	–	–	

52.6.4 ISC Parallel Front End Configuration 0 Register

Name: ISC_PFE_CFG0

Address: 0xF000800C

Access: Read/Write

31	30	29	28	27	26	25	24
REP	BPS			CCIR_REP	–	–	–

23	22	21	20	19	18	17	16
SKIPCNT							

15	14	13	12	11	10	9	8
–	–	ROWEN	COLEN	CCIR10_8N	CCIR_CRC	CCIR656	GATED

7	6	5	4	3	2	1	0
CONT	MODE			FPOL	PPOL	VPOL	HPOL

HPOL: Horizontal Synchronization Polarity

0: HSYNC signal is active high, i.e. valid pixels are sampled when HSYNC is asserted.

1: HSYNC signal is active low, i.e. valid pixels are sampled when HSYNC is deasserted.

VPOL: Vertical Synchronization Polarity

0: VSYNC signal is active high, i.e. valid pixels are sampled when VSYNC is asserted.

1: VSYNC signal is active low, i.e. valid pixels are sampled when VSYNC is deasserted.

PPOL: Pixel Clock Polarity

0: The pixel stream is sampled on the rising edge of the pixel clock.

1: The pixel stream is sampled on the falling edge of the pixel clock.

FPOL: Field Polarity

0: Top field is sampled when F value is 0; Bottom field is sampled when F value is 1

1: Top field is sampled when F value is 1; Bottom field is sampled when F value is 0

MODE: Parallel Front End Mode

Value	Name	Description
0	PROGRESSIVE	Video source is progressive.
1	DF_TOP	Video source is interlaced, two fields are captured starting with top field.
2	DF_BOTTOM	Video source is interlaced, two fields are captured starting with bottom field.
3	DF_IMMEDIATE	Video source is interlaced, two fields are captured immediately.
4	SF_TOP	Video source is interlaced, one field is captured starting with the top field.
5	SF_BOTTOM	Video source is interlaced, one field is captured starting with the bottom field.
6	SF_IMMEDIATE	Video source is interlaced, one field is captured starting immediately.

CONT: Continuous Acquisition

0: Single Shot mode

1: Video mode

52.6.51 ISC DMA Configuration Register

Name: ISC_DCFG

Address: 0xF00083E0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	CMBSIZE	

7	6	5	4	3	2	1	0
–	–	YMBSIZE		–	IMODE		

IMODE: DMA Input Mode Selection

Value	Name	Description
0	PACKED8	8 bits, single channel packed
1	PACKED16	16 bits, single channel packed
2	PACKED32	32 bits, single channel packed
3	YC422SP	32 bits, dual channel
4	YC422P	32 bits, triple channel
5	YC420SP	32 bits, dual channel
6	YC420P	32 bits, triple channel

YMBSIZE: DMA Memory Burst Size Y channel

Value	Name	Description
0	SINGLE	DMA single access
1	BEATS4	4-beat burst access
2	BEATS8	8-beat burst access
3	BEATS16	16-beat burst access

CMBSIZE: DMA Memory Burst Size C channel

Value	Name	Description
0	SINGLE	DMA single access
1	BEATS4	4-beat burst access
2	BEATS8	8-beat burst access
3	BEATS16	16-beat burst access

53.6.45 MCAN Transmit Event FIFO Configuration

Name: MCAN_TXEFC

Address: 0xF80540F0 (0), 0xFC0500F0 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	EFWM					
23	22	21	20	19	18	17	16
–	–	EFS					
15	14	13	12	11	10	9	8
EFSA							
7	6	5	4	3	2	1	0
EFSA						–	–

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

EFSA: Event FIFO Start Address

Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 53-12).

Write EFSA with the bits [15:2] of the 32-bit address.

EFS: Event FIFO Size

0: Tx Event FIFO disabled.

1-32: Number of Tx Event FIFO elements.

>32: Values greater than 32 are interpreted as 32.

The Tx Event FIFO elements are indexed from 0 to EFS - 1.

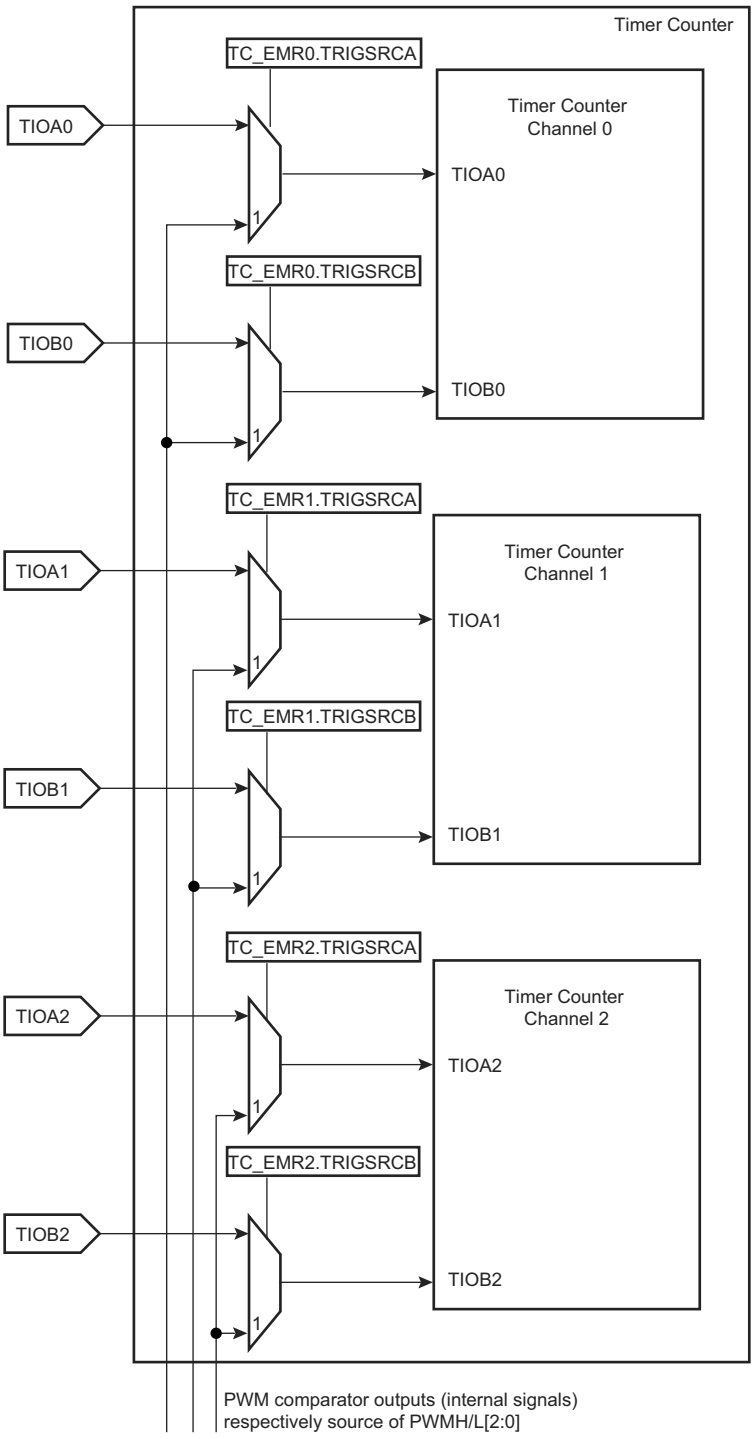
EFWM: Event FIFO Watermark

0: Watermark interrupt disabled.

1-32: Level for Tx Event FIFO watermark interrupt (MCAN_IR.TEFW).

>32: Watermark interrupt disabled.

Figure 54-16: Synchronization with PWM



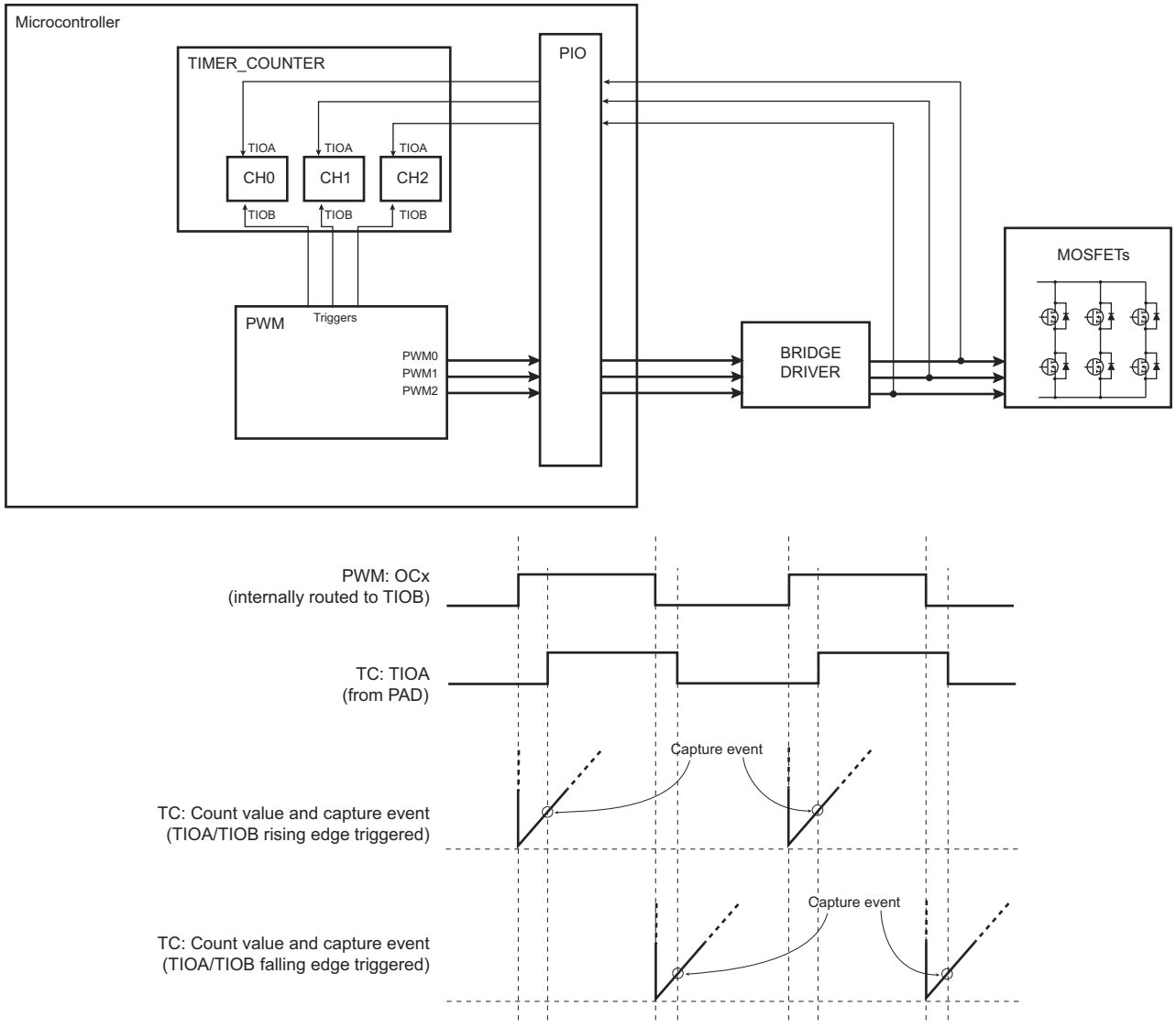
56.6.2.3 Trigger Selection for Timer Counter

The PWM controller can be used as a trigger source for the Timer Counter (TC) to achieve the two application examples described below.

- Delay Measurement

To measure the delay between the channel x comparator output (OCx) and the feedback from the bridge driver of the MOSFETs (see Figure 56-6), the bit TCTS in the PWM Channel Mode Register must be at 0. This defines the comparator output of the channel x as the TC trigger source. The TIOB trigger (TC internal input) is used to start the TC; the TIOA input (from PAD) is used to capture the delay.

Figure 56-6: Triggering the TC: Delay Measurement



- Cumulated ON Time Measurement

To measure the cumulated “ON” time of MOSFETs (see Figure 56-7), the bit TCTS of the PWM Channel Mode Register must be set to 1 to define the counter event (see Figure 56-5) as the Timer Counter trigger source.

57.5.2 SFC Mode Register

Name: SFC_MR

Address: 0xF804C004

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	SASEL	–	–	–	MSK

MSK: Mask Data Registers

0: No effect

1: The data registers from SFC_DR20 to SFC_DR23 are always read at 0x00000000.

Note: The MSK bit is set-only. Only a hardware reset can disable fuse masking.

SASEL: Sense Amplifier Selection

0: Comparator type sense amplifier selected

1: Latch type sense amplifier selected

2. Set the AES Key Register and wait for AES_ISR.DATRDY to be set (GCM hash subkey generation complete); use interrupt if needed. After the GCM hash subkey generation is complete the GCM hash subkey can be read or overwritten with specific value in AES_GCMHRx. See Section 60.4.6.2 “Key Writing and Automatic Hash Subkey Calculation”.
3. Calculate the J_0 value as described in NIST documentation $J_0 = IV \,||\, 0^{31} \,||\, 1$ when len(IV) = 96 and $J_0 = \text{GHASH}_H(IV \,||\, 0^{s+64} \,||\, [\text{len}(IV)]_{64})$ if len(IV) ≠ 96. See Processing a Message with only AAD (GHASHH) for J_0 generation example when len(IV) ≠ 96.
4. Set AES_IVRx.IV with inc32(J_0) (J_0 + 1 on 32 bits).
5. Configure AES_AADLENR.AADLEN and AES_CLENR.CLEN according to the length of the first fragment, or set the fields with the full message length (both configurations work).
6. Fill AES_IDATARx.IDATA with the first fragment of the message to process (aligned on 16-byte boundary) according to the SMOD configuration used. If Manual Mode or Auto Mode is used the DATRDY bit indicates when the data have been processed (however, no output data are generated when processing *AAD*).
7. Make sure the last output data have been read if the fragment ends in C phase (or wait for DATRDY if the fragment ends in *AAD* phase), then read AES_GHASHRx.GHASH to obtain the value of the hash after the last processed data and finally read AES_CTR.CTR to obtain the value of the CTR encryption counter (not needed when the fragment ends in *AAD* phase).

- Next fragment (or last fragment):

1. Set AES_MR.OPMOD to GCM and AES_MR.GTAGEN to ‘0’.
2. Set the AES Key Register and wait until AES_ISR.DATRDY is set (GCM hash subkey generation complete); use interrupt if needed. After the GCM hash subkey generation is complete the GCM hash subkey can be read or overwritten with specific value in AES_GCMHRx. See Section 60.4.6.2 “Key Writing and Automatic Hash Subkey Calculation”.
3. Set AES_IVRx.IV as follows:
   - If the first block of the fragment is a block of Additional Authenticated data, set AES_IVRx.IV with the J0 initial value
   - If the first block of the fragment is a block of Plaintext data, set AES_IVRx.IV with a value constructed as follows: ‘LSB96(J0) || CTR’ value, (96 bit LSB of J0 concatenated with saved CTR value from previous fragment).
4. Configure AES_AADLENR.AADLEN and AES_CLENR.CLEN according to the length of the current fragment, or set the fields with the remaining message length, both configurations work.
5. Fill AES_GHASHRx.GHASH with the value stored after the previous fragment.
6. Fill AES_IDATARx.IDATA with the current fragment of the message to process (aligned on 16 byte boundary) according to the SMOD configuration used. If Manual Mode or Auto Mode is used, the DATRDY bit indicates when the data have been processed (however, no output data are generated when processing *AAD*).
7. Make sure the last output data have been read if the fragment ends in C phase (or wait for DATRDY if the fragment ends in *AAD* phase), then read AES_GHASHRx.GHASH to obtain the value of the hash after the last processed data and finally read AES_CTR.CTR to obtain the value of the CTR encryption counter (not needed when the fragment ends in *AAD* phase).

Note: Step 1 and 2 are required only if the value of the concerned registers has been modified.

Once the last fragment has been processed, the GHASH value will allow manual generation of the GCM tag. See Manual GCM Tag Generation.

- Manual GCM Tag Generation

This section describes the last steps of the GCM Tag generation.

The Manual GCM Tag Generation is used to complete the GCM Tag Generation when the message has been processed without Tag Generation.

Note: The Message Processing without Tag Generation must be finished before processing the Manual GCM Tag Generation.

To generate a GCM Tag manually, the sequence is as follows:

Processing $S = \text{GHASH}_H(AAD \,||\, 0^v \,||\, C \,||\, 0^u \,||\, [\text{len}(AAD)]_{64} \,||\, [\text{len}(C)]_{64})$:

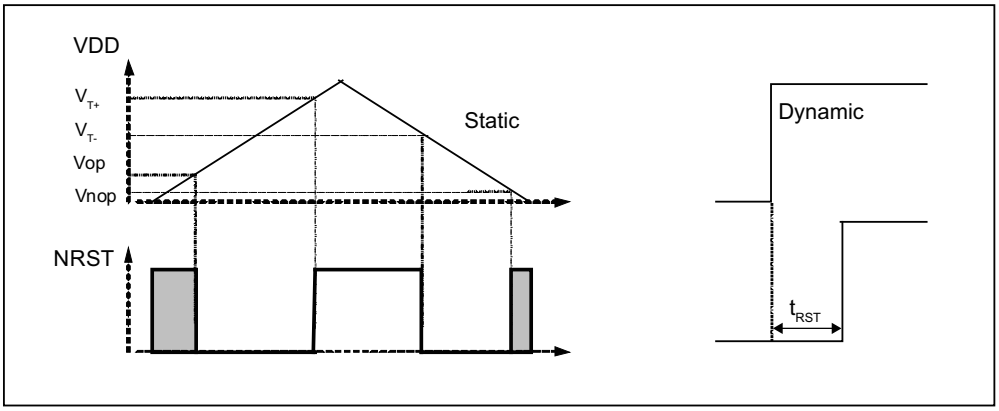
1. Set AES_MR.OPMOD to GCM and AES_MR.GTAGEN to ‘0’.
2. Set the AES Key Register and wait for AES_ISR.DATRDY to be set (GCM hash subkey generation complete); use interrupt if needed. After the GCM hash subkey generation is complete the GCM hash subkey can be read or overwritten with specific value in AES_GCMHRx. See Section 60.4.6.2 “Key Writing and Automatic Hash Subkey Calculation”.
3. Configure AES_AADLENR.AADLEN to 0x10 (16 bytes) and AES_CLENR.CLEN to ‘0’. This will allow running a single GHASH_H on a 16-byte input data (see Figure 60-7).
4. Fill AES_GHASHRx.GHASH with the state of the GHASH field stored at the end of the message processing.
5. Fill AES_IDATARx.IDATA according to the SMOD configuration used with ‘$\text{len}(AAD)_{64} \,||\, \text{len}(C)_{64}$’ value as described in the NIST documentation and wait for DATRDY to be set; use interrupt if needed.
6. Read AES_GHASHRx.GHASH to obtain the current value of the hash.

Processing $T = \text{GCTR}_K(J_0, S)$:

66.13 POR Characteristics

Figure 66-9 provides a general presentation of Power-On-Reset (POR) characteristics.

Figure 66-9: General Presentation of POR Behavior



When a very slow (versus t_{RST}) supply rising slope is applied on the POR VDD pin, the reset time becomes negligible and the reset signal is released when VDD raises higher than V_{T+}.

When a very fast (versus t_{RST}) supply rising slope is applied on the POR VDD pin, the voltage threshold becomes negligible and the reset signal is released after t_{RST}. It is the smallest possible reset time.

Table 66-40: VDDBU Power-On Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T+}	Threshold Voltage Rising	–	1.3	–	1.5	V
V_{T-}	Threshold Voltage Falling	–	1.22	–	1.4	V
V_{hys}	Hysteresis Voltage	–	50	–	160	mV
t_{RST}	Reset Timeout Period	–	890	–	5100	µs

Table 66-41: VDDCORE Power-On Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T+}	Threshold Voltage Rising	–	0.927	–	1.075	V
V_{T-}	Threshold Voltage Falling	–	0.848	–	1.025	V
V_{hys}	Hysteresis Voltage	–	38	–	109	mV
t_{RST}	Reset Timeout Period	–	150	–	650	µs

Table 66-42: VDDANA Power-On Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T+}	Threshold Voltage Rising	–	1.3	–	1.5	V
V_{T-}	Threshold Voltage Falling	–	1.22	–	1.4	V
V_{hys}	Hysteresis Voltage	–	50	–	160	mV
t_{RST}	Reset Timeout Period	–	130	–	650	µs