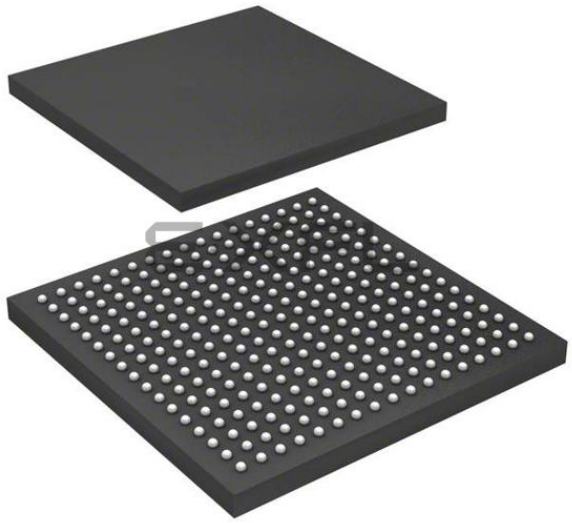


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d28b-cur

Table 6-2: Pin Description (Continued)

289-pin BGA	256-pin BGA	196-pin BGA	Power Rail	I/O Type	Primary		Alternate		PIO peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1][2]
					Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
M14	P17	–	VDDIOP1	GPIO_QSPI	PA14	I/O	–	–	A	SPI0_SPCK	I/O	1	PIO, I, PU, ST
									B	TK1	I/O	1	
									C	QSPI0_SCK	O	2	
									D	I2SC1_MCK	O	2	
									E	FLEXCOM3_IO2	I/O	1	
									F	D9	I/O	2	
N16	R18	–	VDDIOP1	GPIO	PA15	I/O	–	–	A	SPI0_MOSI	I/O	1	PIO, I, PU, ST
									B	TF1	I/O	1	
									C	QSPI0_CS	O	2	
									D	I2SC1_CK	I/O	2	
									E	FLEXCOM3_IO0	I/O	1	
									F	D10	I/O	2	
M10	N15	–	VDDIOP1	GPIO_IO	PA16	I/O	–	–	A	SPI0_MISO	I/O	1	PIO, I, PU, ST
									B	TD1	O	1	
									C	QSPI0_IO0	I/O	2	
									D	I2SC1_WS	I/O	2	
									E	FLEXCOM3_IO3	O	1	
									F	D11	I/O	2	
N17	P18	–	VDDIOP1	GPIO_IO	PA17	I/O	–	–	A	SPI0_NPCS0	I/O	1	PIO, I, PU, ST
									B	RD1	I	1	
									C	QSPI0_IO1	I/O	2	
									D	I2SC1_DI0	I	2	
									E	FLEXCOM3_IO4	O	1	
									F	D12	I/O	2	
U14	M9	L9	VDDIOP1	GPIO_IO	PA18	I/O	–	–	A	SPI0_NPCS1	O	1	PIO, I, PU, ST
									B	RK1	I/O	1	
									C	QSPI0_IO2	I/O	2	
									D	I2SC1_DO0	O	2	
									E	SDMMC1_DAT0	I/O	1	
									F	D13	I/O	2	
T14	V13	N9	VDDIOP1	GPIO_IO	PA19	I/O	–	–	A	SPI0_NPCS2	O	1	PIO, I, PU, ST
									B	RF1	I/O	1	
									C	QSPI0_IO3	I/O	2	
									D	TIOA0	I/O	1	
									E	SDMMC1_DAT1	I/O	1	
									F	D14	I/O	2	

30.5.4 Register Write Protection

To prevent any single software error from corrupting RXLP behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the RXLP Write Protection Mode Register (RXLP_WPMR).

The following registers can be write-protected:

- RXLP Mode Register
- RXLP Baud Rate Generator Register
- RXLP Comparison Register

33.22.24 PMC Peripheral Clock Enable Register 1

Name: PMC_PCER1

Address: 0xF0014100

Access: Write-only

31	30	29	28	27	26	25	24
PID63	PID62	PID61	PID60	PID59	PID58	PID57	PID56
23	22	21	20	19	18	17	16
PID55	PID54	PID53	PID52	PID51	PID50	PID49	PID48
15	14	13	12	11	10	9	8
PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
7	6	5	4	3	2	1	0
PID39	PID38	PID37	PID36	PID35	PID34	PID33	PID32

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

PIDx: Peripheral Clock x Enable

0: No effect.

1: Enables the corresponding peripheral clock.

Note 1: PID32 to PID63 refer to identifiers as defined in Section 11.2 “Peripheral Identifiers”.

2: Programming the control bits of the Peripheral ID that are not implemented has no effect on the behavior of the PMC.

34.7.8 PIO Interrupt Enable Register

Name: PIO_IERx [x=0..3]

Address: 0xFC038020 [0], 0xFC038060 [1], 0xFC0380A0 [2], 0xFC0380E0 [3]

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0–P31: Input Change Interrupt Enable

0: No effect.

1: Enables the Input Change interrupt on the I/O line of the I/O group x.

34.7.29 Secure PIO I/O Freeze Configuration Register

Name: S_PIO_IOFRx [x=0..3]

Address: 0xFC03903C [0], 0xFC03907C [1], 0xFC0390BC [2], 0xFC0390FC [3]

Access: Write-only

31	30	29	28	27	26	25	24
FRZKEY							
23	22	21	20	19	18	17	16
FRZKEY							
15	14	13	12	11	10	9	8
FRZKEY							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	FINT	FPHY

Writing this register will only affect I/O lines enabled in the S_PIO_MSKRx.

FPHY: Freeze Physical Configuration

0: No effect.

1: Freezes the following configuration fields of Secure I/O lines if FRZKEY corresponds to 0x494F46 (“IOF” in ASCII):

- FUNC: I/O Line Function
- DIR: Direction
- PUEN: Pull-Up Enable
- PDEN: Pull-Down Enable
- OPD: Open-Drain
- SCHMITT: Schmitt Trigger
- DRVSTR: Drive Strength

Only a hardware reset can reset the FPHY bit.

FINT: Freeze Interrupt Configuration

0: No effect.

1: Freezes the following configuration fields of Secure I/O lines if FRZKEY corresponds to 0x494F46 (“IOF” in ASCII):

- IFEN: Input Filter Enable
- IFSCEN: Input Filter Slow Clock Enable
- EVTSEL: Event Selection

Only a hardware reset can reset the FINT bit.

FRZKEY: Freeze Key

Value	Name	Description
0x494F46	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit.

Table 36-13: Sequential Mapping for DDR-SDRAM Configuration: 16K Rows,1024/ Columns, 8 banks

CPU Address Line																										
27	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bk[2:0]			Row[13:0]														Column[9:0]										M0

Table 36-14: Interleaved Mapping for DDR-SDRAM Configuration: 16K Rows,1024/ Columns, 8 banks

CPU Address Line																										
27	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Row[13:0]														Bk[2:0]			Column[9:0]										M0

37.20.10 PMECC Spare Area Size Register

Name: HSMC_PMECCSAREA

Address: 0xF8014074

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	SPARESIZE

7	6	5	4	3	2	1	0
SPARESIZE							

SPARESIZE: Spare Area Size

Number of bytes in the spare area. The spare area size is equal to (SPARESIZE + 1) bytes.

39.7.133 High-End Overlay Configuration Register 38

Name: LCDC_HEOCFG38

Address: 0xF0000424

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
YPHI5COEFF2							

15	14	13	12	11	10	9	8
YPHI5COEFF1							

7	6	5	4	3	2	1	0
YPHI5COEFF0							

YPHI5COEFF0: Vertical Coefficient for phase 5 tap 0

Coefficient format is 1 sign bit and 7 fractional bits.

YPHI5COEFF1: Vertical Coefficient for phase 5 tap 1

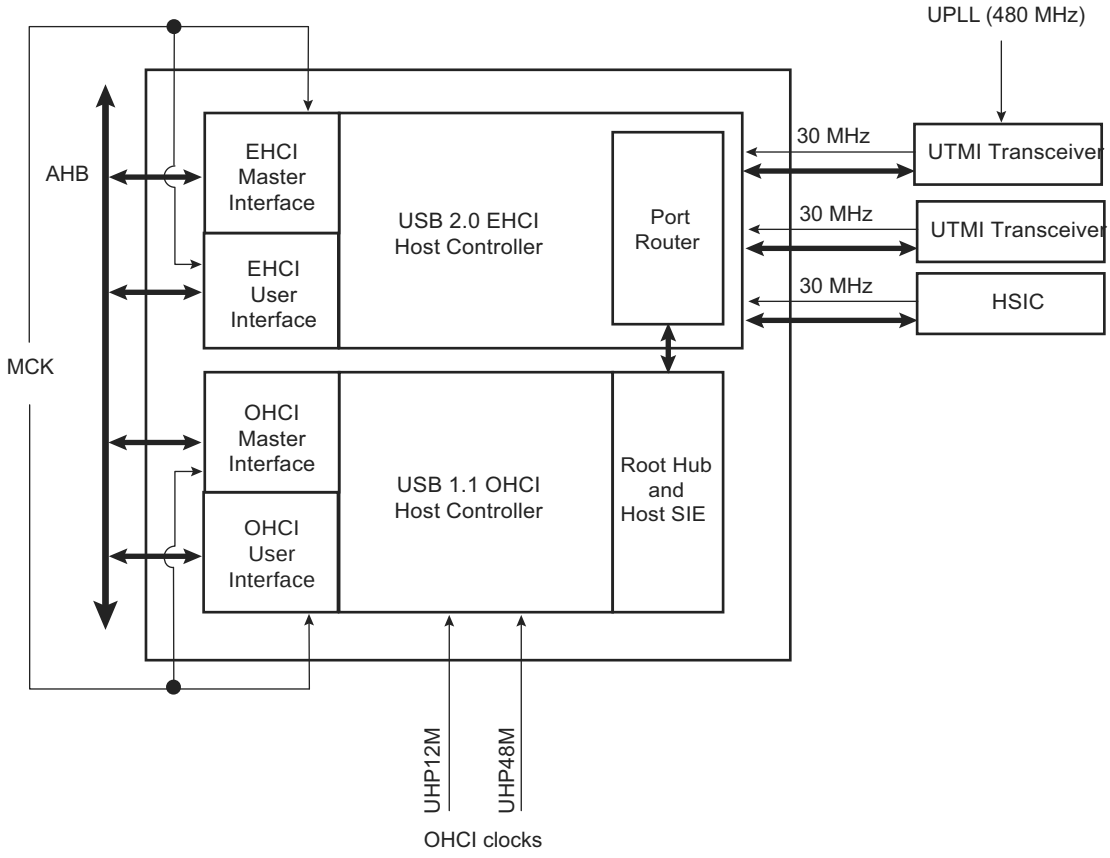
Coefficient format is 1 magnitude bit and 7 fractional bits.

YPHI5COEFF2: Vertical Coefficient for phase 5 tap 2

Coefficient format is 1 sign bit and 7 fractional bits.

- Enable UHP peripheral clock in PMC_PCER.
- Select PLLACK as Input clock of OHCI part (USBS bit in PMC_USB register).
- Program OHCI clocks (UHP48M and UHP12M) with USBDIV field in PMC_USB register. USBDIV value is to be calculated according to the PLLACK value and USB Full-speed accuracy.
- Enable the OHCI clocks with UHP bit in PMC_SCER.

Figure 42-3: UHP Clock Trees



42.5.3 Interrupt Sources

The USB host interface has an interrupt line connected to the interrupt controller.

Handling USB host interrupts requires programming the interrupt controller before configuring the UHPHS.

46.7.19 TWIHS Transmit Holding Register (FIFO_ENABLED)

Name: TWIHS_THR (FIFO_ENABLED)

Address: 0xF8028034 (0), 0xFC028034 (1)

Access: Write-only

31	30	29	28	27	26	25	24
TXDATA3							
23	22	21	20	19	18	17	16
TXDATA2							
15	14	13	12	11	10	9	8
TXDATA1							
7	6	5	4	3	2	1	0
TXDATA0							

Note: If FIFO is enabled (FIFOEN bit in TWIHS_CR), see Master Multiple Data Mode for details.

TXDATA0: Master or Slave Transmit Holding Data 02

TXDATA1: Master or Slave Transmit Holding Data 1

TXDATA2: Master or Slave Transmit Holding Data 2

TXDATA3: Master or Slave Transmit Holding Data 3

Figure 47-83: START and STOP Conditions

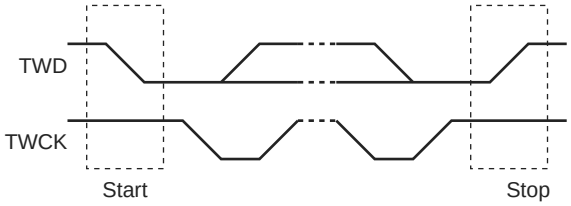
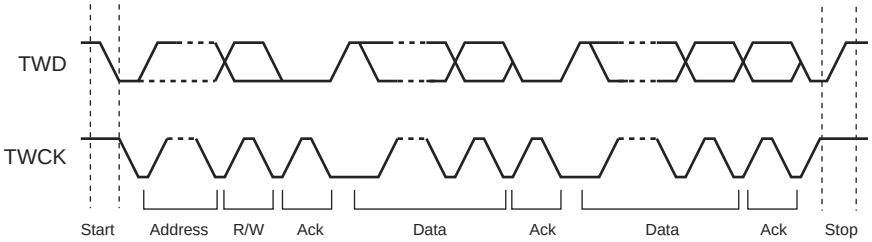


Figure 47-84: Transfer Format



47.9.2 Modes of Operation

The TWI has different modes of operation:

- Master Transmitter mode (Standard and Fast modes only)
- Master Receiver mode (Standard and Fast modes only)
- Multi-master Transmitter mode (Standard and Fast modes only)
- Multi-master Receiver mode (Standard and Fast modes only)
- Slave Transmitter mode (Standard, Fast and High-speed modes)
- Slave Receiver mode (Standard, Fast and High-speed modes)

These modes are described in the following sections.

47.9.3 Master Mode

47.9.3.1 Definition

The master is the device that starts a transfer, generates a clock and stops it. This operating mode is not available if High-speed mode is selected.

47.9.3.2 Programming Master Mode

The following fields must be programmed before entering Master mode:

1. DADR (+ IADRSZ + IADR if a 10-bit device is addressed): The device address is used to access slave devices in Read or Write mode.
2. CWGR + CKDIV + CHDIV + CLDIV: Clock waveform.
3. SVDIS: Disables Slave mode.
4. MSEN: Enables Master mode.

Note: If the TWI is already in Master mode, the device address (DADR) can be configured without disabling the Master mode.

47.9.3.3 Transfer Speed/Bit Rate

The TWI speed is defined in FLEX_TWI_CWGR. The TWI bit rate can be based either on the peripheral clock if the BRSRCCLK bit value is 0 or on a programmable clock source provided by the GCLK if the BRSRCCLK bit value is 1.

If BRSRCCLK = 1, the bit rate is independent of the processor/peripheral clock and thus processor/peripheral clock frequency can be changed without affecting the TWI transfer rate.

The GCLK frequency must be at least three times lower than the peripheral clock frequency.

47.9.3.4 Master Transmitter Mode

This operating mode is not available if High-speed mode is selected.

47.10.52 SPI Interrupt Disable Register

Name: FLEX_SPI_IDR

Address: 0xF8034418 (0), 0xF8038418 (1), 0xFC010418 (2), 0xFC014418 (3), 0xFC018418 (4)

Access: Write-only

31	30	29	28	27	26	25	24
RXFPTEF	TXFPTEF	RXFTHF	RXFFF	RXFEF	TXFTHF	TXFFF	TXFEF
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	CMP	UNDES	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
–	–	–	–	OVRES	MODF	TDRE	RDRF

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

RDRF: Receive Data Register Full Interrupt Disable

TDRE: SPI Transmit Data Register Empty Interrupt Disable

MODF: Mode Fault Error Interrupt Disable

OVRES: Overrun Error Interrupt Disable

NSSR: NSS Rising Interrupt Disable

TXEMPTY: Transmission Registers Empty Disable

UNDES: Underrun Error Interrupt Disable

CMP: Comparison Interrupt Disable

TXFEF: TXFEF Interrupt Disable

TXFFF: TXFFF Interrupt Disable

TXFTHF: TXFTHF Interrupt Disable

RXFEF: RXFEF Interrupt Disable

RXFFF: RXFFF Interrupt Disable

RXFTHF: RXFTHF Interrupt Disable

TXFPTEF: TXFPTEF Interrupt Disable

RXFPTEF: RXFPTEF Interrupt Disable

48.5.8 Test Modes

The UART supports three test modes. These modes of operation are programmed by using the CHMODE field in UART_MR.

The Automatic Echo mode allows a bit-by-bit retransmission. When a bit is received on the URXD line, it is sent to the UTXD line. The transmitter operates normally, but has no effect on the UTXD line.

The Local Loopback mode allows the transmitted characters to be received. UTXD and URXD pins are not used and the output of the transmitter is internally connected to the input of the receiver. The URXD pin level has no effect and the UTXD line is held high, as in idle state.

The Remote Loopback mode directly connects the URXD pin to the UTXD line. The transmitter and the receiver are disabled and have no effect. This mode allows a bit-by-bit retransmission.

Figure 48-15: Test Modes

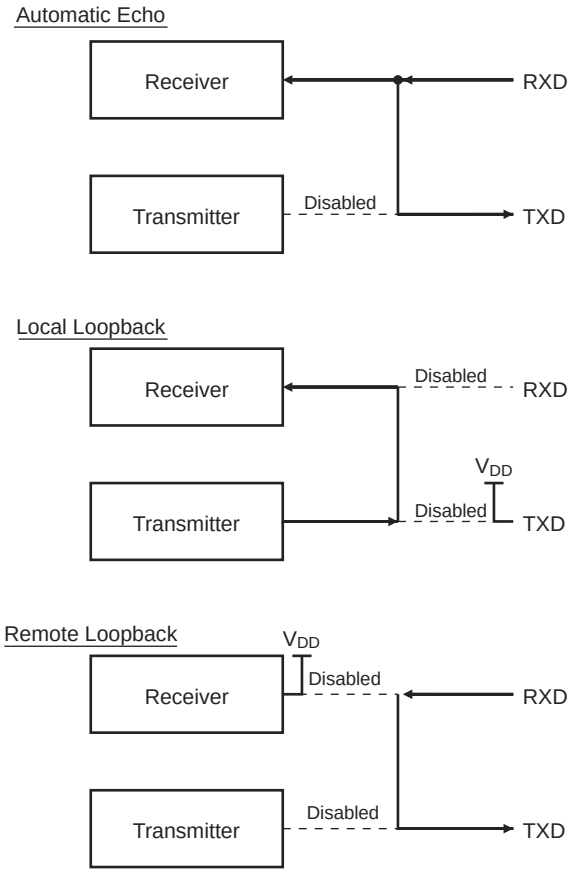


Figure 49-19: TDRE in Single Data Mode and TXRDYM=0

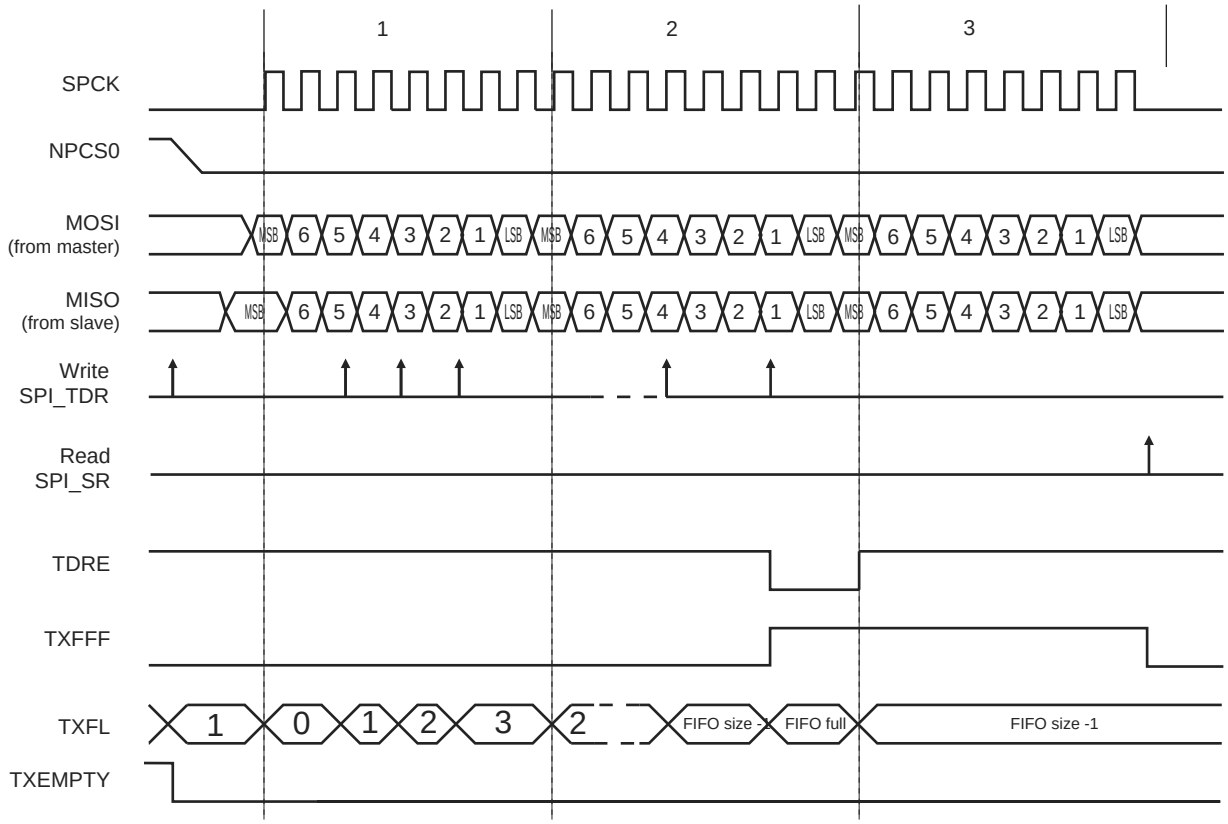
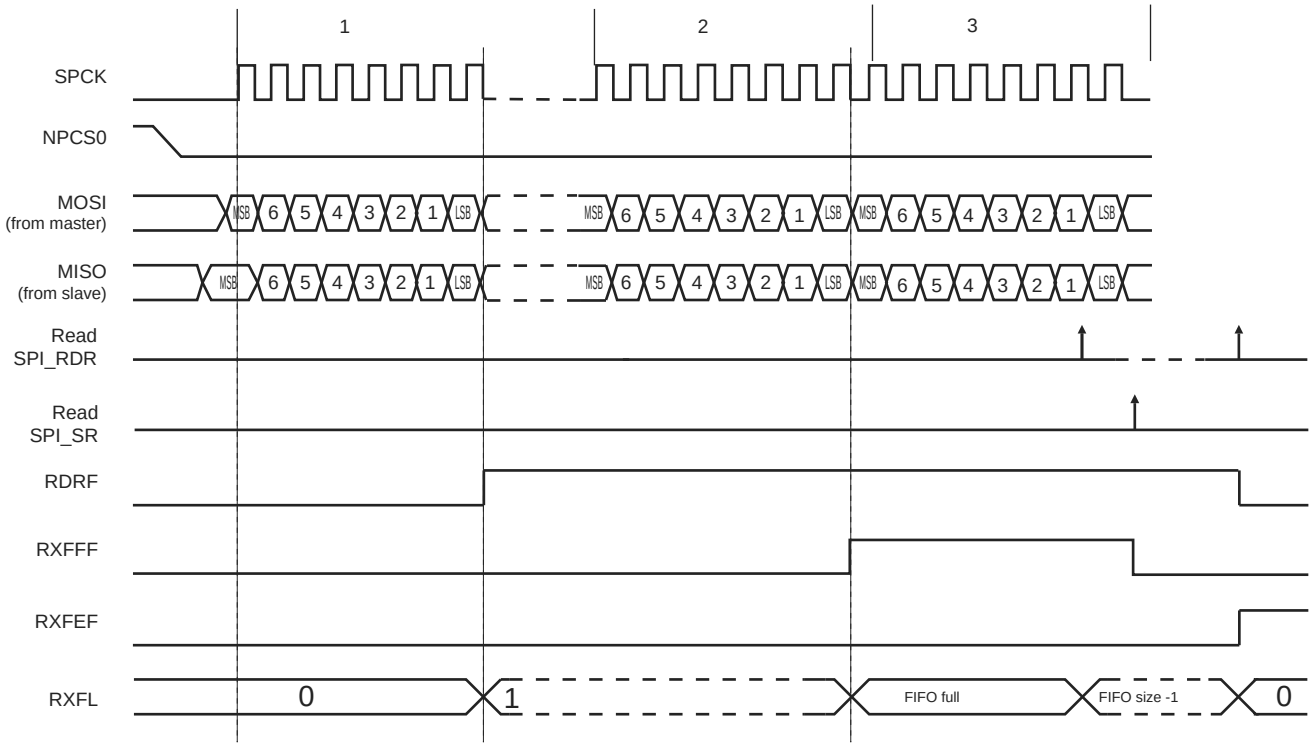


Figure 49-20: RDRF in Single Data Mode and RXRDYM=0



53.6.6 MCAN RAM Watchdog Register

Name: MCAN_RWD

Address: 0xF8054014 (0), 0xFC050014 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
WDV							
7	6	5	4	3	2	1	0
WDC							

The RAM Watchdog monitors the Message RAM response time. A Message RAM access via the MCAN's Generic Master Interface starts the Message RAM Watchdog Counter with the value configured by MCAN_RWD.WDC. The counter is reloaded with MCAN_RWD.WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag MCAN_IR.WDI is set. The RAM Watchdog Counter is clocked by the system bus clock (peripheral clock).

WDC: Watchdog Configuration (read/write)

Start value of the Message RAM Watchdog Counter. The counter is disabled when WDC is cleared.

WDV: Watchdog Value (read-only)

Watchdog Counter Value for the current message located in RAM.

QDEN: Quadrature Decoder Enabled

0: Disabled.

1: Enables the QDEC (filter, edge detection and quadrature decoding).

Quadrature decoding (direction change) can be disabled using QDTRANS bit.

One of the POSEN or SPEEDEN bits must be also enabled.

POSEN: Position Enabled

0: Disable position.

1: Enables the position measure on channel 0 and 1.

SPEEDEN: Speed Enabled

0: Disabled.

1: Enables the speed measure on channel 0, the time base being provided by channel 2.

QDTRANS: Quadrature Decoding Transparent

0: Full quadrature decoding logic is active (direction change detected).

1: Quadrature decoding logic is inactive (direction change inactive) but input filtering and edge detection are performed.

EDGPHA: Edge on PHA Count Mode

0: Edges are detected on PHA only.

1: Edges are detected on both PHA and PHB.

INVA: Inverted PHA

0: PHA (TIOA0) is directly driving the QDEC.

1: PHA is inverted before driving the QDEC.

INVB: Inverted PHB

0: PHB (TIOB0) is directly driving the QDEC.

1: PHB is inverted before driving the QDEC.

INVIDX: Inverted Index

0: IDX (TIOA1) is directly driving the QDEC.

1: IDX is inverted before driving the QDEC.

SWAP: Swap PHA and PHB

0: No swap between PHA and PHB.

1: Swap PHA and PHB internally, prior to driving the QDEC.

IDXPHB: Index Pin is PHB Pin

0: IDX pin of the rotary sensor must drive TIOA1.

1: IDX pin of the rotary sensor must drive TIOB0.

AUTOC: AutoCorrection of missing pulses

0 (DISABLED): The detection and autocorrection function is disabled.

1 (ENABLED): The detection and autocorrection function is enabled.

MAXFILT: Maximum Filter

1–63: Defines the filtering capabilities.

Pulses with a period shorter than MAXFILT+1 peripheral clock cycles are discarded. For more details on MAXFILT constraints, see Section 54.6.16.2 “Input Preprocessing”

MAXCMP: Maximum Consecutive Missing Pulses

0: The flag MPE in TC_QISR never rises.

54.7.18 TC QDEC Interrupt Disable Register

Name: TC_QIDR

Address: 0xF800C0CC (0), 0xF80100CC (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	MPE	QERR	DIRCHG	IDX

IDX: Index

0: No effect.

1: Disables the interrupt when a rising edge occurs on IDX input.

DIRCHG: Direction Change

0: No effect.

1: Disables the interrupt when a change on rotation direction is detected.

QERR: Quadrature Error

0: No effect.

1: Disables the interrupt when a quadrature error occurs on PHA, PHB.

MPE: Consecutive Missing Pulse Error

0: No effect.

1: Disables the interrupt when an occurrence of MAXCMP consecutive missing pulses has been detected.

CES: Counter Event Selection

The bit CES defines when the channel counter event occurs when the period is center-aligned (flag CHIDx in PWM Interrupt Status Register 1).

CALG = 0 (Left Alignment):

0/1: The channel counter event occurs at the end of the PWM period.

CALG = 1 (Center Alignment):

0: The channel counter event occurs at the end of the PWM period.

1: The channel counter event occurs at the end of the PWM period and at half the PWM period.

UPDS: Update Selection

When the period is center aligned, the bit UPDS defines when the update of the duty cycle, the polarity value/mode occurs after writing the corresponding update registers.

CALG = 0 (Left Alignment):

0/1: The update always occurs at the end of the PWM period after writing the update register(s).

CALG = 1 (Center Alignment):

0: The update occurs at the next end of the PWM period after writing the update register(s).

1: The update occurs at the next end of the PWM half period after writing the update register(s).

DPOLI: Disabled Polarity Inverted

0: When the PWM channel x is disabled (CHIDx(PWM_SR) = 0), the OCx output waveform is the same as the one defined by the CPOL bit.

1: When the PWM channel x is disabled (CHIDx(PWM_SR) = 0), the OCx output waveform is inverted compared to the one defined by the CPOL bit.

TCTS: Timer Counter Trigger Selection

0: The comparator of the channel x (OCx) is used as the trigger source for the Timer Counter (TC).

1: The counter events of the channel x is used as the trigger source for the Timer Counter (TC).

DTE: Dead-Time Generator Enable

0: The dead-time generator is disabled.

1: The dead-time generator is enabled.

DTHI: Dead-Time PWMHx Output Inverted

0: The dead-time PWMHx output is not inverted.

1: The dead-time PWMHx output is inverted.

DTLI: Dead-Time PWMLx Output Inverted

0: The dead-time PWMLx output is not inverted.

1: The dead-time PWMLx output is inverted.

PPM: Push-Pull Mode

0: The Push-Pull mode is disabled for channel x.

1: The Push-Pull mode is enabled for channel x.

For this example, the 512-bit message is:

0x61626380000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000018

and the expected SHA-256 result is:

0xba7816bf_8f01cfea_414140de_5dae2223_b00361a3_96177a9c_b410ff61_f20015ad

If the message has not already been stored in the system memory, the first step is to convert the input message to little-endian before writing to the SHA_IDATARx registers. This would result in a write of:

SHA_IDATAR0 = 0x80636261...... SHA_IDATAR15 = 0x18000000

The data in the output message digest registers, SHA_IODATARx, contain SHA_IODATAR0 = 0xbf1678ba... SHA_IODATAR7 = 0xad1500f2 which is the little-endian format of 0xba7816bf,..., 0xf20015ad.

Reading SHA_IODATAR0 to SHA_IODATAR1 and storing into a little-endian memory system forces hash results to be stored in the same format as the message.

When the output message is read, the user can convert back to big-endian for a resulting message value of:

0xba7816bf_8f01cfea_414140de_5dae2223_b00361a3_96177a9c_b410ff61_f20015ad

61.4.10 Security Features

61.4.10.1 Unspecified Register Access Detection

When an unspecified register access occurs, the URAD bit in the SHA_ISR is set. Its source is then reported in the Unspecified Register Access Type field (URAT). Only the last unspecified register access is available through the URAT field.

Several kinds of unspecified register accesses can occur:

- SHA_IDATARx written during data processing in DMA mode
- SHA_IODATARx read during data processing
- SHA_MR written during data processing
- Write-only register read access

The URAD bit and the URAT field can only be reset by the SWRST bit in the SHA_CR.

66.7.1.1 Recommended Crystal Characteristics

The following characteristics are applicable to the operating temperature range T_A = -40°C to 85°C and to the worst case of power supply, unless otherwise specified.

Table 66-18: Recommended Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistance	FREQ = 00, 11	–	–	100	Ω
		FREQ = 10, 01	–	–	80	
CM	Motional Capacitance	FREQ = 00	5	–	9	fF
		FREQ = 01, 10, 11	1.3	–	3.2	
CS	Shunt Capacitance	FREQ = 00, 01, 10	–	–	3	pF
		FREQ = 11	–	–	1.3	
$C_{CRYSTAL}$	Allowed crystal capacitive load	From crystal specification FREQ = 00, 01, 11 FREQ = 10	 12.5 8	–	 18 12.5	pF

66.7.1.2 XIN Clock Characteristics

Table 66-19: XIN Clock Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN Clock Frequency	–	–	–	50	MHz
t_{CPXIN}	XIN Clock Period	–	20	–	–	ns
t_{CHXIN}	XIN Clock High Half-period	–	0.4 x t_{CPXIN}	–	0.6 x t_{CPXIN}	ns
t_{CLXIN}	XIN Clock Low Half-period	–	0.4 x t_{CPXIN}	–	0.6 x t_{CPXIN}	ns
CIN	XIN Input Capacitance	–	–	–	25	pF
RIN	XIN Pulldown Resistor	–	–	–	500	kΩ
VIN	XIN Voltage	–	V_{DDOSC}	–	V_{DDOSC}	V

Note: These characteristics apply only when the Main Oscillator is in Bypass mode (i.e., when MOSCEN = 0 and OSCBYPASS = 1 in CKGR_MOR). Refer to “PMC Clock Generator Main Oscillator Register” in the section "Power Management Controller (PMC)".

66.7.2 12 MHz RC Oscillator Characteristics

Table 66-20: 12 MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	RC Oscillator Frequency	@ 25°C	11.63	–	12.12	MHz
t_{START}	Startup Time	–	–	–	15	µs
Duty	Duty Cycle	–	45	50	55	%
I_{DDON}	Current Consumption	After startup time	–	160	350	µA