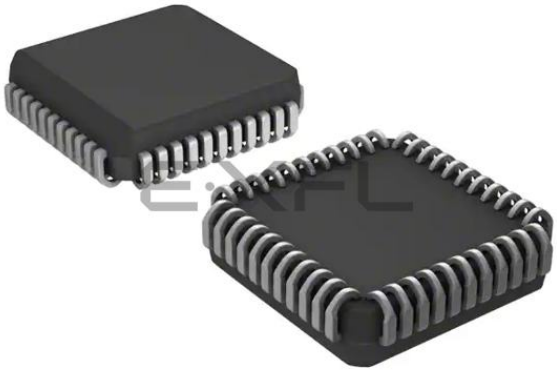

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8609316vsg

Z86093

ROMLESS CMOS 8-BIT Z8® MCU

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86093	N/A	236	16

Note: *General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages
- 3.0- to 5.5-Volt Operating Range
- Available Temperature Ranges:
  S = 0°C to 70°C
  E = –40°C to +105°C
- 32 Input/Output Lines
- Six Vectored, Prioritized Interrupts from Six Different Sources
- Two On-Chip Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Power-On Reset (POR)
- Low-Power Consumption
- Expanded Register File (ERF)
- Programmable Interrupt Polarity
- Optional Features Required Selections:
  - ROM Protect - Disabled
  - RAM Protect - Disabled
  - WDT - Enabled by Software Only
  - Autolatches - Enabled
  - Clock Source - Crystal, Ceramic Resonator, LC, or External Clock Drive

GENERAL DESCRIPTION

The Z86093 is a ROMless member of Zilog's Z8® MCU single-chip family with 236 bytes of general purpose RAM. It is available in a 40-pin DIP package, 44-pin PLCC package, and 44-pin QFP package. The Z86093 offers the use of external memory which enables this Z8® MCU to be used where code flexibility is required. Zilog's CMOS MCUs offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86093 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers.

For applications demanding powerful I/O capabilities, the Z86093's 32 input and output lines are grouped into four ports, and are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Two on-chip counter/timers, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-chip comparators process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

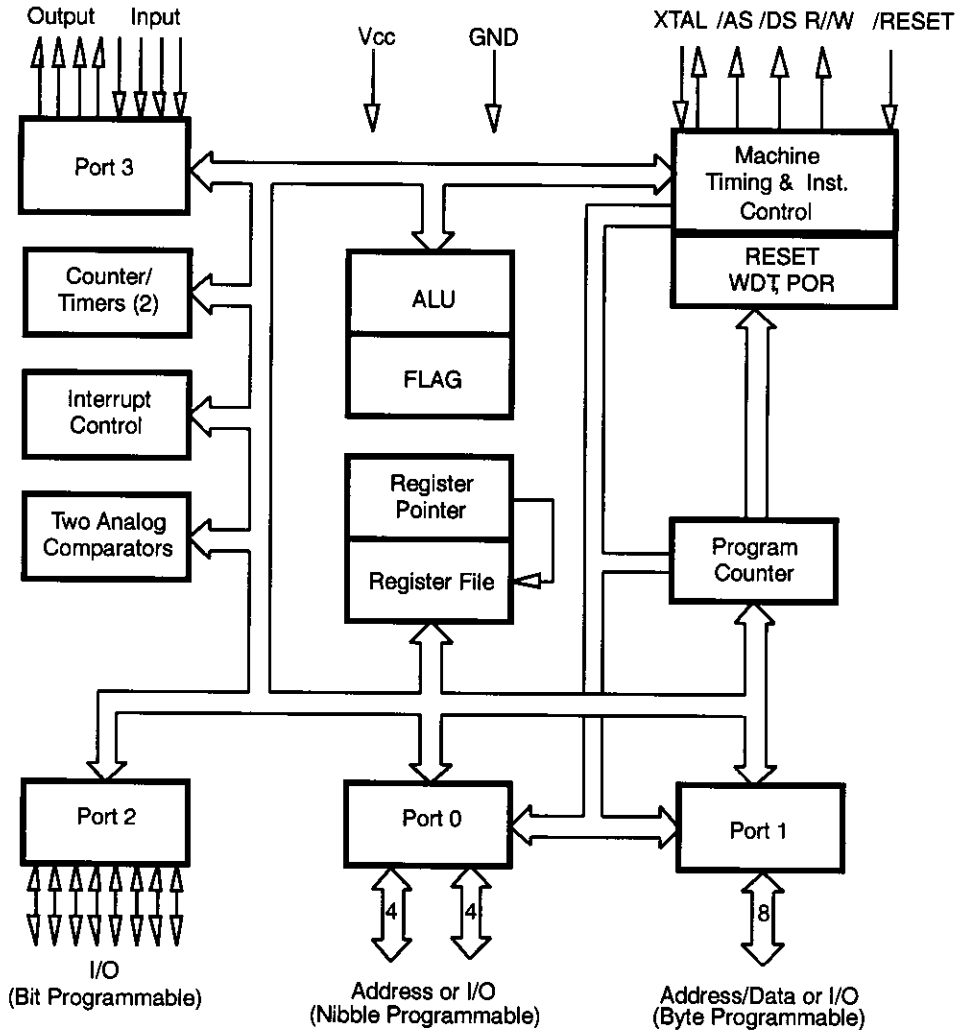

Figure 1. Functional Block Diagram

PIN DESCRIPTION

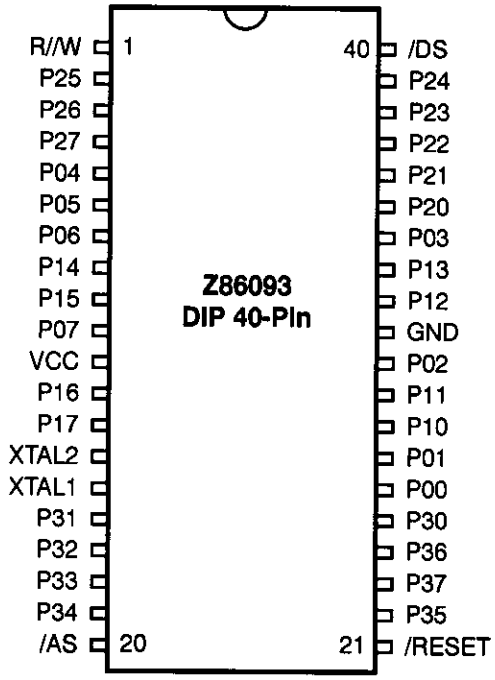

Figure 2. 40-Pin DIP Assignments

Table 1. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output
8-9	P14-15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output
15	XTAL1	Crystal, Oscillator Clock	Input
16-18	P31-33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output

Table 1. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-01	Port 0, Pin 0,1	In/Output
28-29	P10-11	Port 1, Pin 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-13	Port 1, Pin 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

PIN DESCRIPTION (Continued)

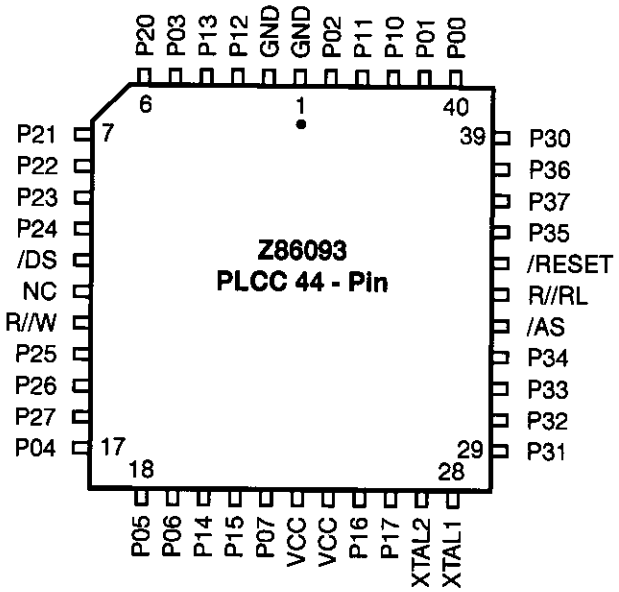

Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	N/C	Not Connected	
13	R//W	Read/Write	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output
20-21	P14-15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23,24	V_{CC}	Power Supply	
25-26	P16-17	Port 1, Pins 6,7	In/Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
27	XTAL2	Crystal, Oscillator Clock	Output
28	XTAL1	Crystal, Oscillator Clock	Input
29-31	P31-33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless Control	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-01	Port 0, Pins 0,1	In/Output
42-43	P10-11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

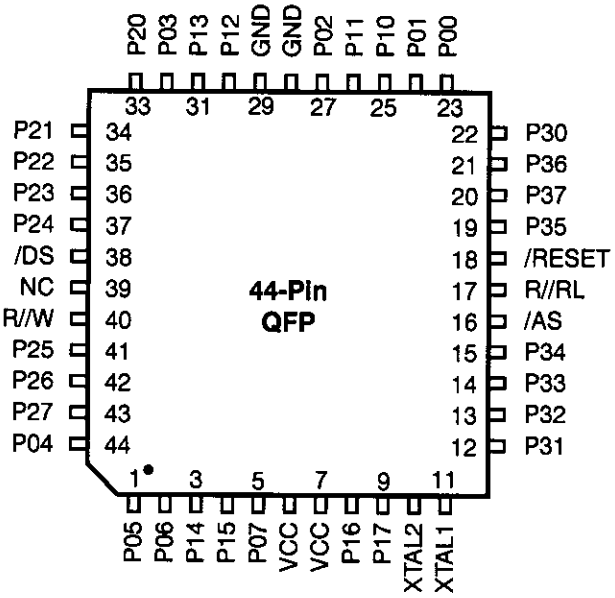

Figure 4. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output
3-4	P14-15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	V_{CC}	Power Supply	
8-9	P16-17	Port 1 Pins 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless Control	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-01	Port 0, Pins 0,1	In/Output
25-26	P10-11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	N/C	Not Connected	
40	R//W	Read/Write	Output
41-43	P25-27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7.)

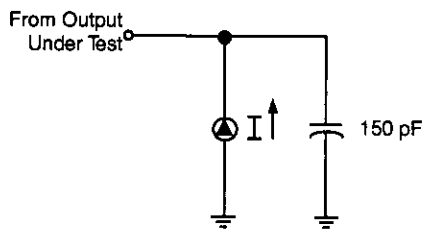

Figure 5. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.6	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.4	V	I_{OL} = +12 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.8	V		13
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.6	V		13
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		13
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.6	V		13
V_{OLR}	Reset Output Low Voltage	3.0V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	13
		5.5V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	13
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	2	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V	-20	-130	-18	-130	-60	µA		
		5.5V	-20	-180	-18	-180	-85	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	4
		5.5V		25		25	20	mA	@ 16 MHz	4
		3.0V		15		15	5	mA	@ 12 MHz	4
		5.5V		20		20	15	mA	@ 12 MHz	4

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		5.5V		10		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,11, 14
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	0.7	10	3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	1.4	15	1.4	20	5	µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.0V	-0.6	-5	-0.6	-7	-3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-8	-1.0	-10	-6	µA	$0V < V_{IN} < V_{CC}$	9
V_{LV}	V_{CC} Low Voltage Protection Voltage				2.0	3.3	2.8	V	4 MHz max Int. CLK Freq.	7,15
			2.2	3.1			2.8		6 MHz max Int. CLK Freq.	7,14
V_{OH}	Output High Voltage (Low EMI Mode)	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -0.5 mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.0V		0.6		0.6	0.2	V	I_{OL} = 1.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = 1.0 mA	

Notes:

1. Typicals are at V_{CC} = 5.0V and 3.3V.
2. GND = 0V.
3. The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC}=3.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC}-5.0V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 10 pF.
6. Same as note [4] except inputs at V_{CC}.
7. The V_{LV} voltage increases as the temperature decreases and will overlap lower V_{CC} operating region.
8. Standard Mode (not Low EMI).
9. Auto Latch (Mask Option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Z86093 only.
14. 0°C to 70°C (standard temperature).
15. –40°C to 150°C (extended temperature).

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

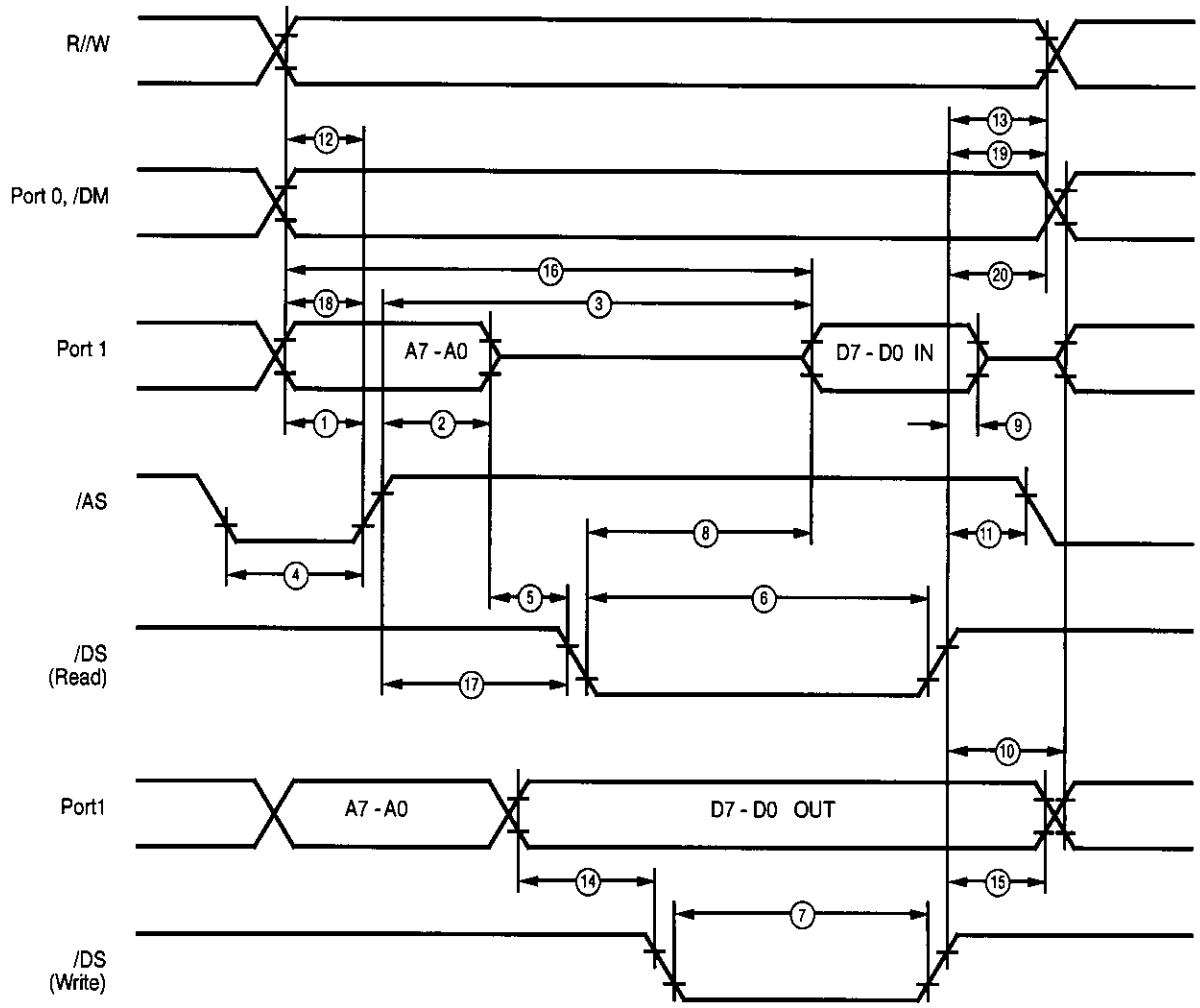

Figure 6. External I/O or Memory Read and Write Timing Table

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3]	T_A=0°C to 70°C				T_A = –40°C to +105°C				Units	Notes
				12 MHz		16 MHz		12 MHz		16 MHz			
			V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25		ns	2
			5.5	35		25		35		25			2
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	1,2
			5.5		250		180		250		180	ns	2
4	TwAS	/AS Low Width	3.0	55		40		55		40		ns	2
			5.5	55		40		55		40		ns	2
5	TdAS(DS)	Address Float to /DS Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135		ns	1,2
			5.5	200		135		200		135		ns	1,2
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80		ns	1,2
			5.5	110		80		110		80		ns	1,2
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	1,2
			5.5		150		75		150		75	ns	1,2
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.0	0		0		0		0		ns	2
			5.5	0		0		0		0		ns	2
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50		ns	2
			5.5	55		50		55		50		ns	2
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35		ns	2
			5.5	45		35		45		55		ns	2
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	3.0	45		25		45		25		ns	2
			5.5	45		25		45		25		ns	2
13	TdDS(R/W)	/DS Rise to R//W Not Valid	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25		ns	2
			5.5	55		25		55		25		ns	2
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	1,2
			5.5		310		230		310		230	ns	1,2
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45		ns	2
			5.5	65		45		65		45		ns	2
18	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30		ns	2
			5.5	35		30		35		30		ns	2

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	Note [3] V_{CC}	T_A=0°C to 70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = –40°C to +105°C 12 MHz Min	Max	16 MHz Min	Max	Units	Notes
19	TdDs(DM)	/DS Rise to DM	3.0	45		35		45		35		ns	2
		Valid Delay	5.5	45		35		45		35		ns	2
20	ThDS(AS)	/DS Valid to Address	3.0	45		35		45		35		ns	2
		Valid Home Time	5.5	45		35		45		35		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

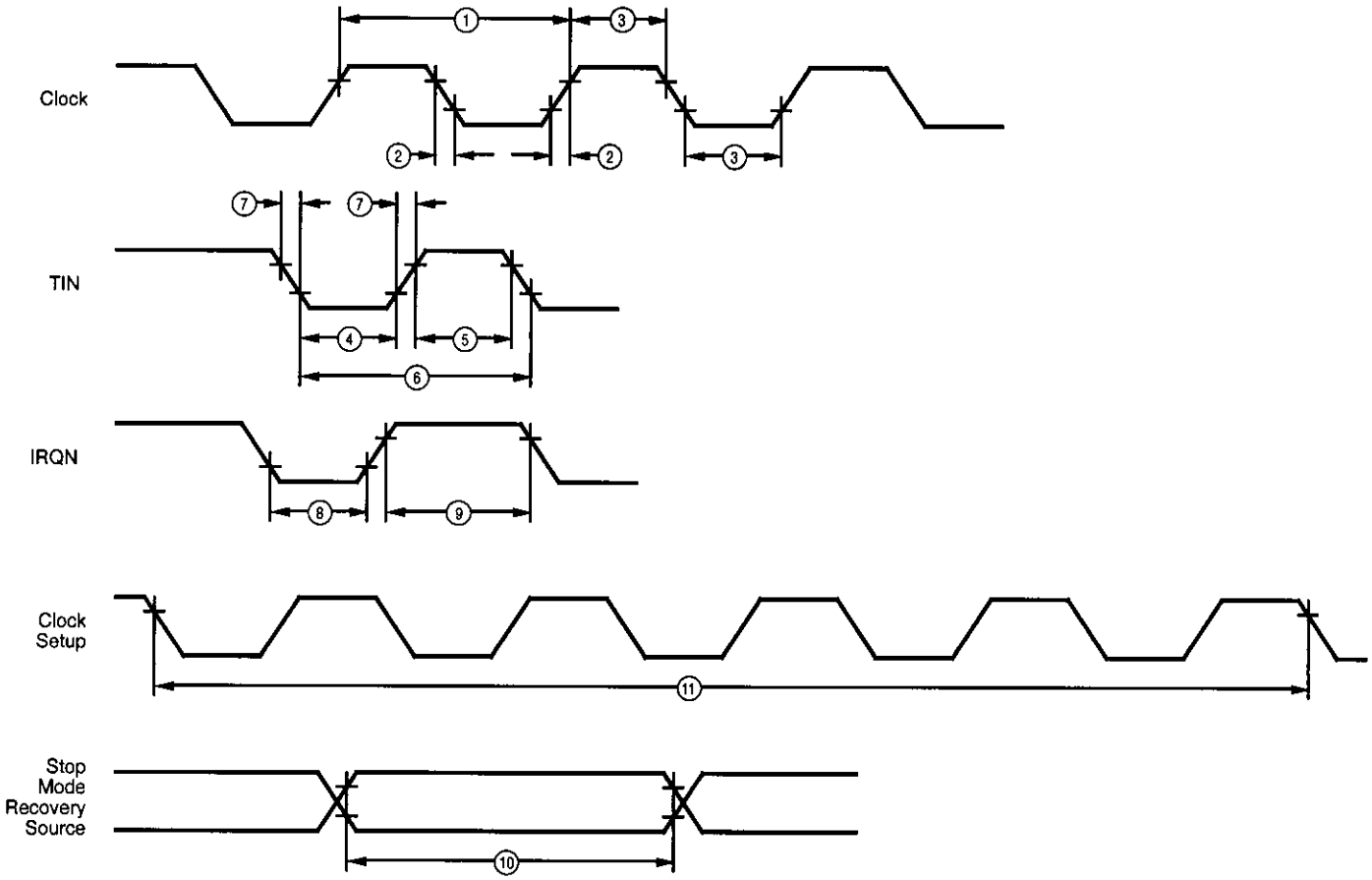

Figure 7. Additional Timing

AC CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3] V_{CC}	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A =–4 0°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1,7
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1,7
			3.0V	250	DC	250	DC	250	DC	250	DC	ns	1,8
			5.5V	250	DC	250	DC	250	DC	250	DC	ns	1,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
			3.0V	125		125		125		125		ns	1,8
			5.5V	125		125		125		125		ns	1,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		4
			5.5V		5TpC		5TpC		5TpC		5TpC		4
													D1, D0 [Note]
12	Twdt	Watch-Dog Timer Delay Time before time-out	3.0V	7		7		7		7		ms	0, 0 [5]
			5.5V	3.5		3.5		3.5		3.5		ms	0, 0 [5]
			3.0V	14		14		14		14		ms	0, 1 [5]
			5.5V	7		7		7		7		ms	0, 1 [5]
			3.0V	28		28		28		28		ms	1, 0 [5]
			5.5V	14		14		14		14		ms	1, 0 [5]
			3.0V	112		112		112		112		ms	1, 1 [5]
			5.5V	56		56		56		56		ms	1, 1 [5]

No	Symbol	Parameter	Note [3] V_{CC}	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A =–4 0°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
13	TPOR	Power-On Reset Delay	3.0V	3	24	3	24	3	25	3	25	ms	
			5.5V	1.5	13	1.5	13	1	14	1	14	ms	

Notes: :

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. Standard Oscillator mode, Pcon RegD7=1.
8. Maximum frequency for external XTAL Clock is 4MHz when using low EMI oscillator mode, Pcon Reg D7=0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 8 MHz Min	Max	T_A = 40°C to +105°C 8 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
			3.0V	125	DC	125	DC	ns	1,7
			5.5V	125	DC	125	DC	ns	1,7
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	1,7
			5.5V		25		25	ns	1,7
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
			3.0V	62		62		ns	1,7
			5.5V	62		62		ns	1,7
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7
			5.5V	70		70		ns	1,7
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			1,7
			5.5V	3TpC		3TpC			1,7
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7
			5.5V	4TpC		4TpC			1,7
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7
			5.5V		100		100	ns	1,7
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,2,7
			5.5V	70		70		ns	1,2,7
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			1,3,7
			5.5V	3TpC		3TpC			1,3,7
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			1,2,7
			5.5V	3TpC		2TpC			1,2,7
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4
			5.5V	12		12		ns	4
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		4,9
			5.5V		5TpC		5TpC		4,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0.
8. Maximum frequency for external XTAL clock is 4 MHz when using low EMI Oscillator mode Pcon Reg.D7=0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Handshake Timing Diagrams

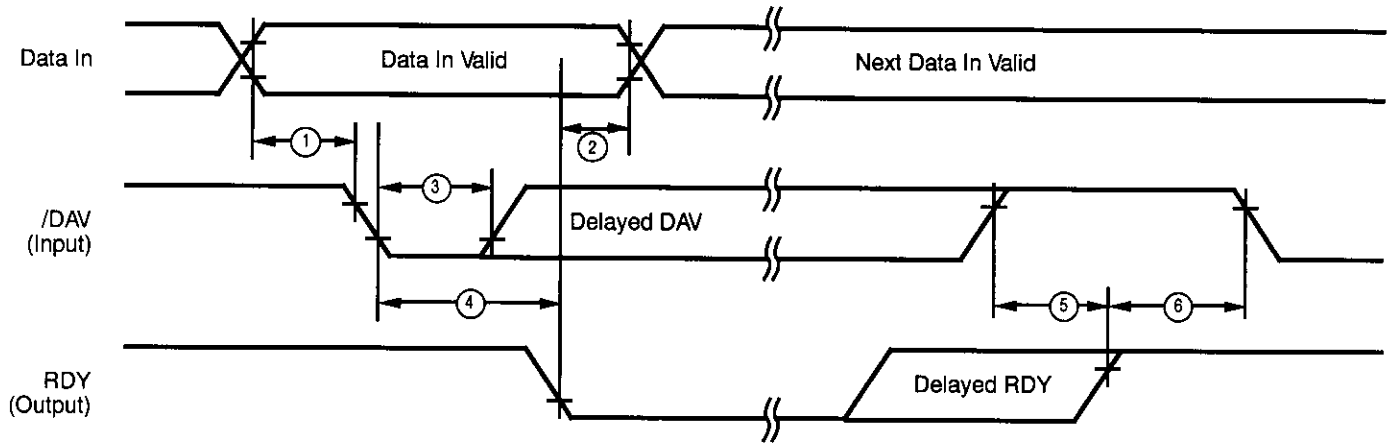

Figure 8. Input Handshake Timing

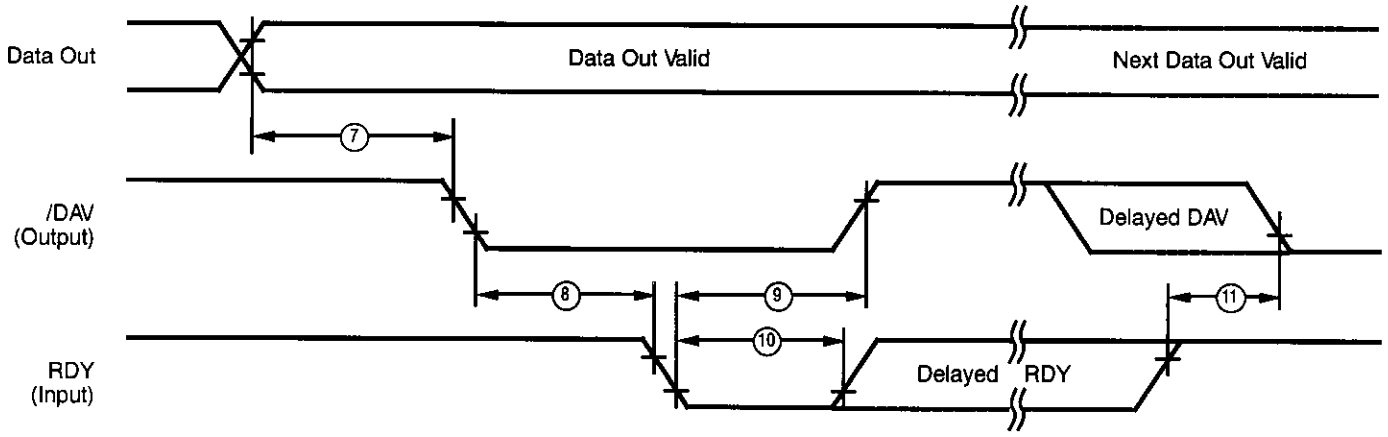

Figure 9. Output Handshake Timing

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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