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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2437fv

Configuration of This Manual

This manual comprises the following items:

1. General Precautions in the Handling of MPU/MCU Products
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions for This Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index

2.5.2 Memory Data Formats

Figure 2.10 shows the data formats in memory. The H8S/2600 CPU can access word data and longword data in memory, but word or longword data must begin at an even address. If an attempt is made to access word or longword data at an odd address, no address error occurs but the least significant bit of the address is regarded as 0, so the access starts at the preceding address. This also applies to instruction fetches.

When ER7 is used as an address register to access the stack, the operand size should be word size or longword size.

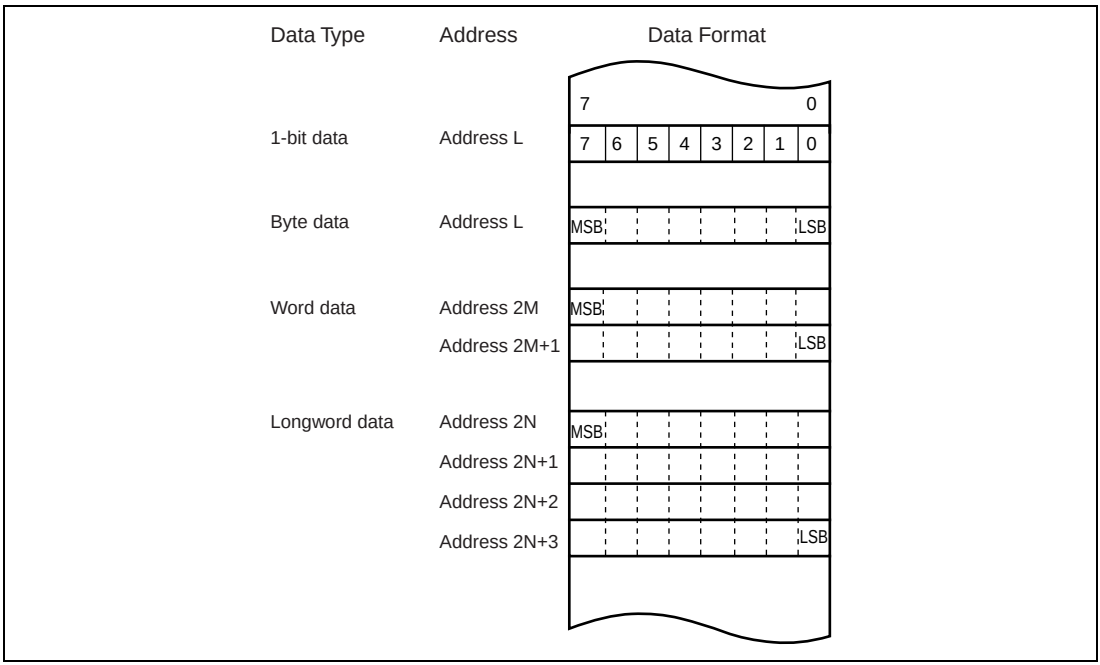


Figure 2.10 Memory Data Formats

Table 2.7 Bit Manipulation Instructions (1)

Instruction	Size*	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in a general register or memory operand to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in a general register or memory operand to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory operand and sets or clears the Z flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIAND	B	C ∧ [~ (<bit-No.> of <EAd>)] → C ANDs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIOR	B	C ∨ [~ (<bit-No.> of <EAd>)] → C ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

Note: Size refers to the operand size.
B: Byte

- Operation Field

  Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.

- Register Field

  Specifies a general register. Address registers are specified by 3 bits, data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.

- Effective Address Extension

  8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement.

- Condition Field

  Specifies the branching condition of Bcc instructions.

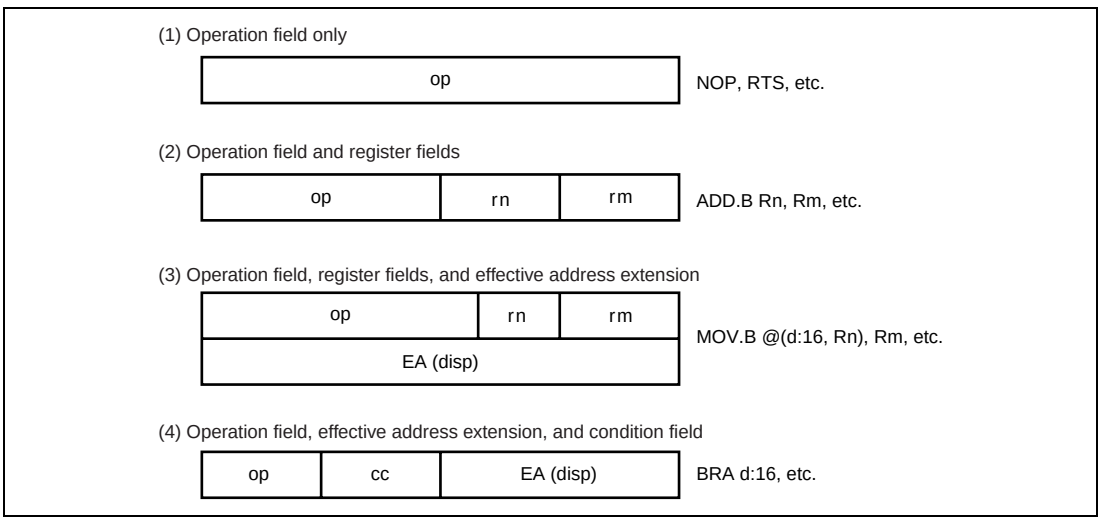


Figure 2.11 Instruction Formats (Examples)

The external extended wait function is effective when the low-speed device is connected to the external address area.

For details on multiplex extended address range, external address area, as well as bus interface specifications, refer to tables 6.4 to 6.6.

Table 6.4 Address Range and External Address Area (Multiplex Extended Mode)

Address Range	Area
H'080000 to H'FBFFFF (15 Mbytes)	Basic area
H'FC0000 to H'FCFFFF (64 kbytes)	Area 1
H'FD0000 to H'FDFFFF (64 kbytes)	Area 2
H'FE0000 to H'FEFFFF (64 kbytes)	Area 3
H'FF0000 to H'FF9FFF (40 kbytes)	Integrated with basic area when RAME = 0 (use prohibited)

Table 6.5 Bus Specifications for Multiplex Extended Bus Interface (Address Cycle)

ASTn	AWn	WMSn1	WMSn0	WCn1	WCn0	Number of Access States	Number of Program Wait States
—	0	—	—	—	—	2	0
	1	—	—	—	—	2	1

[Legend]

n = 1 to 3

Table 6.6 Bus Specifications for Multiplex Extended Bus Interface (Data Cycle)

ASTn	AWn	WMSn1	WMSn0	WCn1	WCn0	Number of Access States	Number of Program Wait States
0	—	—	—	—	—	2	0
1	—	0	1	—	—	3	0
	—	0	0	0	0	3	0
		1	*		1	3	1
				1	0	3	2
					1	3	3

[Legend]

n = 1 to 3

*: Don't care.

[Legend]

x: Don't care

Notes: 1. When TIOCD0/TCLKBS = 0, MD3 to MD0 = B'0000, and IOD3 to IOD0 = B'10xx, this pin functions as the TIOCD0 input pin.

2. When TIOCD0/TCLKBS = 0 and TPSC2 to TPSC0 in one of TCR_0 to TCR2 = B′101, this pin functions as the TCLKB input pin. When TIOCB1/TCLKCS = 0 and phase-count mode is set to the TCR channel 1, this pin functions as the TCLKB input pin.

- P22/TIOCC0/TCLKA/A10/AD10

  When the TIOCC0/TCLKAS bit in PTCNT2 is cleared to 0, this pin can be used as the TIOCC0/TCLKA pin.

  According to operating modes, the TPU channel 0 settings by the MD3 to MD0 bits in TMDR_0, the IOC3 to IOC0 bits in TIORL_0, and the CCLR2 to CCLR0 bits in TCR_0, and the combination of the TPSC2 to TPSC0 bits in TCR_0 to TCR_2, the TIOCC0/TCLKAS bit, and the P22DDR bit, pin functions change as follows.

- Extended Mode (EXPE = 1)

	Normal Extended Mode (ADMXE = 0)		Multiplex Extended Mode (ADMXE = 1)
P22DDR	0	1	—
Pin function	P22 input pin	A10 output pin	AD10 I/O pin
	TIOCC0 input pin*[1]		
	TCLKA input pin*[1]		

- Single-Chip Mode (EXPE = 0)

TIOCC0/ TCLKAS	0			1	
TPU channel 0 setting	Table below (2)		Table below (1)		—
P22DDR	0	1	—	0	1
Pin function	P22 input pin	P22 output pin	TIOCC0 output pin	P22 input pin	P22 output pin
	TIOCC0 input pin*[1]				
	TCLKA input pin*[2]				

7.4.4 Port 3 Pull-Up MOS Control Register (P3PCR)

P3PCR controls the on or off state of input pull-up MOSs for port 3.

Bit	Bit Name	Initial Value	R/W	Description
7	P37PCR	0	R/W	• In normal extended mode Operation is not affected. • In multiplex extended mode Operates as single-chip mode • In single-chip mode When the pins are in the input states, the corresponding input pull-up MOS is turned on when a P3PCR bit is set to 1.
6	P36PCR	0	R/W	
5	P35PCR	0	R/W	
4	P34PCR	0	R/W	
3	P33PCR	0	R/W	
2	P32PCR	0	R/W	
1	P31PCR	0	R/W	
0	P30PCR	0	R/W	

7.4.5 Pin Functions

When the corresponding bit in PTCNT1 is set to 1, port 3 pins can be used as interrupt input pins ($\overline{\text{ExIRQ3}}$ to $\overline{\text{ExIRQ0}}$). In normal extended mode, port 3 pins function as data I/O pins. In multiplex extended mode, operation of port 3 pins is the same as that in single-chip mode. The relationship between register setting values and pin functions is as follows.

- P37/D15

  The pin function is switched as shown below according to the operating mode and the P37DDR bit.

	Extended Mode (EXPE = 1)			Single-Chip Mode (EXPE = 0)	
	Normal Extended Mode (ADMXE = 0)	Multiplex Extended Mode (ADMXE = 1)			
P37DDR	—	0	1	0	1
Pin function	D15 I/O pin	P37 input pin	P37 output pin	P37 input pin	P37 output pin

TPU channel 0 setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

[Legend]

x: Don't care

Notes: 1. When TIOCD0/TCLKBS = 1, MD3 to MD0 = B'0000, and IOD3 to IOD0 = B'10xx, this pin functions as the TIOCD0 input pin.

2. When TIOCD0/TCLKBS = 1 and TPSC2 to TPSC0 in one of TCR_0 to TCR2 = B'101, this pin functions as the TCLKB input pin. When TIOCB1/TCLKCS = 1 and phase-count mode is set to the TCR channel 1, this pin functions as the TCLKB input pin.

- P96/ϕ

According to the setting of the P96DDR bit, the pin function is switched as shown below.

P96DDR	0	1
Pin function	P96 input pin	ϕ output pin

- P95/$\overline{AS}$/$\overline{AH}$

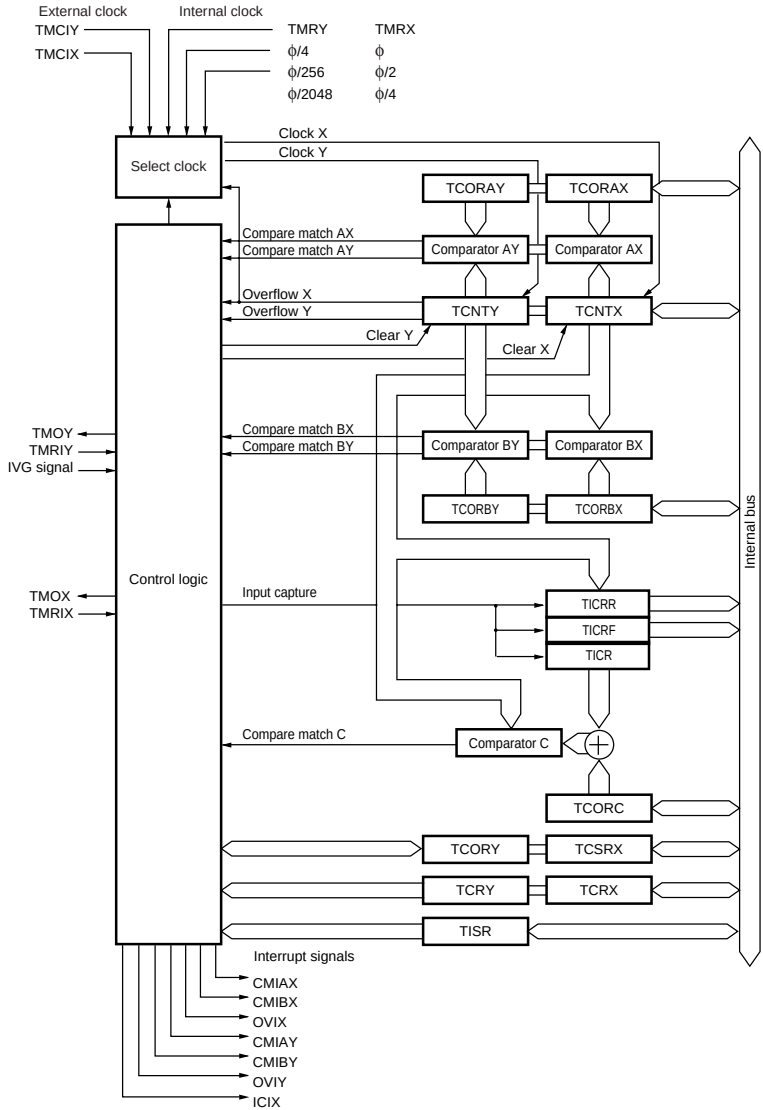
  According to the operating mode and combination of the ASOE bit and the P95DDR bit, the pin function is switched as shown below.

- Extended Mode (EXPE = 1)

	Normal Extended Mode (ADMXE = 0)			Multiplex Extended Mode (ADMXE = 1)
ASOE	0		1	—
P95DDR	0	1	—	—
Pin function	P95 input pin	P95 output pin	$\overline{AS}$ output pin	$\overline{AH}$ output pin

- Single-Chip Mode (EXPE = 0)

P95DDR	0	1
Pin function	P95 input pin	P95 output pin



[Legend]

TCORAY:	Time constant register AY	TCORAX:	Time constant register AX
TCORBY:	Time constant register BY	TCORBX:	Time constant register BX
TCNTY:	Timer counter Y	TCNTX:	Timer counter X
TCSRY:	Timer control/status register Y	TCSRX:	Timer control/status register X
TCRY:	Timer control register Y	TCRX:	Timer control register X
TISR:	Timer input select register	TICR:	Input capture register
		TCORC:	Time constant register
		TICRR:	Input capture register R
		TICRF:	Input capture register F

Figure 11.2 Block Diagram of 8-Bit Timer (TMRY and TMRX)

Table 11.2 Clock Input to TCNT and Count Condition

	TCR			TECR		
System	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR0	0	0	0	—	—	Disables clock input
	0	0	1	—	0	Increments at falling edge of internal clock ϕ/8
	0	0	1	—	1	Increments at falling edge of internal clock ϕ/2
	0	1	0	—	0	Increments at falling edge of internal clock ϕ/64
	0	1	0	—	1	Increments at falling edge of internal clock ϕ/32
	0	1	1	—	0	Increments at falling edge of internal clock ϕ/1024
	0	1	1	—	1	Increments at falling edge of internal clock ϕ/256
	1	0	0	—	—	Increments at overflow signal from TCNT1*
TMR1	0	0	0	—	—	Disables clock input
	0	0	1	0	—	Increments at falling edge of internal clock ϕ/8
	0	0	1	1	—	Increments at falling edge of internal clock ϕ/2
	0	1	0	0	—	Increments at falling edge of internal clock ϕ/64
	0	1	0	1	—	Increments at falling edge of internal clock ϕ/128
	0	1	1	0	—	Increments at falling edge of internal clock ϕ/1024
	0	1	1	1	—	Increments at falling edge of internal clock ϕ/2048
	1	0	0	—	—	Increments at compare-match A from TCNT0*
TMRY	0	0	0	—	—	Disables clock input
	0	0	1	—	—	Increments at falling edge of internal clock ϕ/4
	0	1	0	—	—	Increments at falling edge of internal clock ϕ/256

11.5.6 Timing of Overflow Flag (OVF) Setting

The OVF flag in TCSR is set to 1 by an overflow signal output when the TCNT overflows (changes from H'FF to H'00). Figure 11.10 shows the timing of OVF flag setting.

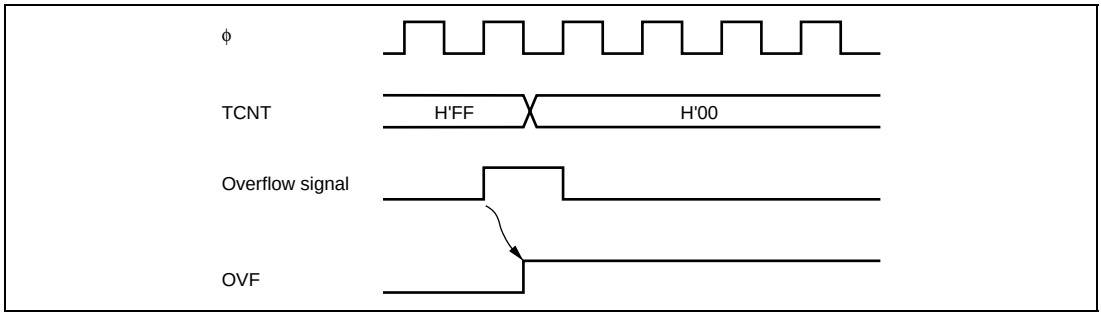


Figure 11.10 Timing of OVF Flag Setting

- Timer general register B_2 (TGRB_2)

Common Registers:

- Timer start register (TSTR)
- Timer synchro register (TSYR)

12.3.1 Timer Control Register (TCR)

TCR controls the TCNT operation for each channel. The TPU has a total of three TCR registers, one for each channel (channels 0 to 2). TCR settings should be made only when TCNT operation is stopped.

Bit	Bit Name	Initial Value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	Select the TCNT counter clearing source. See tables 12.3 and 12.4 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 1, 0
3	CKEG0	0	R/W	Select the input clock edge. When the internal clock is counted using both edges, the input clock cycle is 1/2 (example: ϕ/4 both edges = ϕ/2 rising edge). If phase counting mode is used on channels 1 and 2, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is ϕ/4 or slower. This setting is ignored if the input clock is ϕ/1 and the rising edge counting is selected. 00: Count at rising edge 01: Count at falling edge 1x: Count at both edges [Legend] x: Don't care
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	Select the TCNT counter clock. The clock source can be selected independently for each channel. See tables 12.5 to 12.7 for details.
0	TPSC0	0	R/W	

Table 13.3 HSYNCO Output Selection

TECR			TCONRO_1	TCONRO_0	HSYNCO Output Signal
HS2	HS1	HS0	HOINV	HOINV	
0	0	0	—	0	The IHO signal in channel 0 is used directly as the HSYNCO output
			—	1	The IHO signal in channel 0 is inverted before use as the HSYNCO output
		1	0	—	The IHO signal in channel 1 is used directly as the HSYNCO output
			1	—	The IHO signal in channel 1 is inverted before use as the HSYNCO output
	1	0	—	—	The input signal of the HSYNCI_0 is used as the HSYNCO output
		1	—	—	The input signal of the HSYNCI_1 is used as the HSYNCO output
1	0	0	—	—	The input signal of the CSYNCI_0 is used as the HSYNCO output
		1	—	—	The input signal of the CSYNCI_1 is used as the HSYNCO output
	1	0	—	—	Port output inverted*
		1	—	—	Setting prohibited

Note: * The PB1DR inverted value is output regardless of the PB1DDR setting.

Table 13.4 VSYNCO Output Selection

TECR	TCONRI_1	TCONRI_0	VSYNCO Output Signal
VS0	VOINV	VOINV	
0	—	0	The IVO signal in channel 0 is used directly as the VSYNCO output
	—	1	The IVO signal in channel 0 is inverted before use as the VSYNCO output
1	0	—	The IVO signal in channel 1 is used directly as the VSYNCO output
	1	—	The IVO signal in channel 1 is inverted before use as the VSYNCO output

Table 13.10 Examples of OCRAR, OCRAF, TOCR, TCORA, TCORB, TCR, and TCSR Settings

Register	Bit	Abbreviation	Contents	Description
TCR of TMRY	7	CMIEB	0	Interrupts due to compare-match and overflow are disabled
	6	CMIEA	0	
	5	OVIE	0	
	4, 3	CCLR1, CCLR0	01	TCNT is cleared by compare-match A
	2 to 0	CKS2 to CKS0	001	TCNT is incremented on internal clock: $\phi/4$
TCSR of TMRY	3 to 0	OS3 to OS0	0110	0 output on compare-match B 1 output on compare-match A
TCORA of TMRY	H'3F (example)	IHG signal period = $\phi \times 256$		
TCORB of TMRY	H'03 (example)	1 interval of IHG signal = $\phi \times 16$		
TCR of FRT	1, 0	CKS1, CKS0	01	FRC is incremented on internal clock: $\phi/8$
OCRAR of FRT	H'7FEF (example)	0 interval of IVG signal = $\phi \times 262016$		IVG signal period = $\phi \times 262144$ (1024 times IHG signal)
OCRAF of FRT	H'000F (example)	1 interval of IVG signal = $\phi \times 128$		
TOCR of FRT	6	OCRAMS	1	OCRA is set to the operating mode in which OCRAR and OCRAF are used

17.3.13 I²C Bus Shift Register (ICDRS)

ICDRS is a register that is used to transfer/receive data. In transmission, data is transferred from ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred from ICDRS to ICDRR after one byte of data is received. This register cannot be read from the CPU.

- Programming/erasing protection

  Sets protection against flash memory programming/erasing via hardware, software, or error protection.
- Programmer mode

  This mode uses the PROM programmer. The user MAT and user boot MAT can be programmed.

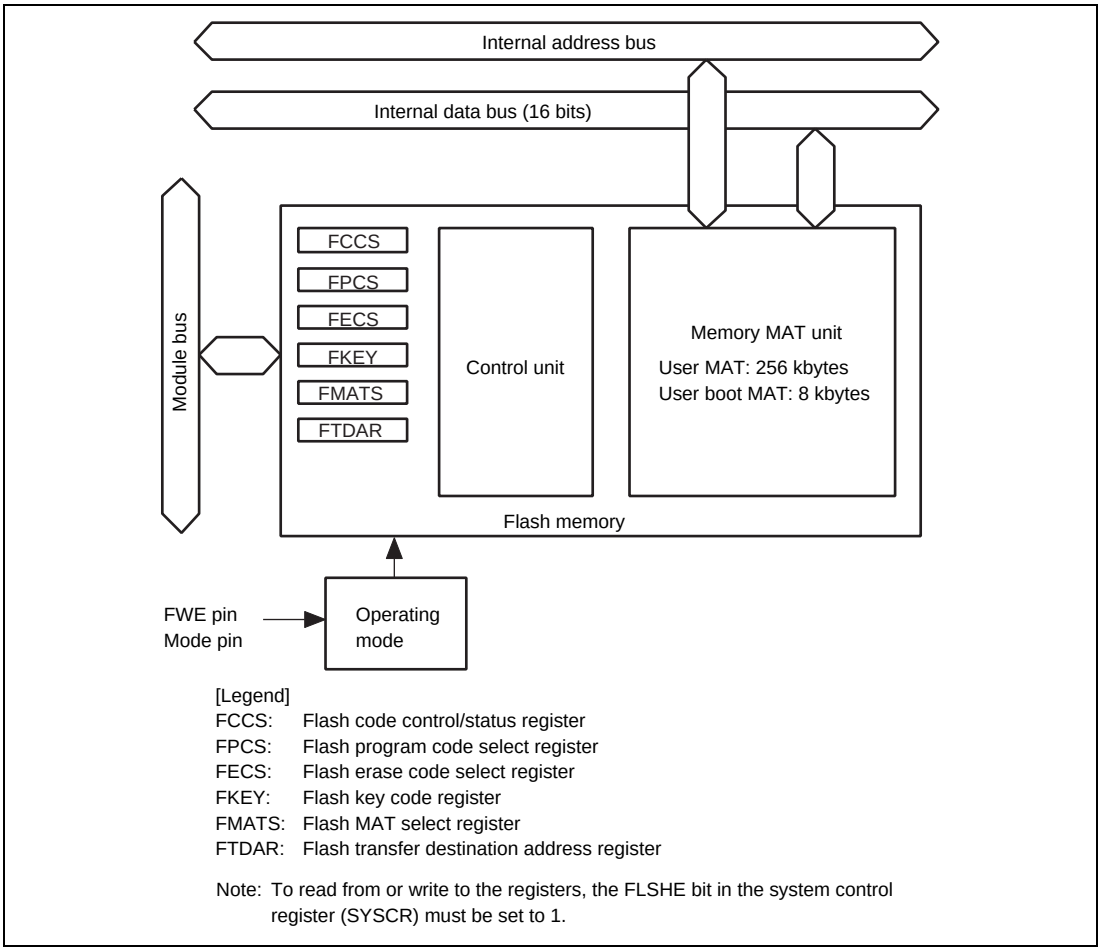


Figure 20.1 Block Diagram of Flash Memory

The system configuration diagram in boot mode is shown in figure 20.6. For details on the pin setting in boot mode, see table 20.5. The NMI and other interrupts are ignored in boot mode. However, the NMI and other interrupts should be disabled in the system.

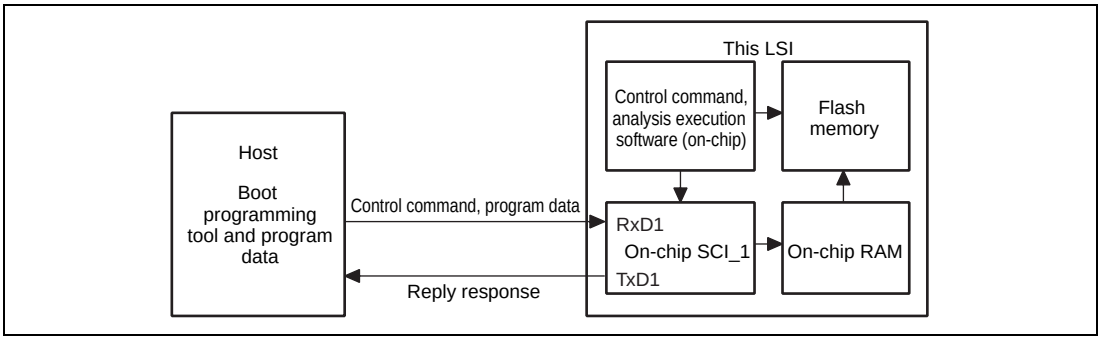


Figure 20.6 System Configuration in Boot Mode

(1) SCI Interface Setting by Host

When boot mode is initiated, this LSI measures the low period of asynchronous SCI-communication data (H'00), which is transmitted consecutively by the host. The SCI transmit/receive format should be set to 8-bit data, 1 stop bit, and no parity. This LSI calculates the bit rate which is transmitted by the host according to the measured low period and transmits the bit adjustment end sign (1 byte of H'00) to the host. The host must confirm that this bit adjustment end sign (H'00) has been received normally and transmit 1 byte of H'55 to this LSI. When reception is not performed normally, boot mode is initiated again (reset) and the operation described above must be executed. The bit rates of the host and this LSI do not match according to the bit rate transmitted by the host and system clock frequency of this LSI. To operate the SCI normally, the transfer bit rate of the host must be set to 4,800 bps, 9,600 bps, or 19,200 bps.

The system clock frequency, which can automatically adjust the transfer bit rate of the host and the bit rate of this LSI, is shown in table 20.6. Boot mode must be initiated in the range of this system clock.

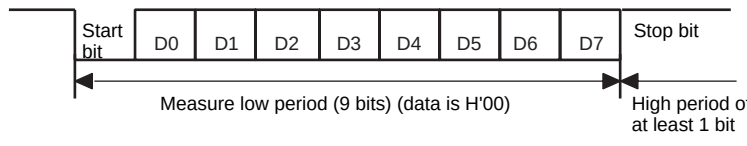


Figure 20.7 Automatic-Bit-Rate Adjustment Operation of SCI

Item	Storable/Executable Area			Selected MAT	
	On-chip RAM	User MAT	External Space (Extended Mode)	User MAT	Embedded Program Storage MAT
Operation for erasure error	○	×	○	○	
Operation for FKEY clear	○	×	○	○	

(11) Memory Read

The boot program will return the data in the specified address.

Command	H'52	Size	Area	Read address	
	Read size				SUM

- Command: H'52 (one byte): Memory read
- Size (one byte): Amount of data that represents the area, read address, and read size (fixed to 9)
- Area (one byte)
  H'00: User boot MAT
  H'01: User MAT
  An address error occurs when the area setting is incorrect.
- Read address (four bytes): Start address to be read from
- Read size (four bytes): Size of data to be read
- SUM (one byte): Checksum

Response	H'52	Read size						
	Data	···						
	SUM							

- Response: H'52 (one byte): Response to memory read
- Read size (four bytes): Size of data to be read
- Data (n bytes): Data for the read size from the read address
- SUM (one byte): Checksum

Error Response	H'D2	ERROR

- Error response: H'D2 (one byte): Error response to memory read
- ERROR: (one byte): Error code
  H'11: Checksum error
  H'2A: Address error
  The read address is not in the MAT.
  H'2B: Size error
  The read size exceeds the MAT.

(12) User Boot MAT Sum Check

The boot program will return the byte-by-byte total of the contents of the bytes of the user boot MAT, as a four-byte value.

Command	H'4A

- Command, H'4A, (one byte): Sum check for user boot MAT