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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427igh6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427igh6</a>

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## 2.1 Full compatibility throughout the family

The STM32F427xx and STM32F429xx devices are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F427xx and STM32F429xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F427xx and STM32F429xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F42x family remains simple as only a few pins are impacted.

[Figure 1](#), [Figure 2](#), and [Figure 3](#), give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

**Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package**

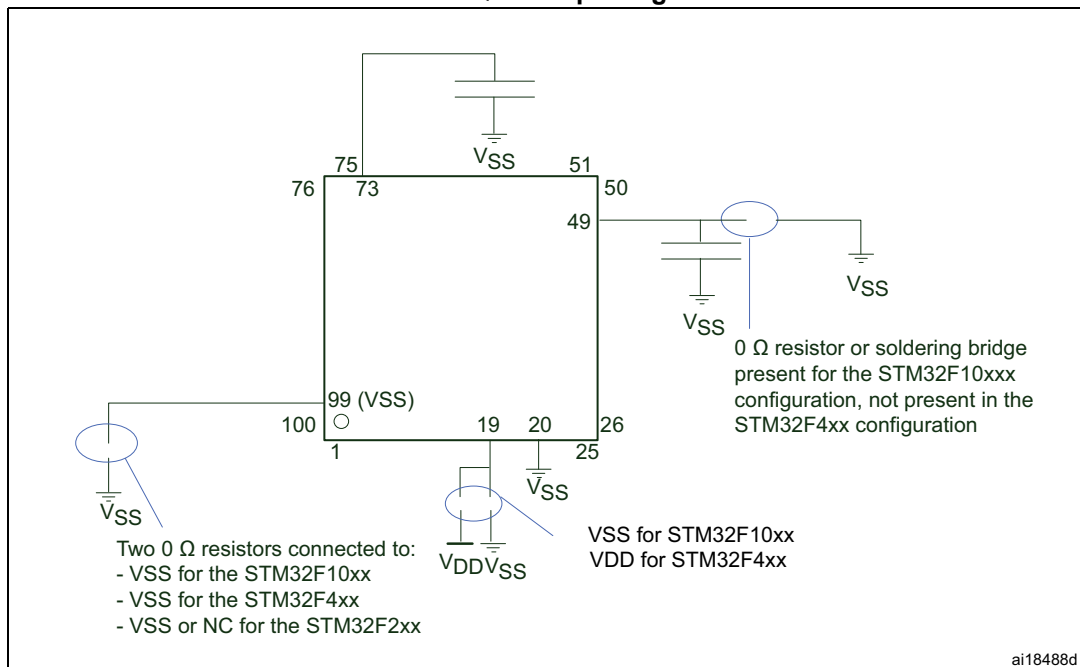
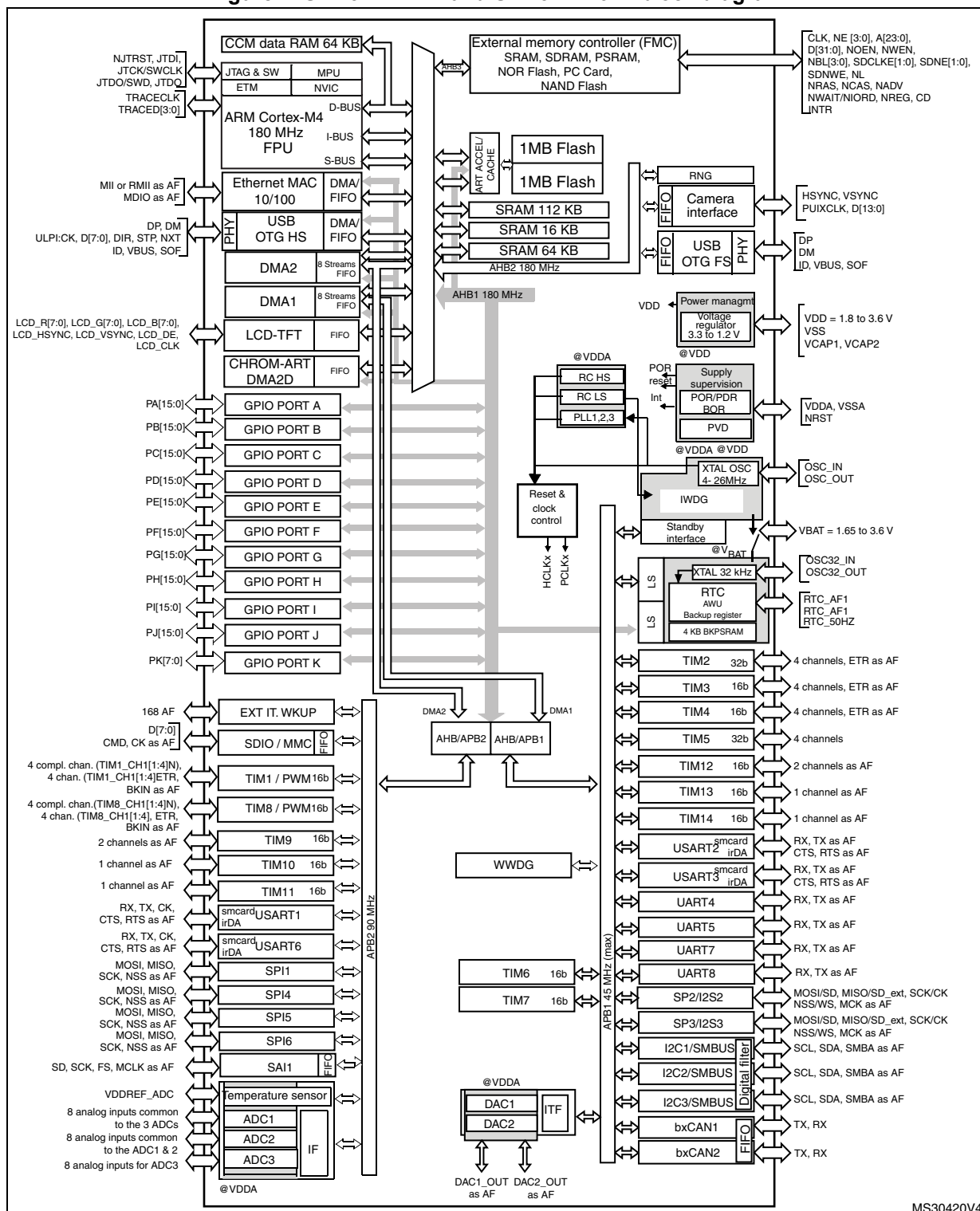


Figure 4. STM32F427xx and STM32F429xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.
2. The LCD-TFT is available only on STM32F429xx devices.

## 3 Functional overview

### 3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F42x family is compatible with all ARM tools and software.

*Figure 4* shows the general block diagram of the STM32F42x family.

*Note:* Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

### 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

### 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 180 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 180 MHz while the maximum frequency of the high-speed APB domains is 90 MHz. The maximum allowed frequency of the low-speed APB domain is 45 MHz.

The devices embed a dedicated PLL (PLL12S) and PLLSAI which allows to achieve audio class performance. In this case, the I<sup>2</sup>S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

### 3.15 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to application note AN2606 for details.

### 3.16 Power supply schemes

- $V_{DD} = 1.7$  to  $3.6$  V: external power supply for I/Os and the internal regulator (when enabled), provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 1.7$  to  $3.6$  V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL.  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.
- $V_{BAT} = 1.65$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

*Note:*  $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

### 3.17 Power supply supervisor

#### 3.17.1 Internal reset ON

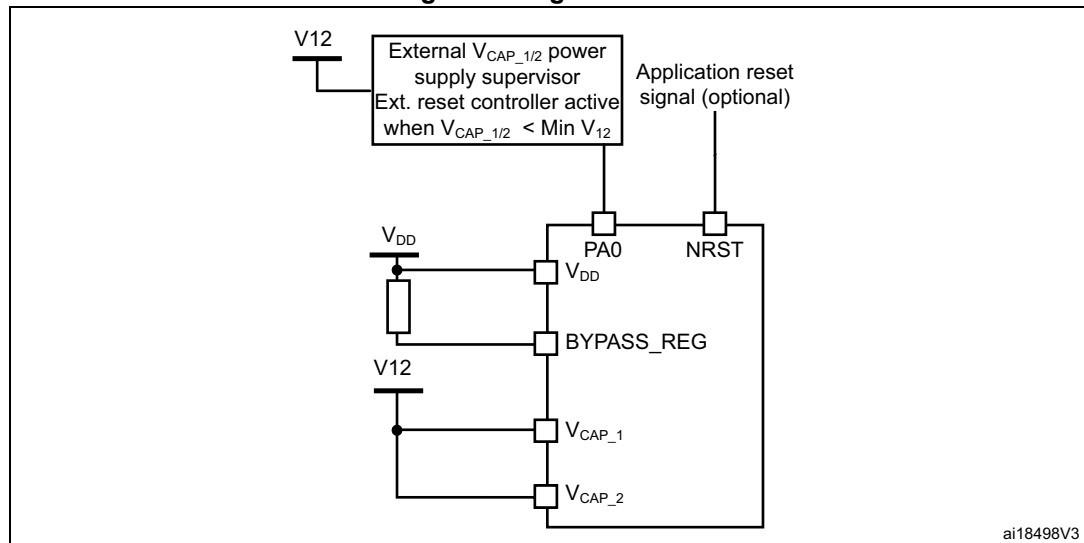
On packages embedding the PDR\_ON pin, the power supply supervisor is enabled by holding PDR\_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the  $V_{12}$  logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

**Figure 8. Regulator OFF**



The following conditions must be respected:

- $V_{DD}$  should always be higher than  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to avoid current injection between power domains.
- If the time for  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to reach  $V_{12}$  minimum value is faster than the time for  $V_{DD}$  to reach 1.7 V, then PA0 should be kept low to cover both conditions: until  $V_{CAP\_1}$  and  $V_{CAP\_2}$  reach  $V_{12}$  minimum value and until  $V_{DD}$  reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to reach  $V_{12}$  minimum value is slower than the time for  $V_{DD}$  to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If  $V_{CAP\_1}$  and  $V_{CAP\_2}$  go below  $V_{12}$  minimum value and  $V_{DD}$  is higher than 1.7 V, then a reset must be asserted on PA0 pin.

**Note:** The minimum value of  $V_{12}$  depends on the maximum frequency targeted in the application (see [Table 17: General operating conditions](#)).

### 3.21 $V_{BAT}$ operation

The  $V_{BAT}$  pin allows to power the device  $V_{BAT}$  domain from an external battery, an external supercapacitor, or from  $V_{DD}$  when no external battery and an external supercapacitor are present.

$V_{BAT}$  operation is activated when  $V_{DD}$  is not present.

The  $V_{BAT}$  pin supplies the RTC, the backup registers and the backup SRAM.

*Note:* When the microcontroller is supplied from  $V_{BAT}$ , external interrupts and RTC alarm/events do not exit it from  $V_{BAT}$  operation.

When  $PDR\_ON$  pin is not connected to  $V_{DD}$  (Internal Reset OFF), the  $V_{BAT}$  functionality is no more available and  $V_{BAT}$  pin should be connected to  $V_{DD}$ .

### 3.22 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

[Table 6](#) compares the features of the advanced-control, general-purpose and basic timers.



FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

### 3.33 Universal serial bus on-the-go full-speed (OTG\_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of  $320 \times 35$  bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

### 3.34 Universal serial bus on-the-go high-speed (OTG\_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of  $1 \text{ Kbit} \times 35$  with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
4	4	D1	B2	4	D9	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	D2	B3	5	E8	5	B2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	V <sub>SS</sub>	S	-	-	-	-
-	-	-	-	-	-	-	F5	V <sub>DD</sub>	S	-	-	-	-
6	6	E5	C1	6	C11	6	C1	V <sub>BAT</sub>	S	-	-	-	-
-	-	NC (2)	D2	7	-	7	C2	PI8	I/O	FT	(3) (4)	EVENTOUT	TAMP_2
7	7	E4	D1	8	D10	8	D1	PC13	I/O	FT	(3) (4)	EVENTOUT	TAMP_1
8	8	E1	E1	9	D11	9	E1	PC14- OSC32_IN (PC14)	I/O	FT	(3) (4)	EVENTOUT	OSC32_IN (5)
9	9	F1	F1	10	E11	10	F1	PC15- OSC32_OUT (PC15)	I/O	FT	(3) (4)	EVENTOUT	OSC32_OUT <sup>(5)</sup>
-	-	-	-	-	-	-	G5	V <sub>DD</sub>	S	-	-	-	-
-	-	E2	D3	11	-	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	E3	12	-	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	NC (2)	E4	13	-	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	F6	F2	14	E7	14	F2	V <sub>SS</sub>	S	-	-	-	-
-	-	F4	F3	15	E10	15	F4	V <sub>DD</sub>	S	-	-	-	-

Table 11. FMC pin definition (continued)

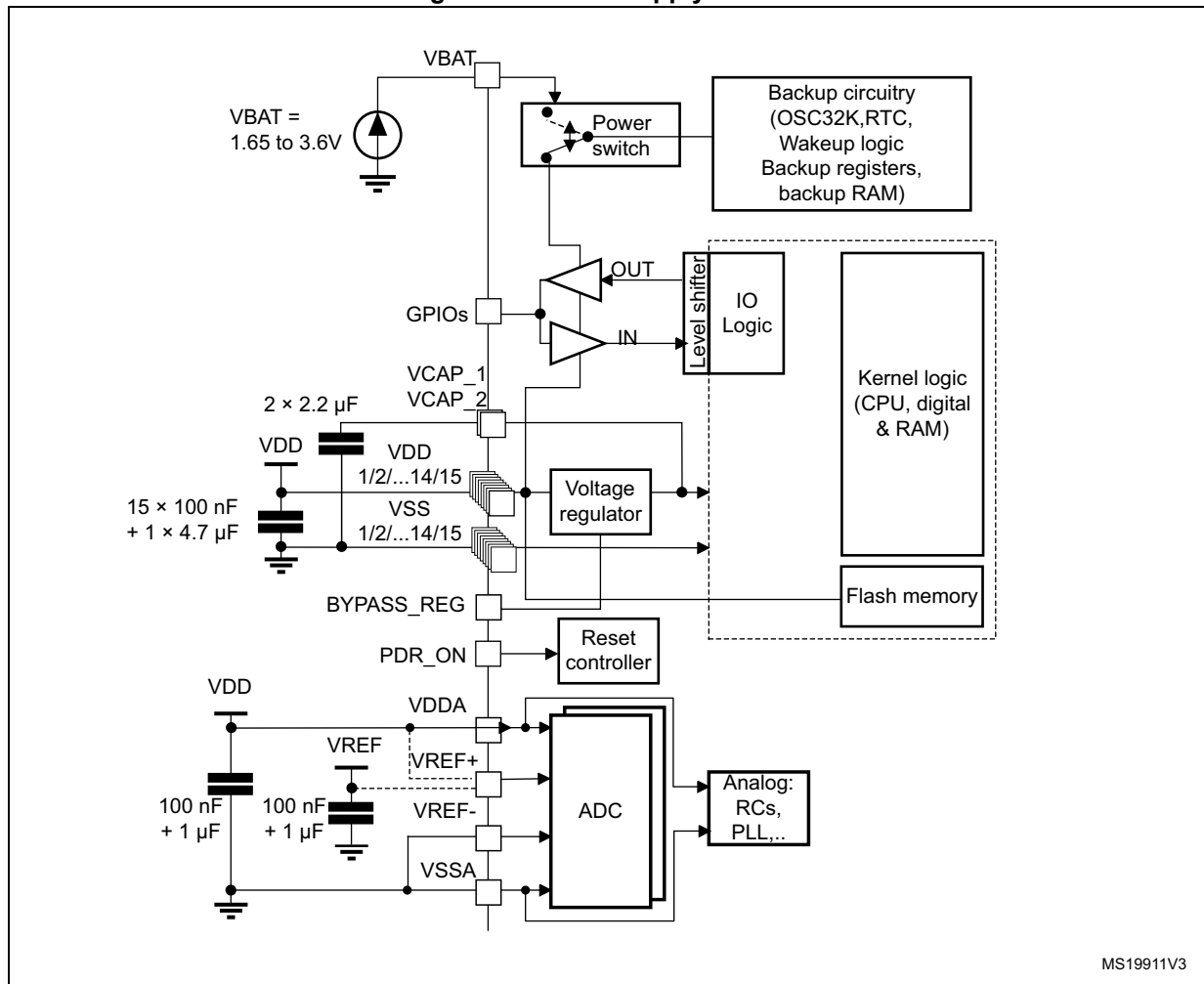
Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	D8	DA8	D8	D8
PE12	D9	D9	DA9	D9	D9
PE13	D10	D10	DA10	D10	D10
PE14	D11	D11	DA11	D11	D11
PE15	D12	D12	DA12	D12	D12
PD8	D13	D13	DA13	D13	D13
PD9	D14	D14	DA14	D14	D14
PD10	D15	D15	DA15	D15	D15
PH8		D16			D16
PH9		D17			D17
PH10		D18			D18
PH11		D19			D19
PH12		D20			D20
PH13		D21			D21
PH14		D22			D22
PH15		D23			D23
PI0		D24			D24
PI1		D25			D25
PI2		D26			D26
PI3		D27			D27
PI6		D28			D28
PI7		D29			D29
PI9		D30			D30
PI10		D31			D31
PD7		NE1	NE1	NCE2	
PG9		NE2	NE2	NCE3	
PG10	NCE4_1	NE3	NE3		
PG11	NCE4_2				
PG12		NE4	NE4		
PD3		CLK	CLK		
PD4	NOE	NOE	NOE	NOE	
PD5	NWE	NWE	NWE	NWE	
PD6	NWAIT	NWAIT	NWAIT	NWAIT	
PB7		NL(NADV)	NL(NADV)		

Table 11. FMC pin definition (continued)

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF6	NIORD				
PF7	NREG				
PF8	NIOWR				
PF9	CD				
PF10	INTR				
PG6				INT2	
PG7				INT3	
PE0		NBL0	NBL0		NBL0
PE1		NBL1	NBL1		NBL1
PI4		NBL2			NBL2
PI5		NBL3			NBL3
PG8					SDCLK
PC0					SDNWE
PF11					SDNRAS
PG15					SDNCAS
PH2					SDCKE0
PH3					SDNE0
PH6					SDNE1
PH7					SDCKE1
PH5					SDNWE
PC2					SDNE0
PC3					SDCKE0
PB5					SDCKE1
PB6					SDNE1

## 6.1.6 Power supply scheme

Figure 22. Power supply scheme



1. To connect BYPASS\_REG and PDR\_ON pins, refer to [Section 3.17: Power supply supervisor](#) and [Section 3.18: Voltage regulator](#)
2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the  $V_{DD}$  pin.
4.  $V_{DDA}=V_{DD}$  and  $V_{SSA}=V_{SS}$ .

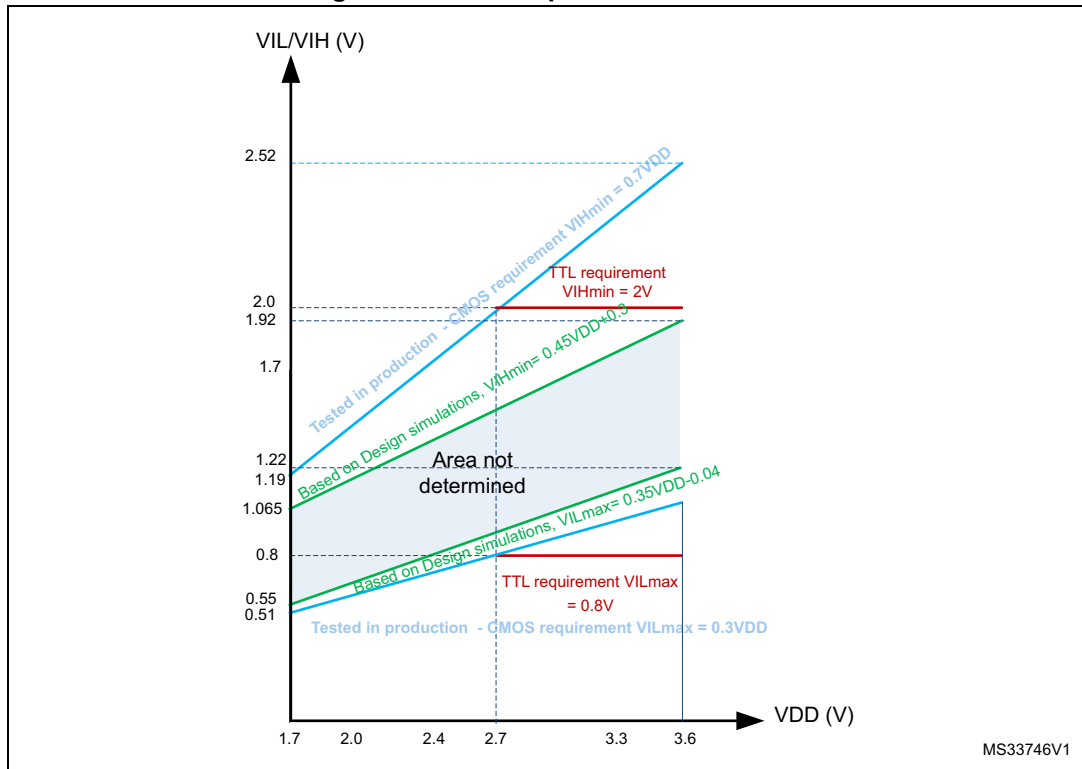
**Caution:** Each power supply pair ( $V_{DD}/V_{SS}$ ,  $V_{DDA}/V_{SSA}$  ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

**Table 31. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)<sup>(1)</sup>**

Symbol	Parameter	Conditions	f <sub>HCLK</sub> (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I <sub>DD12</sub>	I <sub>DD</sub>	I <sub>DD12</sub>	I <sub>DD</sub>	
I <sub>DD12</sub> / I <sub>DD</sub>	Supply current in RUN mode from V <sub>12</sub> and V <sub>DD</sub> supply	All Peripherals enabled	168	77.8	1.3	76.8	1.0	mA
			150	70.8	1.3	69.8	1.0	
			144	64.5	1.3	63.6	1.0	
			120	49.9	1.2	49.3	0.9	
			90	39.2	1.3	38.7	1.0	
			60	27.2	1.2	26.8	0.9	
			30	15.6	1.2	15.4	0.9	
			25	13.6	1.2	13.5	0.9	
		All Peripherals disabled	168	38.2	1.3	37.0	1.0	
			150	34.6	1.3	33.4	1.0	
			144	31.3	1.3	30.3	1.0	
			120	24.0	1.2	23.2	0.9	
			90	18.1	1.4	18.0	1.0	
			60	12.9	1.2	12.5	0.9	
			30	7.2	1.2	6.9	0.9	
			25	6.3	1.2	6.1	0.9	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

Figure 35. FT I/O input characteristics



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ) except PC13, PC14, PC15 and PI8 which can sink or source up to  $\pm 3$  mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#). In particular:

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 15](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 15](#)).

**Table 61. I2C analog filter characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{AF}$	Maximum pulse width of spikes that are suppressed by the analog filter	50 <sup>(2)</sup>	260 <sup>(3)</sup>	ns

1. Guaranteed by design.
2. Spikes with widths below  $t_{AF(min)}$  are filtered.
3. Spikes with widths above  $t_{AF(max)}$  are not filtered

### SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 62](#) for the SPI interface are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 10$
- Capacitive load  $C = 30$  pF
- Measurement points are done at CMOS levels:  $0.5V_{DD}$

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 62. SPI dynamic characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{SCK}$ $1/t_c(SCK)$	SPI clock frequency	Master mode, SPI1/4/5/6, 2.7 V≤V <sub>DD</sub> ≤3.6 V		-	-	45	MHz
		Slave mode, SPI1/4/5/6, 2.7 V≤V <sub>DD</sub> ≤3.6 V	Receiver			45	
			Transmitter/ full-duplex			38 <sup>(2)</sup>	
		Master mode, SPI1/2/3/4/5/6, 1.7 V≤V <sub>DD</sub> ≤3.6 V		-	-	22.5	
		Slave mode, SPI1/2/3/4/5/6, 1.7 V≤V <sub>DD</sub> ≤3.6 V				22.5	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode		30	50	70	%

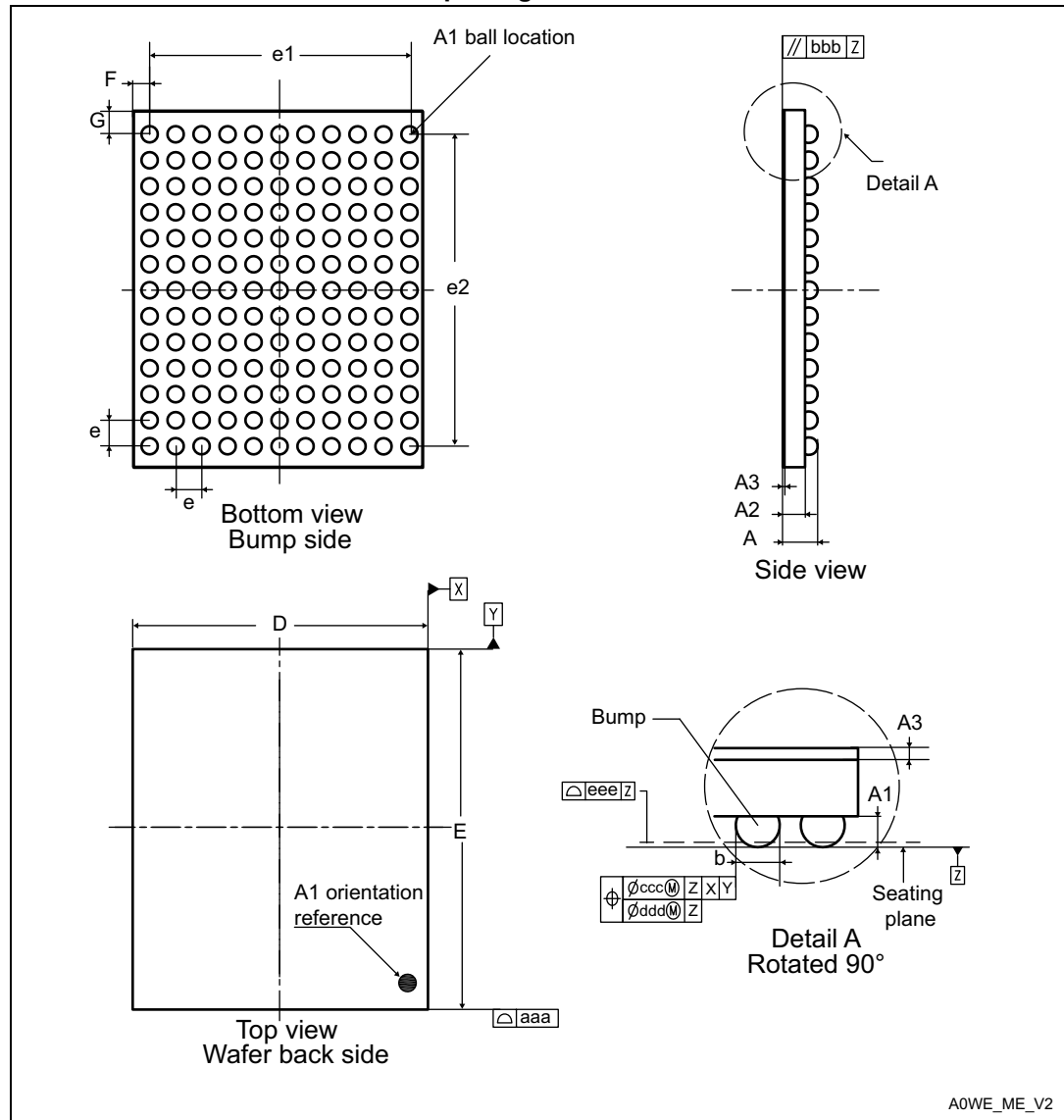


Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
$I_{DDA}^{(4)}$	DAC DC VDDA current consumption in quiescent mode <sup>(3)</sup>	-	-	280	380	$\mu A$	With no load, middle code (0x800) on the inputs
		-	-	475	625	$\mu A$	With no load, worst code (0xF1C) at $V_{REF+} = 3.6 V$ in terms of DC consumption on the inputs
DNL <sup>(4)</sup>	Differential non linearity Difference between two consecutive code-1LSB)	-	-	-	$\pm 0.5$	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	$\pm 2$	LSB	Given for the DAC in 12-bit configuration.
INL <sup>(4)</sup>	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	$\pm 1$	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	$\pm 4$	LSB	Given for the DAC in 12-bit configuration.
Offset <sup>(4)</sup>	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$ )	-	-	-	$\pm 10$	mV	Given for the DAC in 12-bit configuration
		-	-	-	$\pm 3$	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6 V$
		-	-	-	$\pm 12$	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6 V$
Gain error <sup>(4)</sup>	Gain error	-	-	-	$\pm 0.5$	%	Given for the DAC in 12-bit configuration
$t_{SETTLIN\_G}^{(4)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 4LSB$ )	-	-	3	6	$\mu s$	$C_{LOAD} \leq 50 pF$ , $R_{LOAD} \geq 5 k\Omega$
THD <sup>(4)</sup>	Total Harmonic Distortion Buffer ON	-	-	-	-	dB	$C_{LOAD} \leq 50 pF$ , $R_{LOAD} \geq 5 k\Omega$
Update rate <sup>(2)</sup>	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50 pF$ , $R_{LOAD} \geq 5 k\Omega$

## 7.2 WLCSP143 package information

Figure 83. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 115. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	--	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1732	1.1811	1.1890
D1	27.800	28.000	28.200	1.0945	1.1024	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1732	1.1811	1.1890
E1	27.800	28.000	28.200	1.0945	1.1024	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7.0°	0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$  functionality is no more available and VBAT pin should be connected to  $V_{DD}$ .
- The over-drive mode is not supported.

### A.1 Operating conditions

Table 123. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ( $f_{Flashmax}$ )	Maximum Flash memory access frequency with wait states <sup>(1)(2)</sup>	I/O operation	Possible Flash memory operations
$V_{DD} = 1.7$ to $2.1 V^{(3)}$	Conversion time up to 1.2 Msps	20 MHz <sup>(4)</sup>	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3.  $V_{DD}/V_{DDA}$  minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 3.17.1: Internal reset ON](#)).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

Table 124. Document revision history

Date	Revision	Changes
24-Apr-2014	4	<p>In the whole document, minimum supply voltage changed to 1.7 V when external power supply supervisor is used.</p> <p>Added DCMI_VSYNC alternate function on PG9 and updated note 6. in <a href="#">Table 10: STM32F427xx and STM32F429xx pin and ball definitions</a> and <a href="#">Table 12: STM32F427xx and STM32F429xx alternate function mapping</a>. Added note 2. below <a href="#">Figure 16: STM32F42x UFBGA169 ballout</a>.</p> <p>Changed SVGA (800x600) into XGA1024x768) on cover page and in <a href="#">Section 3.10: LCD-TFT controller (available only on STM32F429xx)</a>.</p> <p>Updated <a href="#">Section 3.18.2: Regulator OFF</a>.</p> <p>Updated signal corresponding to pin L5 in <a href="#">Figure 12: STM32F42x WLCSP143 ballout</a>.</p> <p>Added ACC<sub>HSE</sub> in <a href="#">Table 39: HSE 4-26 MHz oscillator characteristics</a> and ACC<sub>LSE</sub> in <a href="#">Table 40: LSE oscillator characteristics (fLSE = 32.768 kHz)</a>.</p> <p>Updated <a href="#">Table 53: ESD absolute maximum ratings</a>.</p> <p>Updated V<sub>IH</sub> in <a href="#">Table 56: I/O static characteristics</a>. Added condition V<sub>DD</sub>&gt;1.7 V in <a href="#">Table 58: I/O AC characteristics</a>.</p> <p>Updated conditions in <a href="#">Table 62: SPI dynamic characteristics</a>.</p> <p>Added Z<sub>DRV</sub> in <a href="#">Table 67: USB OTG full speed electrical characteristics</a>.</p> <p>Removed note 3 in <a href="#">Table 80: Temperature sensor characteristics</a>.</p> <p>Added <a href="#">Figure 82: LQFP100 marking example (package top view)</a>, <a href="#">Figure 85: WLCSP143 marking example (package top view)</a>, <a href="#">Figure 88: LQFP144 marking example (package top view)</a>, <a href="#">Figure 91: LQFP176 marking (package top view)</a>, <a href="#">Figure 94: LQFP208 marking example (package top view)</a>, <a href="#">Figure 97: UFBGA169 marking example (package top view)</a> and <a href="#">Figure 100: UFBGA176+25 marking example (package top view)</a>.</p> <p>Added <a href="#">Appendix A: Recommendations when using internal reset OFF</a>.</p> <p>Removed Internal reset OFF hardware connection appendix.</p>