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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427igh6tr

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In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V₁₂ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.





The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V₁₂ minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V₁₂ minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V₁₂ minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V₁₂ minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application (see Table 17: General operating conditions).



Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	90	180
	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
General	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	90	180
purpose	TIM10 TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	90	180
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	45	90/180
	TIM13 TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	45	90/180
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	45	90/180

Table 6. Timer feature comparison

1. The maximum timer clock is either 90 or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.





Figure 13. STM32F42x LQFP144 pinout

1. The above figure shows the package top view.



			Pin nu	imbe	r								
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
-	-	M1	L4	48	N11	-	L5	BYPASS_ REG	I	FT	-	-	-
28	39	J11	K4	49	J8	52	K5	V _{DD}	S	-	-	-	-
29	40	N2	N4	50	M10	53	N4	PA4	I/O	ТТа	(5)	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_ IN4 /DAC_ OUT1
30	41	М3	P4	51	M9	54	P4	PA5	I/O	ТТа	(5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, EVENTOUT	ADC12_ IN5/DAC_ OUT2
31	42	N3	P3	52	N10	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_ IN6
32	43	K4	R3	53	L8	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_ RMII_CRS_DV, EVENTOUT	ADC12_ IN7
33	44	L4	N5	54	M8	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_ RMII_RXD0, EVENTOUT	ADC12_ IN14
34	45	M4	P5	55	N9	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_ RMII_RXD1, EVENTOUT	ADC12_ IN15
-	-	-	-	-	J7	59	L7	V _{DD}	S	-	-		-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx	pin and ball definitions	(continued)
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			Pin nu	ımbeı	r								
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
68	101	E8	E15	120	E2	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
69	102	E9	D15	121	D5	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
70	103	E10	C15	122	D4	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, LCD_R4, OTG_FS_DM, EVENTOUT	-
71	104	E11	B15	123	E1	146	B15	PA12 I/O FT - CAN1_TX, LCD_R5, OTG_FS_DP, EVENTOUT		-			
72	105	E12	A15	124	D3	147	A15	PA13 (JTMS- SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	106	D12	F13	125	D1	148	E11	V _{CAP_2}	S		-	-	-
74	107	J10	F12	126	D2	149	F10	V _{SS}	S		-	-	-
75	108	H4	G13	127	C1	150	F11	V_{DD}	S		-	-	-
-	-	D13	E12	128	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	C13	E13	129	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	C12	D13	130	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	B13	E14	131	-	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS ⁽⁷⁾ , FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx	pin and ball definitio	ns (continued)
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Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

-																	
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
P	Port		TIM1/2	TIM3/4/5	TIM8/9/ 10/11	l2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ЕТН	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
	PC8	-	-	TIM3_ CH3	TIM8_ CH3	-	-	-	-	USART6_ CK	-	-	-	SDIO_D0	DCMI_ D2	-	EVEN TOUT
	PC9	MCO2	-	TIM3_ CH4	TIM8_ CH4	I2C3_ SDA	I2S_ CKIN	-	-	-	-	-	-	SDIO_D1	DCMI_ D3	-	EVEN TOUT
	PC10	-	-	-	-	-	-	SPI3_ SCK/I2S 3_CK	USART3_ TX	UART4_TX	-	-	-	SDIO_D2	DCMI_ D8	LCD_R2	EVEN TOUT
Port	PC11	-	-	-	-	-	I2S3ext _SD	SPI3_ MISO	USART3_ RX	UART4_RX	-	-	-	SDIO_D3	DCMI_ D4	-	EVEN TOUT
С	PC12	-	-	-	-	-	-	SPI3_ MOSI/I2 S3_SD	USART3_ CK	UART5_TX	-	-	-	SDIO_CK	DCMI_ D9	-	EVEN TOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVEN TOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FMC_D3	-	-	EVEN TOUT
	PD2	-	-	TIM3_ ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_ CMD	DCMI_ D11	-	EVEN TOUT
Port D	PD3	-	-	-	-	-	SPI2_S CK/I 2S2_CK	-	USART2_ CTS	-	-	-	-	FMC_CLK	DCMI_ D5	LCD_G7	EVEN TOUT
	PD4	-	-	-	-	-	-	-	USART2_ RTS	-	-	-	-	FMC_NOE	-	-	EVEN TOUT
	PD5	-	-	-	-	-	-	-	USART2_ TX	-	-	-	-	FMC_NWE	-	-	EVEN TOUT
	PD6	-	-	-	-	-	SPI3_ MOSI/I2 S3_SD	SAI1_ SD_A	USART2_ RX	-	-	-	-	FMC_ NWAIT	DCMI_ D10	LCD_B2	EVEN TOUT

Pinouts and pin description

STM32F427xx STM32F429xx

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		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
P	ort	SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ЕТН	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
	PI7	-	-	-	TIM8_ CH3	-	-	-	-	-	-	-	-	FMC_D29	DCMI_ D7	LCD_B7	EVEN TOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D30	-	LCD_ VSYNC	EVEN TOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ RX_ER	FMC_D31	-	LCD_ HSYNC	EVEN TOUT
Port I	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ ULPI_DIR	-	-	-	-	EVEN TOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ HSYNC	EVEN TOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ VSYNC	EVEN TOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ CLK	EVEN TOUT
	PI15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R0	EVEN TOUT
	PJ0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R1	EVEN TOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVEN TOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVEN TOUT
Dert	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVEN TOUT
Ροπ J	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVEN TOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVEN TOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVEN TOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVEN TOUT

 Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

AF0

SYS

.

Port

PJ8

AF1

TIM1/2

AF2

TIM3/4/5

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	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3
Dort I	PJ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G4
Port J	PJ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B0
	PJ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B1
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3
F	PK0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G5
	PK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G6
	PK2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G7
Deat	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4
Port K	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5
-	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

AF7

SPI3/

USART1/

2/3

AF8

USART6/

UART4/5/7

/8

AF9

CAN1/2/

TIM12/13/14

/LCD

AF11

ETH

AF10

OTG2_HS /OTG1_

FS

AF13

DCMI

AF12

FMC/SDIO

/OTG2 FS

AF14

LCD

LCD_G1

AF15

SYS

EVEN

TOUT EVEN TOUT

EVEN

TOUT EVEN TOUT

EVEN TOUT

EVEN

TOUT EVEN TOUT

EVEN TOUT

EVEN TOUT

EVEN TOUT

EVEN

TOUT EVEN TOUT

EVEN

TOUT EVEN TOUT

EVEN TOUT

EVEN TOUT

AF6

SPI2/3/

SAI1

AF4

I2C1/

2/3

AF5

SPI1/2/

3/4/5/6

AF3

TIM8/9/

10/11

1. The DCMI_VSYNC alternate function on PG9 is only available on silicon revision 3.

Symbol	Parameter	Conditions	l/O toggling frequency (fsw)	Тур	Unit	
			2 MHz	0.0		
			8 MHz	0.2		
		$V_{DD} = 3.3 V$	25 MHz	0.6		
			50 MHz	1.1		
		0- 0 _{N1}	60 MHz	1.3		
			84 MHz	1.8		
	I/O switching		90 MHz	1.9		
I _{DDIO}	Current		2 MHz	0.1	MA	
			8 MHz	0.4		
		V _{DD} = 3.3 V	25 MHz	1.23		
		$C_{EXT} = 0 \text{ pF}$ $C = C_{INT} + C_{EXT}$ $+ C_{S}$	50 MHz	2.43		
			60 MHz	2.93		
			84 MHz	3.86		
			90 MHz	4.07		
			2 MHz	0.18		
		$V_{DD} = 3.3 V$ $C_{EXT} = 10 \text{ pF}$ $C = C_{INT} + C_{EXT}$ $+ C_{S}$	8 MHz	0.67		
			25 MHz	2.09		
			50 MHz	3.6		
			60 MHz	4.5		
			84 MHz	7.8		
			90 MHz	9.8		
	I/O switching		2 MHz	0.26		
IDDIO	Current	V _{DD} = 3.3 V	8 MHz	1.01	mA	
		$C_{EXT} = 22 \text{ pF}$	25 MHz	3.14		
		$C = C_{INT} + C_{EXT}$ + C_{S}	50 MHz	6.39		
			60 MHz	10.68		
		$V_{\rm DD} = 3.3 V$	2 MHz	0.33		
		$C_{EXT} = 33 \text{ pF}$	8 MHz	1.29		
		$C = C_{INT} + Cext + C_S$	25 MHz	4.23		
			50 MHz	11.02		

Table 34. Switching output I/O current consumption⁽¹⁾

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).

2. This test is performed by cutting the LQFP176 package pin (pad removal).



Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC[?] code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Symbol	Parameter	Conditions	Monitored	Max vs. [f _{HSE} /f _{CPU}]	Max vs. [f _{HSE} /f _{CPU}]	Unit	
				25/168 MHz	25/180 MHz		
		$V_{DD} = 3.3 \text{ V}$ T ₄ = 25 °C OEP176	0.1 to 30 MHz	16	19	_ dBµV	
		$v_{DD} = 3.3 v$, $r_A = 23 v$, $c_A = 100 v$, $r_A = 100 v$, $r_$	30 to 130 MHz	23	23		
		EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.Peak level $V_{DD} = 3.3 \text{ V}, T_A = 25 \text{ °C}, LQFP176$ package, conforming to SAE J1752/3 EEMBC, ART ON, all peripheral clocks enabled, clock dithering enabled	130 MHz to 1GHz	25	22		
S	Peak level		SAE EMI Level	4	4	-	
SEWI			0.1 to 30 MHz	17	16	dBuV	
			30 to 130 MHz	8	10		
			130 MHz to 1GHz	11	16		
			SAE EMI level	3.5	3.5	-	

Table 52. EMI characteristics



6.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESD S5.3.1 standards.

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	2	2000	
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device	T_A = +25 °C conforming to ANSI/ESD S5.3.1, LQFP100/144/176, UFBGA169/176, TFBGA176 and WLCSP143 packages	C3	250	V
	model)	$T_A = +25$ °C conforming to ANSI/ESD S5.3.1, LQFP208 package	C3	250	

Table 53. ESD absolute maximum ratings

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105 \text{ °C conforming to JESD78A}$	II level A

Table 54. Electrical sensitivities



6.3.19 TIM timer characteristics

The parameters given in Table 60 are guaranteed by design.

Refer to Section 6.3.17: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
t _{res(TIM)}	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, f TIMxCLK = 180 MHz		-	t _{TIMxCLK}
		AHB/APBx prescaler>4, f _{TIMxCLK} = 90 MHz	1	-	t _{TIMxCLK}
f _{EXT}	Timer external clock frequency on CH1 to CH4	f _{TIMxCLK} = 180 MHz	0	f _{TIMxCLK} /2	MHz
Res _{TIM}	Timer resolution		-	16/32	bit
t _{MAX_COUNT}	Maximum possible count with 32-bit counter		-	65536 × 65536	t _{TIMxCLK}

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.

2. Guaranteed by design.

 The maximum timer frequency on APB1 or APB2 is up to 180 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK = 4x PCLKx.

6.3.20 Communications interfaces

I²C interface characteristics

The I^2C interface meets the timings requirements of the I^2C -bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0090 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Refer to Section 6.3.17: I/O port characteristics for more details on the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:



Symbol	Parameter	Min	Мах	Unit							
t _{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns							

Table 61. I2C analog filter characteristics⁽¹⁾

- 1. Guaranteed by design.
- 2. Spikes with widths below $t_{AF(min)}$ are filtered.
- 3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 62* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V_{DD}

Refer to Section 6.3.17: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Symbol	Parameter	Condition	s	Min	Тур	Max	Unit	
fsск 1/t. сост		Master mode, SPI1/4/5 2.7 V≤V _{DD} ≤3.6 V			45			
		Slave mode,	Receiver	-] - -	-	45	
	SPI clock frequency	SPI1/4/5/6, 2.7 V≤V _{DD} ≤3.6 V	Transmitter/ full-duplex			38 ⁽²⁾	MHz	
""C(SCK)		Master mode, SPI1/2/3 1.7 V≤V _{DD} ≤3.6 V			22.5			
		Slave mode, SPI1/2/3/- 1.7 V≤V _{DD} ≤3.6 V	-	-	22.5			
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode		30	50	70	%	

Table 62. SPI dynamic characteristics⁽¹⁾



6.3.23 V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Тур	Мах	Unit
R	Resistor bridge for V _{BAT}	-	50	-	KΩ
Q	Ratio on V _{BAT} measurement	-	4	-	
Er ⁽¹⁾	Error on Q	-1	-	+1	%
T _{S_vbat} ⁽²⁾⁽²⁾	ADC sampling time when reading the V _{BAT} 1 mV accuracy	5	-	-	μs

Table 82. V_{BAT} monitoring characteristics

1. Guaranteed by design.

2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Reference voltage

The parameters given in *Table 83* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{REFINT}	Internal reference voltage	–40 °C < T _A < +105 °C	1.18	1.21	1.24	V
T _{S_vrefint} ⁽¹⁾	ADC sampling time when reading the internal reference voltage		10	-	-	μs
V _{RERINT_s} ⁽²⁾	Internal reference voltage spread over the temperature range	V_{DD} = 3V \pm 10mV	-	3	5	mV
T _{Coeff} ⁽²⁾	Temperature coefficient		-	30	50	ppm/°C
t _{START} ⁽²⁾	Startup time		-	6	10	μs

Table 83. internal reference voltage

1. Shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design, not tested in production

Table 84. Internal reference voltage calibration values

Symbol	Parameter	Memory address		
V_{REFIN} CAL	Raw data acquired at temperature of 30 $^\circ C_{VDDA}$ = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B		



Symbol	Parameter	Min	Мах	Unit
t _{su(ADV-CLKH)}	FMC_A/D[15:0] valid data before FMC_CLK high	5	-	ns
t _{h(CLKH-ADV)}	FMC_A/D[15:0] valid data after FMC_CLK high	0	-	ns
t _{su(NWAIT-CLKH)}	FMC_NWAIT valid before FMC_CLK high	4	-	ns
t _{h(CLKH-NWAIT)}	FMC_NWAIT valid after FMC_CLK high	0	-	ns

Table 94. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

1. C_L = 30 pF.

2. Guaranteed by characterization results.



Figure 60. Synchronous multiplexed PSRAM write timings



Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾			
Symbol	Min	Тур	Мах	Min	Тур	Мах	
eee	-	-	0.150	-	-	0.0059	
fff	-	-	0.080	-	-	0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for TFBGA176

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.



Figure 102. TFBGA176 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

