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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-UFBGA
Supplier Device Package	176-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427iih7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

These features make the STM32F427xx and STM32F429xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.

Periphe	erals	STM32F427 Vx		STM32F429Vx		29Vx	STM32F427 Zx STM32F42		STM32F429Zx Ax		2F427 Ax	STM3	STM32F429 Ax		2F427 x	, STM32F429Ix		291x	STM32F429Bx		STM32F429Nx		29Nx			
Flash memory i	n Kbytes	1024	2048	512	1024	2048	1024	2048	512	1024	2048	1024	2048	1024	2048	1024	2048	512	1024	2048	512	1024	2048	512	1024	2048
SRAM in	System		256(112+16+64+64)																							
Kbytes	Backup													4												
FMC memory controller Yes ⁽¹⁾																										
Ethernet														Yes												
	General- purpose		10																							
Timers	Advanced -control													2												
	Basic													2												
Random numbe	Random number generator Yes																									

Table 2. STM32F427xx and STM32F429xx features and peripheral counts

DocID024030 Rev 9

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

Table 5. Voltage regulator modes in stop mode

• Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.



Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	90	180
	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
General	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	90	180
purpose	TIM10 TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	90	180
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	45	90/180
	TIM13 TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	45	90/180
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	45	90/180

Table 6. Timer feature comparison

1. The maximum timer clock is either 90 or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.



3.35 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.36 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.37 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 90 MHz.

3.38 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.



	11	10	9	8	7	6	5	4	3	2	1
A	PDR ON	(PE1)	(PB8)	(PB6)	PG15	PG12	(PD7)	PD5	PD2	PC10	VDD
В	PE4	PE0	(PB9)	(PB7)	(PB3)	(PG11)	(PD4)	(PD3)	(PD0)	PC11	(PA14)
С	VBAT	(PE3)		(PB5)	(PB4)	PG10	VDD	(PD1)	PC12	(PA15)	VDD
D	PC14	PC13	PE5	PE2	VDD	PG13	(PA10)	(PA11)	(PA13)	vss	VCAP _2
Е	PC15	VDD	(PF1)	PE6	vss	VDD	PG9	PC8	PC9	(PA9)	(PA12)
F	PF0	PF2	(PF4)	PF5	(PF7)	PG14	vss	PD6	PC7	PC6	(PA8)
G	PF3	PF6	(PF10)	PF9	VDD	PG5	PG4	PG6	PG3	PG8	VDD
Н	PF8	(PH1)	NRST	PC0	vss	(PD12)	(PD13)	PD10	vss	vss	PG7
J	PH0	PC2	PC3	VDD	VDD	VDD	VDD	PE10	(PB15)	(PD14)	PG2
К	PC1	VSSA	PA0	(PA1)	(PB1)	(PF13)	(PG1)	(PE11)	(PB14)	(PD11)	PD15
L	VREF +	VDDA	(PA2)	(PA7)	(PB2)	(PF14)	PE7	PE12	PE15	(PD8)	VDD
М	PA3	(PA4)	(PA5)	PC4	(PF11)	(PF15)	PE8	PE14	PB10	(PB12)	(PD9)
Ν	BYPASS_ REG	(PA6)	PC5	(PB0)	(PF12)	(PG0)	PE9	PE13	(PB11)		PB13

Figure 12. STM32F42x WLCSP143 ballout

1. The above figure shows the package bump view.





Figure 14. STM32F42x LQFP176 pinout

1. The above figure shows the package top view.





Figure 16. STM32F42x UFBGA169 ballout

1. The above figure shows the package top view.

2. The 4 corners balls, A1,A13, N1 and N13, are not bonded internally and should be left not connected on the PCB.



			Pin nı	Impe	r								
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
4	4	D1	B2	4	D9	4	B1	PE5	I/O FT - TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT		-		
5	5	D2	В3	5	E8	5	B2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	V _{SS}	S	-	-	-	-
-	-	-	-	-	-	-	F5	V _{DD}	S	-	-	-	-
6	6	E5	C1	6	C11	6	C1	V _{BAT}	S	-	-	-	-
-	-	NC (2)	D2	7	-	7	C2	PI8	I/O	FT	(3) (4)	EVENTOUT	TAMP_2
7	7	E4	D1	8	D10	8	D1	PC13	I/O	FT	(3) (4)	EVENTOUT	TAMP_1
8	8	E1	E1	9	D11	9	E1	PC14- OSC32_IN (PC14)	I/O	FT	(3) (4)	EVENTOUT	OSC32_IN (5)
9	9	F1	F1	10	E11	10	F1	PC15- OSC32_OUT (PC15)	I/O	FT	(3) (4)	EVENTOUT	OSC32_ OUT ⁽⁵⁾
-	-	-	-	-	-	-	G5	V _{DD}	S	-	-	-	-
-	-	E2	D3	11	-	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	E3	12	-	12	D5	PI10 I/O FT - ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT		-			
-	-	NC (2)	E4	13	-	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	F6	F2	14	E7	14	F2	V _{SS}	S	-	-	-	-
-	-	F4	F3	15	E10	15	F4	V _{DD}	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx	pin and ball definitions	(continued)
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51

Table 12. STM32F427xx and STM32F429xx alternate function mapping

		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Po	ort	SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ЕТН	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
	PA0	-	TIM2_ CH1/TIM2 _ETR	TIM5_ CH1	TIM8_ ETR	-	-	-	USART2_ CTS	UART4_TX	-	-	ETH_MII_ CRS	-	-	-	EVEN TOUT
	PA1	-	TIM2_ CH2	TIM5_ CH2	-	-	-	-	USART2_ RTS	UART4_RX	-	-	ETH_MII_ RX_CLK/E TH_RMII_ REF_CLK	-	-	-	EVEN TOUT
	PA2	-	TIM2_ CH3	TIM5_ CH3	TIM9_ CH1	-	-	-	USART2_ TX	-	-	-	ETH_ MDIO	-	-	-	EVEN TOUT
	PA3	-	TIM2_ CH4	TIM5_ CH4	TIM9_ CH2	-	-	-	USART2_ RX	-	-	OTG_HS_ ULPI_D0	ETH_MII_ COL	-	-	LCD_B5	EVEN TOUT
	PA4	-	-	-	-	-	SPI1_ NSS	SPI3_ NSS/ I2S3_WS	USART2_ CK	-	-	-	-	OTG_HS_ SOF	DCMI_ HSYNC	LCD_ VSYNC	EVEN TOUT
Dort A	PA5	-	TIM2_ CH1/TIM2 _ETR	-	TIM8_ CH1N	-	SPI1_ SCK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	-	EVEN TOUT
FULA	PA6	-	TIM1_ BKIN	TIM3_ CH1	TIM8_ BKIN	-	SPI1_ MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_ PIXCLK	LCD_G2	EVEN TOUT
	PA7	-	TIM1_ CH1N	TIM3_ CH2	TIM8_ CH1N	-	SPI1_ MOSI	-	-	-	TIM14_CH1	-	ETH_MII_ RX_DV/ ETH_RMII _CRS_DV	-	-	-	EVEN TOUT
	PA8	MCO1	TIM1_ CH1	-	-	I2C3_ SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	-	-	-	LCD_R6	EVEN TOUT
	PA9	-	TIM1_ CH2	-	-	I2C3_ SMBA	-	-	USART1_ TX	-	-	-	-	-	DCMI_ D0	-	EVEN TOUT
	PA10	-	TIM1_ CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_FS_ ID	-	-	DCMI_ D1	-	EVEN TOUT
	PA11	-	TIM1_ CH4	-	-	-	-	-	USART1_ CTS	-	CAN1_RX	OTG_FS_ DM	-	-	-	LCD_R4	EVEN TOUT
	PA12	-	TIM1_ ETR	-	-	-	-	-	USART1_ RTS	-	CAN1_TX	OTG_FS_ DP	-	-	-	LCD_R5	EVEN TOUT

STM32F427xx STM32F429xx

74/238

DocID024030 Rev 9

Pinouts and pin description

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 1000 - 0xBFFF FFFF	Reserved
	0xA000 0000- 0xA000 0FFF	FMC control register
ALIDS	0x9000 0000 - 0x9FFF FFFF	FMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
	0x5006 0800 - 0X5006 0BFF	RNG
	0x5005 0400 - X5006 07FF	Reserved
AHB2	0x5005 0000 - 0X5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0X5003 FFFF	USB OTG FS

 Table 13. STM32F427xx and STM32F429xx register boundary addresses





Figure 32. ACC_{LSI} versus temperature

6.3.11 PLL characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
f _{PLL_IN}	PLL input clock ⁽¹⁾		0.95 ⁽²⁾	1	2.10	MHz
f _{PLL_OUT}	PLL multiplier output clock		24	-	180	MHz
f _{PLL48_OUT}	48 MHz PLL multiplier output clock		-	48	75	MHz
f _{VCO_OUT}	PLL VCO output		100	-	432	MHz
t	PLL lock time	VCO freq = 100 MHz	75	-	200	116
LOCK		VCO freq = 432 MHz	100	-	300	μο

Table 43. Main PLL characteristics



Symbol	Parameter Conditions Min ⁽¹⁾		Value Min ⁽¹⁾	Unit
N _{END}	Endurance	$T_A = -40$ to +85 °C (6 suffix versions) $T_A = -40$ to +105 °C (7 suffix versions)	10	kcycles
		1 kcycle ⁽²⁾ at T _A = 85 °C	30	
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 105 °C	10	Years
		10 kcycles ⁽²⁾ at T _A = 55 °C	20	

 Table 50. Flash memory endurance and data retention

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Level/ Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V _{DD} = 3.3 V, LQFP176, T _A = +25 °C, f _{HCLK} = 168 MHz, conforms to IEC 61000-4-2	2B
V _{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3 \text{ V}, \text{LQFP176}, \text{T}_{\text{A}} = +25 \text{ °C}, \text{f}_{\text{HCLK}} = 168 \text{ MHz}, \text{ conforms to} \text{IEC 61000-4-2}$	4A

Table 51. EMS characteristics

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, PH2, PH3, PH4, PH5, PA3, PA4, PA5, PA6, PA7, PC4, and PC5.

As a consequence, it is recommended to add a serial resistor (1 k Ω) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 63* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V_{DD}

Refer to Section 6.3.17: I/O port characteristics for more details on the input/output alternate function characteristics (CK, SD, WS).

Symbol	Parameter	Conditions	Min	Max	Unit
f _{MCK}	I2S Main clock output	-	256x8K	256xFs ⁽²⁾	MHz
£	129 clock froguency	Master data: 32 bits	-	64xFs	
^I CK	125 Clock frequency	Slave data: 32 bits	-	64xFs	
D _{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
t _{v(WS)}	WS valid time	Master mode	0	6	
t _{h(WS)}	WS hold time	Master mode	0	-	
t _{su(WS)}	WS setup time	Slave mode	1	-	
t _{h(WS)}	WS hold time	Slave mode	0	-	
t _{su(SD_MR)}	Data input sotup timo	Master receiver	7.5	-	
t _{su(SD_SR)}		Slave receiver	2	-	
t _{h(SD_MR)}	Data input hold time	Master receiver	0	-	ns
t _{h(SD_SR)}	Data input noid time	Slave receiver	0	-	
t _{v(SD_ST)}		Slave transmitter (after enable edge)	-	27	
t _{h(SD_ST)}	Data output valid time				
t _{v(SD_MT)}		Master transmitter (after enable edge)	-	20	
t _{h(SD_MT)}	Data output hold time	Master transmitter (after enable edge)	2.5	-	

Table 63. I ²	² S dv	namic	characteris	stics ⁽¹⁾
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1. Guaranteed by characterization results.

2. The maximum value of 256xFs is 45 MHz (APB1 maximum frequency).

Note: Refer to t

Refer to the I2S section of RM0090 reference manual for more details on the sampling frequency (F_S).

 f_{MCK} , f_{CK} , and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.





Figure 41. I²S slave timing diagram (Philips protocol)⁽¹⁾

1. .LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



Figure 42. I²S master timing diagram (Philips protocol)⁽¹⁾

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Symbol	Parameter	Мах	Unit
t _{STARTUP} ⁽¹⁾	USB OTG full speed transceiver startup time	1	μs

Table 65. USB OTG full speed startup time

1. Guaranteed by design.

Symbol		Parameter	Conditions	Min. ⁽¹⁾	Тур.	Max. ⁽¹⁾	Unit
	V _{DD}	USB OTG full speed transceiver operating voltage		3.0 ⁽²⁾	-	3.6	V
Input	V _{DI} ⁽³⁾	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	
levels	V _{CM} ⁽³⁾	Differential common mode range	Includes V _{DI} range	0.8	-	2.5	V
	$V_{SE}^{(3)}$	Single ended receiver threshold		1.3	-	2.0	
Output levels	V _{OL}	Static output level low	$\rm R_L$ of 1.5 k\Omega to 3.6 $\rm V^{(4)}$	-	-	0.3	V
	V _{OH}	Static output level high	${\sf R}_{\sf L}$ of 15 k Ω to ${\sf V}_{\sf SS}{}^{(4)}$	2.8	-	3.6	v
R _{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	\/ - \/	17	21	24	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	VIN - VDD	0.65	1.1	2.0	kΩ
R _{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	V _{IN} = V _{SS} 1.5 1.8		2.1		
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V _{IN} = V _{SS}	0.25	0.37	0.55	

Table 66. USB OTG full speed DC electrical characteristics

1. All the voltages are measured from the local ground potential.

2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.

3. Guaranteed by design.

4. R_L is the load connected on the USB OTG full speed drivers.



Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.



Figure 51. Typical connection diagram using the ADC

1. Refer to Table 74 for the values of $\mathsf{R}_{\mathsf{AIN}},\,\mathsf{R}_{\mathsf{ADC}}\,\mathsf{and}\,\mathsf{C}_{\mathsf{ADC}}.$

 $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced. 2.



Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FMC_NE low time	3T _{HCLK} – 1	3T _{HCLK} +0.5	ns
t _{v(NOE_NE)}	FMC_NEx low to FMC_NOE low	2T _{HCLK} -0.5	2T _{HCLK}	ns
t _{tw(NOE)}	FMC_NOE low time	T _{HCLK} – 1	T _{HCLK} +1	ns
t _{h(NE_NOE)}	FMC_NOE high to FMC_NE high hold time	1	-	ns
t _{v(A_NE)}	FMC_NEx low to FMC_A valid	-	2	ns
t _{v(NADV_NE)}	FMC_NEx low to FMC_NADV low	0	2	ns
t _{w(NADV)}	FMC_NADV low time	T _{HCLK} – 0.5	T _{HCLK} +0.5	ns
t _{h(AD_NADV)}	FMC_AD(address) valid hold time after FMC_NADV high)	0	-	ns
t _{h(A_NOE)}	Address hold time after FMC_NOE high	T _{HCLK} – 0.5	-	ns
t _{h(BL_NOE)}	FMC_BL time after FMC_NOE high	0	-	ns
t _{v(BL_NE)}	FMC_NEx low to FMC_BL valid	-	2	ns
t _{su(Data_NE)}	Data to FMC_NEx high setup time	T _{HCLK} +1.5	-	ns
t _{su(Data_NOE)}	Data to FMC_NOE high setup time	T _{HCLK} +1	-	ns
t _{h(Data_NE)}	Data hold time after FMC_NEx high	0	-	ns
t _{h(Data_NOE)}	Data hold time after FMC_NOE high	0	-	ns

Table 90. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

1. C_L = 30 pF.

2. Guaranteed by characterization results.

Table 91. Asyn	chronous multi	plexed PSRAM/NOR	read-NWAIT	timings ⁽¹⁾⁽²⁾

Symbol Parameter		Min	Max	Unit
t _{w(NE)}	FMC_NE low time	8T _{HCLK} +0.5	8T _{HCLK} +2	ns
t _{w(NOE)}	FMC_NWE low time	5T _{HCLK} – 1	5T _{HCLK} +1.5	ns
t _{su(NWAIT_NE)}	FMC_NWAIT valid before FMC_NEx high	5T _{HCLK} +1.5	-	ns
t _{h(NE_NWAIT)}	FMC_NEx hold time after FMC_NWAIT invalid	4T _{HCLK} +1		ns

1. C_L = 30 pF.

2. Guaranteed by characterization results.



Symbol	Parameter	Min	Мах	Unit
t _{su(ADV-CLKH)}	FMC_A/D[15:0] valid data before FMC_CLK high	5	-	ns
t _{h(CLKH-ADV)}	FMC_A/D[15:0] valid data after FMC_CLK high	0	-	ns
t _{su(NWAIT-CLKH)}	FMC_NWAIT valid before FMC_CLK high	4	-	ns
t _{h(CLKH-NWAIT)}	FMC_NWAIT valid after FMC_CLK high	0	-	ns

Table 94. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

1. C_L = 30 pF.

2. Guaranteed by characterization results.



Figure 60. Synchronous multiplexed PSRAM write timings





Figure 65. PC Card/CompactFlash controller waveforms for attribute memory read access

1. Only data bits 0...7 are read (bits 8...15 are disregarded).



STM32F427xx STM32F429xx

Date	Revision	Changes
Date	Revision	Changes Update SPI/IS2 in Table 2: STM32F427xx and STM32F429xx features and peripheral counts. Updated LQFP208 in Table 4: Regulator ON/OFF and internal reset ON/OFF availability. Updated Figure 19: Memory map. Changed PLS[2:0]=101 (falling edge) maximum value in Table 22: reset and power control block characteristics. Updated current consumption with all peripherals disabled in Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM. Updated note 1. in Table 28: Typical and maximum current consumptions in Standby mode. Updated twustop in Table 36: Low-power mode wakeup timings. Updated Table 56: I/O static characteristics. Section : 12C interface characteristics; updated section introduction, removed Table 12C characteristics; Updated section introduction, removed Table 12C characteristics. Updated measurement conditions in Table 62: SPI dynamic characteristics. Updated Figure 51: Typical connection diagram using the ADC. Updated Section : Device marking for LQFP100. Updated Section : Device marking for LQFP100. Updated Section : Device marking for LQFP101. Updated Section : Device marking for LQFP101. Updated Figure 83: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline and Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data; added Figure 84: WLCSP143 - 143
		 (package top view) and related note. Updated Section : Device marking for WLCSP143. Updated Section : Device marking for LQFP144. Updated Section : Device marking for LQFP176. Updated Figure 92: LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline; Updated Section : Device marking for LQFP208. Modified UFBGA169 pitch, updated Figure 95: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline and Table 116: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data; updated Section :
		Device marking for LQFP208. updated Section : Device marking for UFBGA169, Section : Device marking for UFBGA176+25 and Section : Device marking for TFBGA176.
		Updated \angle pin count in Table 122: Ordering information scheme.

Table 124. Document revision history

