## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427vgt6 |

Table 1. Device summary

| Reference | Part number |
|---|---|
| STM32F427xx | STM32F427VG, STM32F427ZG, STM32F427IG, STM32F427AG, STM32F427VI, STM32F427ZI, STM32F427II, STM32F427AI |
| STM32F429xx | STM32F429VG, STM32F429ZG, STM32F429IG, STM32F429BG, STM32F429NG, STM32F429AG, STM32F429VI, STM32F429ZI, STM32F429II,, STM32F429BI, STM32F429NI,STM32F429AI, STM32F429VE, STM32F429ZE, STM32F429IE, STM32F429BE, STM32F429NE |

### 3.22.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.22.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.22.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.23 Inter-integrated circuit interface ( $I^2C$)

Up to three $I^2C$ bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 KHz), and fast (up to 400 KHz) modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 7*).

**Table 7. Comparison of I2C analog and digital filters**

| | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |

## 3.24 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to

## Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI3/USART1/2/3 | USART6/UART4/5/7/8 | CAN1/2/TIM12/13/14/LCD | OTG2_HS/OTG1_FS | ETH | FMC/SDIO/OTG2_FS | DCMI | LCD | SYS |
| Port C | PC8 | - | - | TIM3_CH3 | TIM8_CH3 | - | - | - | - | USART6_CK | - | - | - | SDIO_D0 | DCMI_D2 | - | EVENTOUT |
| | PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | - | - | - | - | - | SDIO_D1 | DCMI_D3 | - | EVENTOUT |
| | PC10 | - | - | - | - | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | - | - | - | SDIO_D2 | DCMI_D8 | LCD_R2 | EVENTOUT |
| | PC11 | - | - | - | - | - | I2S3ext_SD | SPI3_MISO | USART3_RX | UART4_RX | - | - | - | SDIO_D3 | DCMI_D4 | - | EVENTOUT |
| | PC12 | - | - | - | - | - | - | SPI3_MOSI/I2S3_SD | USART3_CK | UART5_TX | - | - | - | SDIO_CK | DCMI_D9 | - | EVENTOUT |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| Port D | PD0 | - | - | - | - | - | - | - | - | - | CAN1_RX | - | - | FMC_D2 | - | - | EVENTOUT |
| | PD1 | - | - | - | - | - | - | - | - | - | CAN1_TX | - | - | FMC_D3 | - | - | EVENTOUT |
| | PD2 | - | - | TIM3_ETR | - | - | - | - | - | UART5_RX | - | - | - | SDIO_CMD | DCMI_D11 | - | EVENTOUT |
| | PD3 | - | - | - | - | - | SPI2_SCK/I2S2_CK | - | USART2_CTS | - | - | - | - | FMC_CLK | DCMI_D5 | LCD_G7 | EVENTOUT |
| | PD4 | - | - | - | - | - | - | - | USART2_RTS | - | - | - | - | FMC_NOE | - | - | EVENTOUT |
| | PD5 | - | - | - | - | - | - | - | USART2_TX | - | - | - | - | FMC_NWE | - | - | EVENTOUT |
| | PD6 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | SAI1_SD_A | USART2_RX | - | - | - | - | FMC_NWAIT | DCMI_D10 | LCD_B2 | EVENTOUT |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 17. General operating conditions

| Symbol | Parameter | Conditions(1) | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF | | 0 | - | 120 | MHz |
| | | Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON | Over-drive OFF | 0 | - | 144 | |
| | | | Over-drive ON | | - | 168 | |
| | | Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON | Over-drive OFF | 0 | - | 168 | |
| | | | Over-drive ON | | - | 180 | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | Over-drive OFF | | 0 | - | 42 | |
| | | Over-drive ON | | 0 | - | 45 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | Over-drive OFF | | 0 | - | 84 | |
| | | Over-drive ON | | 0 | - | 90 | |
| $V_{DD}$ | Standard operating voltage | | | 1.7(2) | - | 3.6 | V |
| $V_{DDA}$ (3)(4) | Analog operating voltage (ADC limited to 1.2 M samples) | Must be the same potential as $V_{DD}$(5) | | 1.7(2) | - | 2.4 | |
| | Analog operating voltage (ADC limited to 2.4 M samples) | | | 2.4 | - | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | | 1.65 | - | 3.6 | |
| $V_{12}$ | Regulator ON: 1.2 V internal voltage on $V_{CAP\_1}$/$V_{CAP\_2}$ pins | Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 120 MHz HCLK max frequency | | 1.08 | 1.14 | 1.20 | V |
| | | Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 144 MHz HCLK max frequency with over-drive OFF or 168 MHz with over-drive ON | | 1.20 | 1.26 | 1.32 | |
| | | Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON | | 1.26 | 1.32 | 1.40 | |
| | Regulator OFF: 1.2 V external voltage must be supplied from external regulator on $V_{CAP\_1}$/$V_{CAP\_2}$ pins(6) | Max frequency 120 MHz | | 1.10 | 1.14 | 1.20 | |
| | | Max frequency 144 MHz | | 1.20 | 1.26 | 1.32 | |
| | | Max frequency 168 MHz | | 1.26 | 1.32 | 1.38 | |

Figure 25. Typical $V_{BAT}$ current consumption (LSE and RTC ON/backup RAM OFF)

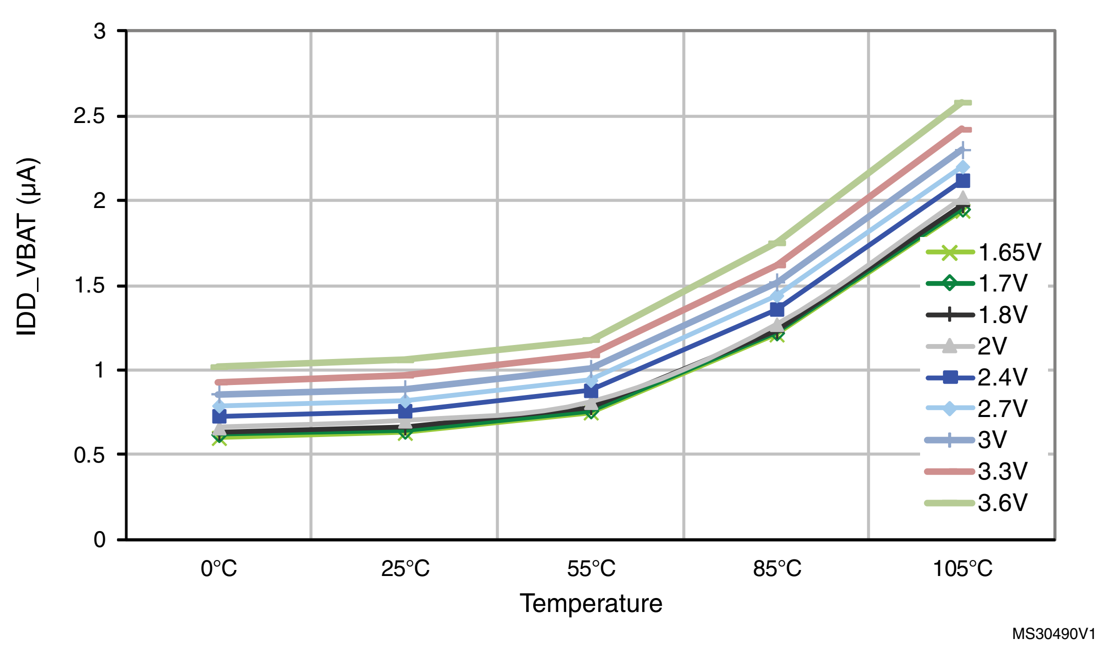
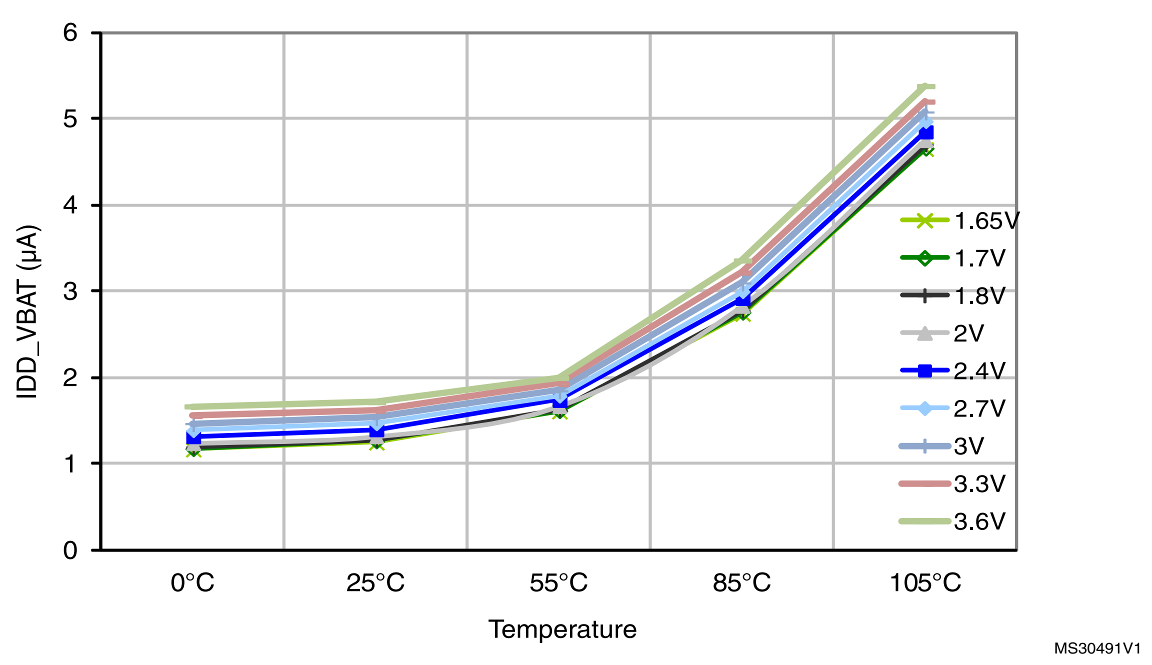


Figure 26. Typical $V_{BAT}$ current consumption (LSE and RTC ON/backup RAM ON)



### On-chip peripheral current consumption

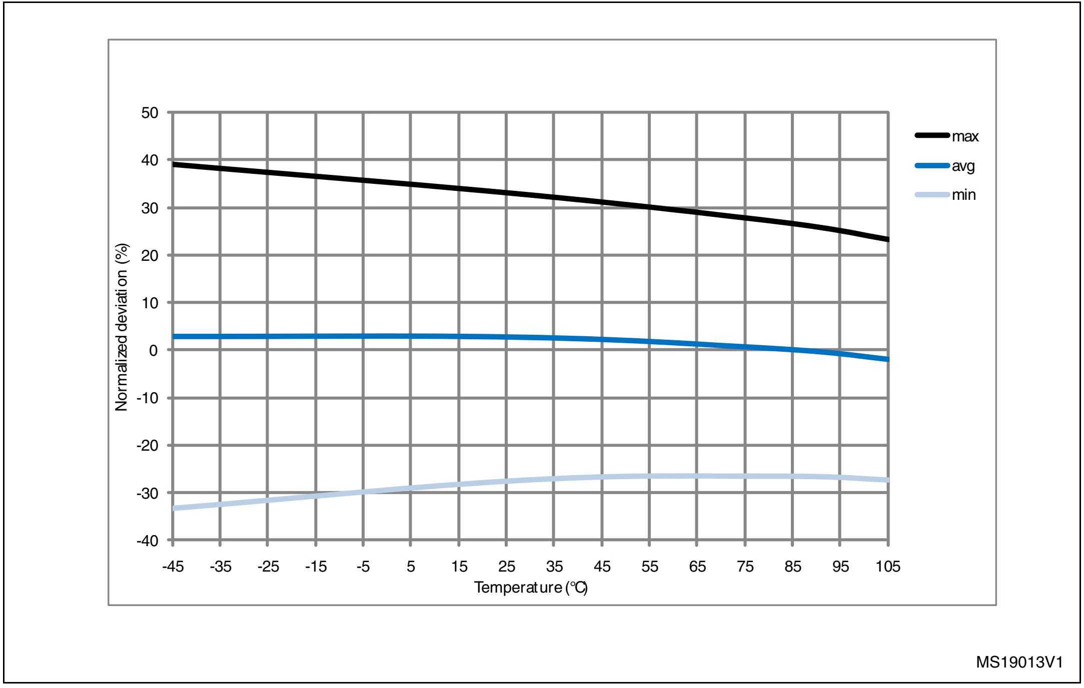
The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART accelerator is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{HCLK}$ = 180 MHz (Scale1 + over-drive ON), $f_{HCLK}$ = 144 MHz (Scale 2), $f_{HCLK}$ = 120 MHz (Scale 3)"
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 35. Peripheral current consumption**

| Peripheral | | $I_{DD}$( Typ)[1] | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| AHB1 (up to 180 MHz) | GPIOA | 2.50 | 2.36 | 2.08 | µA/MHz |
| | GPIOB | 2.56 | 2.36 | 2.08 | |
| | GPIOC | 2.44 | 2.29 | 2.00 | |
| | GPIOD | 2.50 | 2.36 | 2.08 | |
| | GPIOE | 2.44 | 2.29 | 2.00 | |
| | GPIOF | 2.44 | 2.29 | 2.00 | |
| | GPIOG | 2.39 | 2.22 | 2.00 | |
| | GPIOH | 2.33 | 2.15 | 1.92 | |
| | GPIOI | 2.39 | 2.22 | 2.00 | |
| | GPIOJ | 2.33 | 2.15 | 1.92 | |
| | GPIOK | 2.33 | 2.15 | 1.92 | |
| | OTG_HS+ULPI | 27.00 | 24.86 | 21.92 | |
| | CRC | 0.44 | 0.42 | 0.33 | |
| | BKPSRAM | 0.78 | 0.69 | 0.58 | |
| | DMA1 | 25.33 | 23.26 | 20.50 | |
| | DMA2 | 24.72 | 22.71 | 20.00 | |
| | DMA2D | 28.50 | 26.32 | 23.33 | |
| | ETH_MAC<br>ETH_MAC_TX<br>ETH_MAC_RX<br>ETH_MAC_PTP | 21.56 | 20.07 | 17.75 | |

Figure 32. $ACC_{LSI}$ versus temperature



## 6.3.11 PLL characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

Table 43. Main PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock(1) | | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | | 24 | - | 180 | MHz |
| $f_{PLL48\_OUT}$ | 48 MHz PLL multiplier output clock | | - | 48 | 75 | MHz |
| $f_{VCO\_OUT}$ | PLL VCO output | | 100 | - | 432 | MHz |
| $t_{LOCK}$ | PLL lock time | VCO freq = 100 MHz | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | 100 | - | 300 | |

## 6.3.17 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 56: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

**Table 56. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | FT, TTa and NRST I/O input low level voltage | 1.7 V≤$V_{DD}$≤3.6 V | - | - | $0.35V_{DD} - 0.04^{(1)}$<br>$0.3V_{DD}^{(2)}$ | V |
| | BOOT0 I/O input low level voltage | 1.75 V≤$V_{DD}$≤3.6 V, –40 °C≤$T_A$≤105 °C | - | - | $0.1V_{DD}+0.1^{(1)}$ | |
| | | 1.7 V≤$V_{DD}$≤3.6 V, 0 °C≤$T_A$≤105 °C | - | - | | |
| $V_{IH}$ | FT, TTa and NRST I/O input high level voltage$^{(5)}$ | 1.7 V≤$V_{DD}$≤3.6 V | $0.45V_{DD}+0.3^{(1)}$<br>$0.7V_{DD}^{(2)}$ | - | - | V |
| | BOOT0 I/O input high level voltage | 1.75 V≤$V_{DD}$≤3.6 V, –40 °C≤$T_A$≤105 °C | $0.17V_{DD}+0.7^{(1)}$ | - | - | |
| | | 1.7 V≤$V_{DD}$≤3.6 V, 0 °C≤$T_A$≤105 °C | | | | |
| $V_{HYS}$ | FT, TTa and NRST I/O input hysteresis | 1.7 V≤$V_{DD}$≤3.6 V | $10\%V_{DD}^{(3)}$ | - | - | V |
| | BOOT0 I/O input hysteresis | 1.75 V≤$V_{DD}$≤3.6 V, –40 °C≤$T_A$≤105 °C | 0.1 | - | - | |
| | | 1.7 V≤$V_{DD}$≤3.6 V, 0 °C≤$T_A$≤105 °C | | | | |
| $I_{lkg}$ | I/O input leakage current $^{(4)}$ | $V_{SS}$≤$V_{IN}$≤$V_{DD}$ | - | - | ±1 | µA |
| | I/O FT input leakage current $^{(5)}$ | $V_{IN}$ = 5 V | - | - | 3 | |

### SAI characteristics

Unless otherwise specified, the parameters given in *Table 64* for SAI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

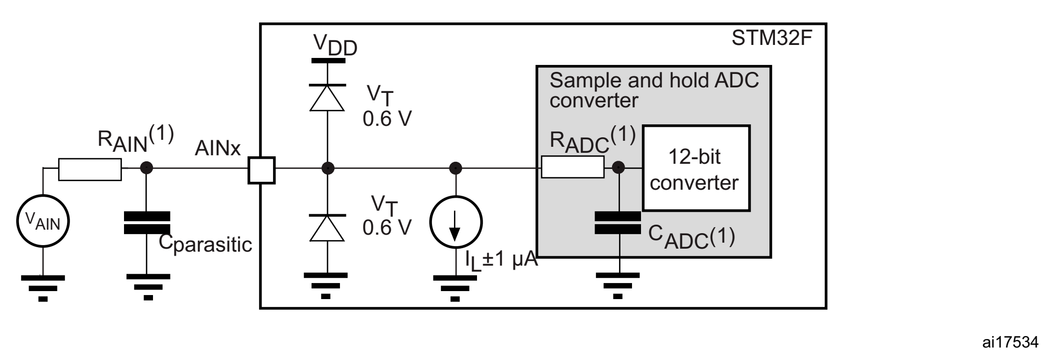
Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

**Table 64. SAI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCKL}$ | SAI Main clock output | - | 256 x 8K | 256xFs(2) | MHz |
| $F_{SCK}$ | SAI clock frequency | Master data: 32 bits | - | 64xFs | MHz |
| | | Slave  data: 32 bits | - | 64xFs | |
| $D_{SCK}$ | SAI clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(FS)}$ | FS valid time | Master mode | 8 | 22 | ns |
| $t_{su(FS)}$ | FS setup time | Slave mode | 2 | - | |
| $t_{h(FS)}$ | FS hold time | Master mode | 8 | - | |
| | | Slave mode | 0 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 5 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 3 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 0 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 0 | - | |
| $t_{v(SD\_ST)}$<br>$t_{h(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 22 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 20 | |
| $t_{h(SD\_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 8 | - | |

1. Guaranteed by characterization results.
2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)

Figure 51. Typical connection diagram using the ADC



1. Refer to *Table 74* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## 6.3.25 DAC electrical characteristics

**Table 85. DAC characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.7(1) | - | 3.6 | V | - |
| $V_{REF+}$ | Reference supply voltage | - | | 1.7(1) | - | 3.6 | V | $V_{REF+} \leq V_{DDA}$ |
| $V_{SSA}$ | Ground | - | | 0 | - | 0 | V | - |
| $R_{LOAD}$(2) | Resistive load | DAC output buffer ON | $R_{LOAD}$ connected to $V_{SSA}$ | 5 | - | - | kΩ | - |
| | | | $R_{LOAD}$ connected to $V_{DDA}$ | 25 | | | | - |
| $R_O$(2) | Impedance output with buffer OFF | - | | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$(2) | Capacitive load | - | | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer ON | - | | 0.2 | - | - | V | It gives the maximum output excursion of the DAC.<br>It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+}$ = 3.6 V and (0x1C7) to (0xE38) at $V_{REF+}$ = 1.7 V |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer ON | - | | - | - | $V_{DDA} - 0.2$ | V | |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer OFF | - | | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer OFF | - | | - | - | $V_{REF+}$ – 1LSB | V | |
| $I_{VREF+}$(4) | DAC DC $V_{REF}$ current consumption in quiescent mode (Standby mode) | - | | - | 170 | 240 | µA | With no load, worst code (0x800) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| | | - | | - | 50 | 75 | | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |

**Figure 59. Synchronous multiplexed NOR/PSRAM read timings**

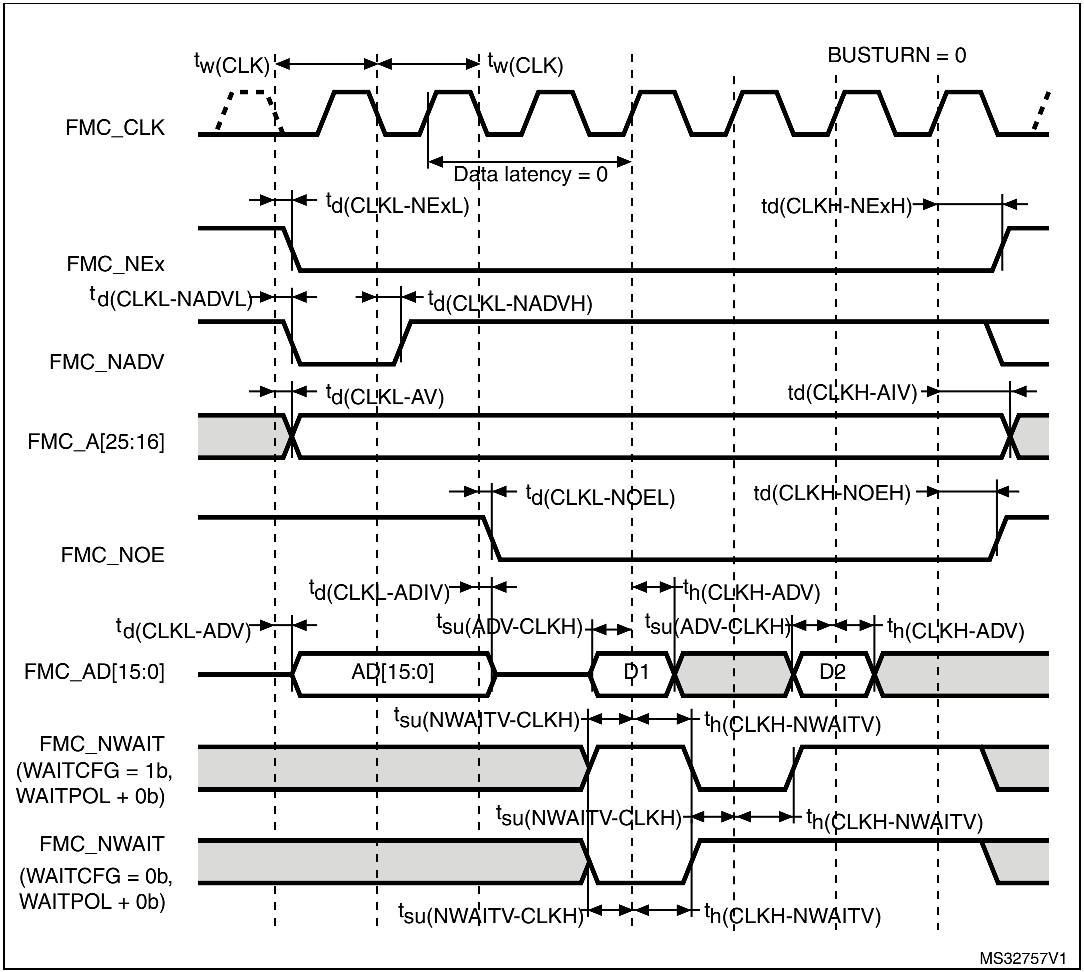


**Table 94. Synchronous multiplexed NOR/PSRAM read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | $2T_{HCLK} - 1$ | - | ns |
| $t_{d(CLKL\text{-}NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 0 | ns |
| $t_{d(CLKH\_NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}$ | - | ns |
| $t_{d(CLKL\text{-}NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0 | ns |
| $t_{d(CLKL\text{-}NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | ns |
| $t_{d(CLKL\text{-}AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 0 | ns |
| $t_{d(CLKH\text{-}AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | 0 | - | ns |
| $t_{d(CLKL\text{-}NOEL)}$ | FMC_CLK low to FMC_NOE low | - | $T_{HCLK}+0.5$ | ns |
| $t_{d(CLKH\text{-}NOEH)}$ | FMC_CLK high to FMC_NOE high | $T_{HCLK}-0.5$ | - | ns |
| $t_{d(CLKL\text{-}ADV)}$ | FMC_CLK low to FMC_AD[15:0] valid | - | 0.5 | ns |
| $t_{d(CLKL\text{-}ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | ns |

### Table 104. SDRAM write timings(1)(2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK} - 0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{d(SDCLKL\ \_Data)}$ | Data output valid time | - | 3.5 | |
| $t_{h(SDCLKL\ \_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 1.5 | |
| $t_{d(SDCLKL\_SDNWE)}$ | SDNWE valid time | - | 1 | |
| $t_{h(SDCLKL\_SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL\_\ SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL-\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | - | 2 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |
| $t_{d(SDCLKL\_NBL)}$ | NBL valid time | - | 0.5 | |
| $t_{h(SDCLKL\_NBL)}$ | NBLoutput time | 0 | - | |

1. CL = 30 pF on data and address lines. CL=15pF on FMC_SDCLK.
2. Guaranteed by characterization results.

### Table 105. LPSDR SDRAM write timings(1)(2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK} - 0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{d(SDCLKL\ \_Data)}$ | Data output valid time | - | 5 | |
| $t_{h(SDCLKL\ \_Data)}$ | Data output hold time | 2 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 2.8 | |
| $t_{d(SDCLKL-SDNWE)}$ | SDNWE valid time | - | 2 | |
| $t_{h(SDCLKL-SDNWE)}$ | SDNWE hold time | 1 | - | |
| $t_{d(SDCLKL-\ SDNE)}$ | Chip select valid time | - | 1.5 | |
| $t_{h(SDCLKL-\ SDNE)}$ | Chip select hold time | 1 | - | |
| $t_{d(SDCLKL-SDNRAS)}$ | SDNRAS valid time | - | 1.5 | |
| $t_{h(SDCLKL-SDNRAS)}$ | SDNRAS hold time | 1.5 | - | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS hold time | 1.5 | - | |
| $t_{d(SDCLKL\_NBL)}$ | NBL valid time | - | 1.5 | |
| $t_{h(SDCLKL-NBL)}$ | NBL output time | 1.5 | - | |

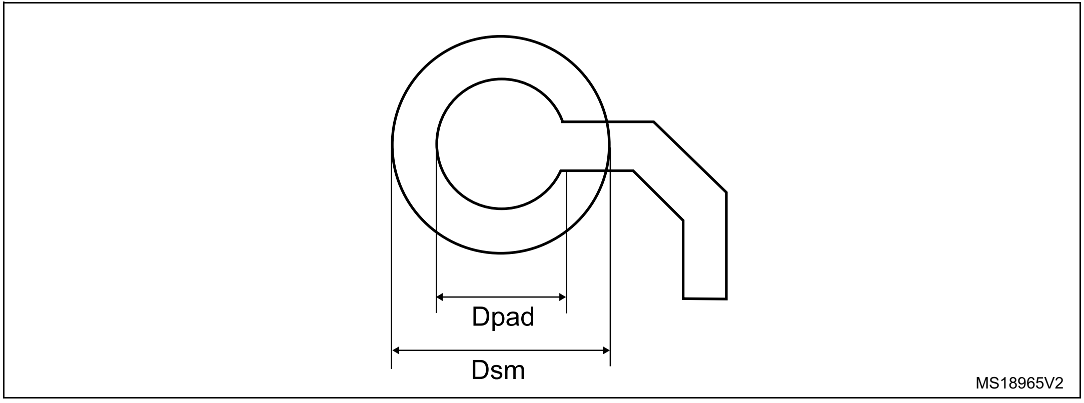
1. CL = 10 pF.
2. Guaranteed by characterization results.

### Table 111. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | 0.155 | 0.175 | 0.195 | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 4.486 | 4.521 | 4.556 | 0.1766 | 0.1780 | 0.1794 |
| E | 5.512 | 5.547 | 5.582 | 0.2170 | 0.2184 | 0.2198 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 4.000 | - | - | 0.1575 | - |
| e2 | - | 4.800 | - | - | 0.1890 | - |
| F | - | 0.2605 | - | - | 0.0103 | - |
| G | - | 0.3735 | - | - | 0.0147 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

### Figure 84. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint



### Table 113. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.874 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.689 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

### Table 115. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | -- | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 29.800 | 30.000 | 30.200 | 1.1732 | 1.1811 | 1.1890 |
| D1 | 27.800 | 28.000 | 28.200 | 1.0945 | 1.1024 | 1.1102 |
| D3 | - | 25.500 | - | - | 1.0039 | - |
| E | 29.800 | 30.000 | 30.200 | 1.1732 | 1.1811 | 1.1890 |
| E1 | 27.800 | 28.000 | 28.200 | 1.0945 | 1.1024 | 1.1102 |
| E3 | - | 25.500 | - | - | 1.0039 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7.0° | 0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

# 8 Part numbering

Table 122. Ordering information scheme

Example: STM32 F 429 V I T 6 xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

427= STM32F427xx, USB OTG FS/HS, camera interface, Ethernet

429= STM32F429xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT

**Pin count**

V = 100 pins
Z = 143 and 144 pins
A = 169 pins
I = 176 pins
B = 208 pins
N = 216 pins

**Flash memory size**

E = 512 Kbytes of Flash memory
G = 1024 Kbytes of Flash memory
I = 2048 Kbytes of Flash memory

**Package**

T = LQFP
H = BGA
Y = WLCSP

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

**Options**

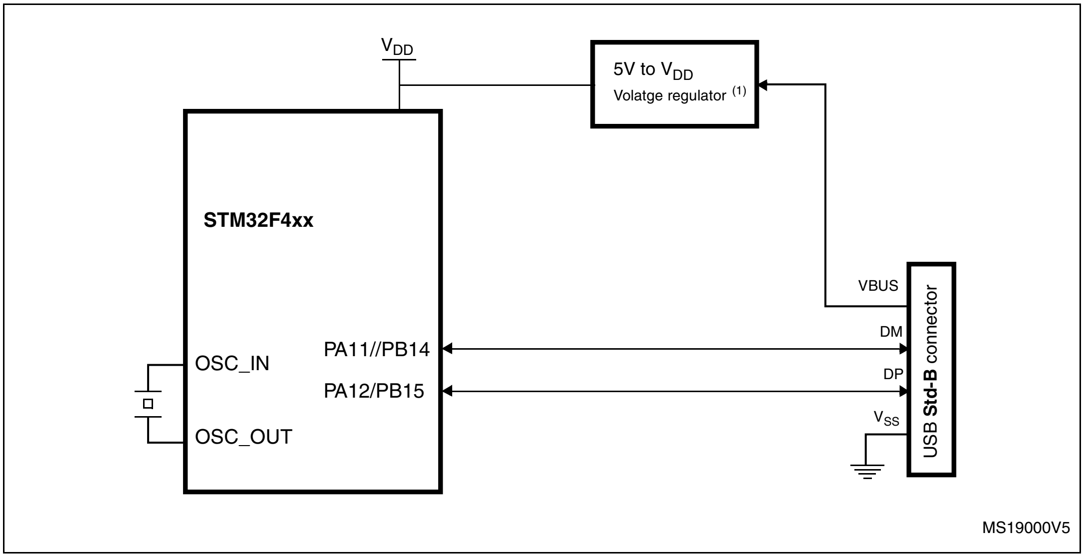
xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# Appendix B Application block diagrams

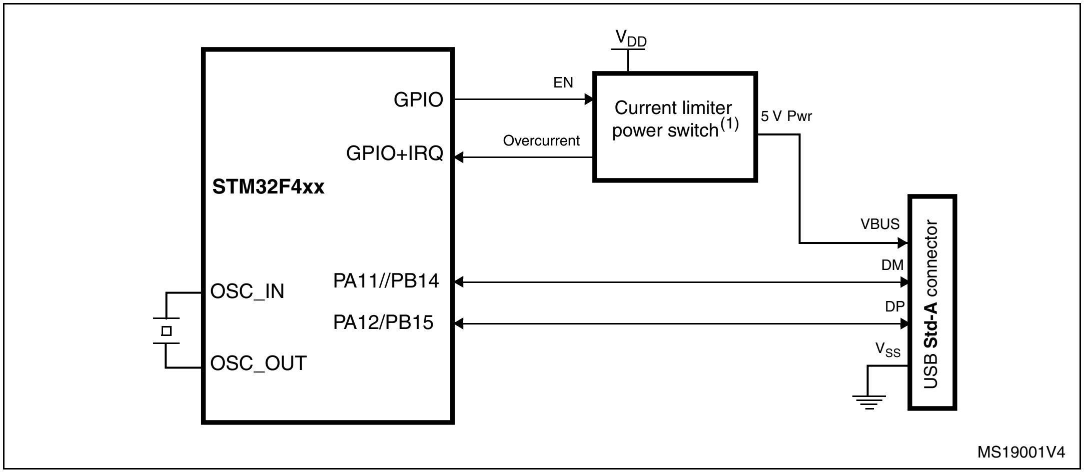
## B.1 USB OTG full speed (FS) interface solutions

Figure 103. USB controller configured as peripheral-only and used in Full speed mode



1. External voltage regulator only needed when building a $V_{BUS}$ powered device.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Figure 104. USB controller configured as host-only and used in full speed mode



1. The current limiter is required only if the application has to support a $V_{BUS}$ powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.