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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427vit6 |

# 1 Introduction

This datasheet provides the description of the STM32F427xx and STM32F429xx line of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F427xx and STM32F429xx datasheet should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214), available from *www.st.com*.

## 3.21 $V_{BAT}$ operation

The $V_{BAT}$ pin allows to power the device $V_{BAT}$ domain from an external battery, an external supercapacitor, or from $V_{DD}$ when no external battery and an external supercapacitor are present.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The $V_{BAT}$ pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation.*

*When PDR_ON pin is not connected to $V_{DD}$ (Internal Reset OFF), the $V_{BAT}$ functionality is no more available and $V_{BAT}$ pin should be connected to $V_{DD}$.*

## 3.22 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

*Table 6* compares the features of the advanced-control, general-purpose and basic timers.

communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

**Table 8. USART feature comparison[(1)]**

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X | X | X | X | X | 5.62 | 11.25 | APB2 (max. 90 MHz) |
| USART2 | X | X | X | X | X | X | 2.81 | 5.62 | APB1 (max. 45 MHz) |
| USART3 | X | X | X | X | X | X | 2.81 | 5.62 | APB1 (max. 45 MHz) |
| UART4 | X | - | X | - | X | - | 2.81 | 5.62 | APB1 (max. 45 MHz) |
| UART5 | X | - | X | - | X | - | 2.81 | 5.62 | APB1 (max. 45 MHz) |
| USART6 | X | X | X | X | X | X | 5.62 | 11.25 | APB2 (max. 90 MHz) |
| UART7 | X | - | X | - | X | - | 2.81 | 5.62 | APB1 (max. 45 MHz) |
| UART8 | X | - | X | - | X | - | 2.81 | 5.62 | APB1 (max. 45 MHz) |

1. X = feature supported.

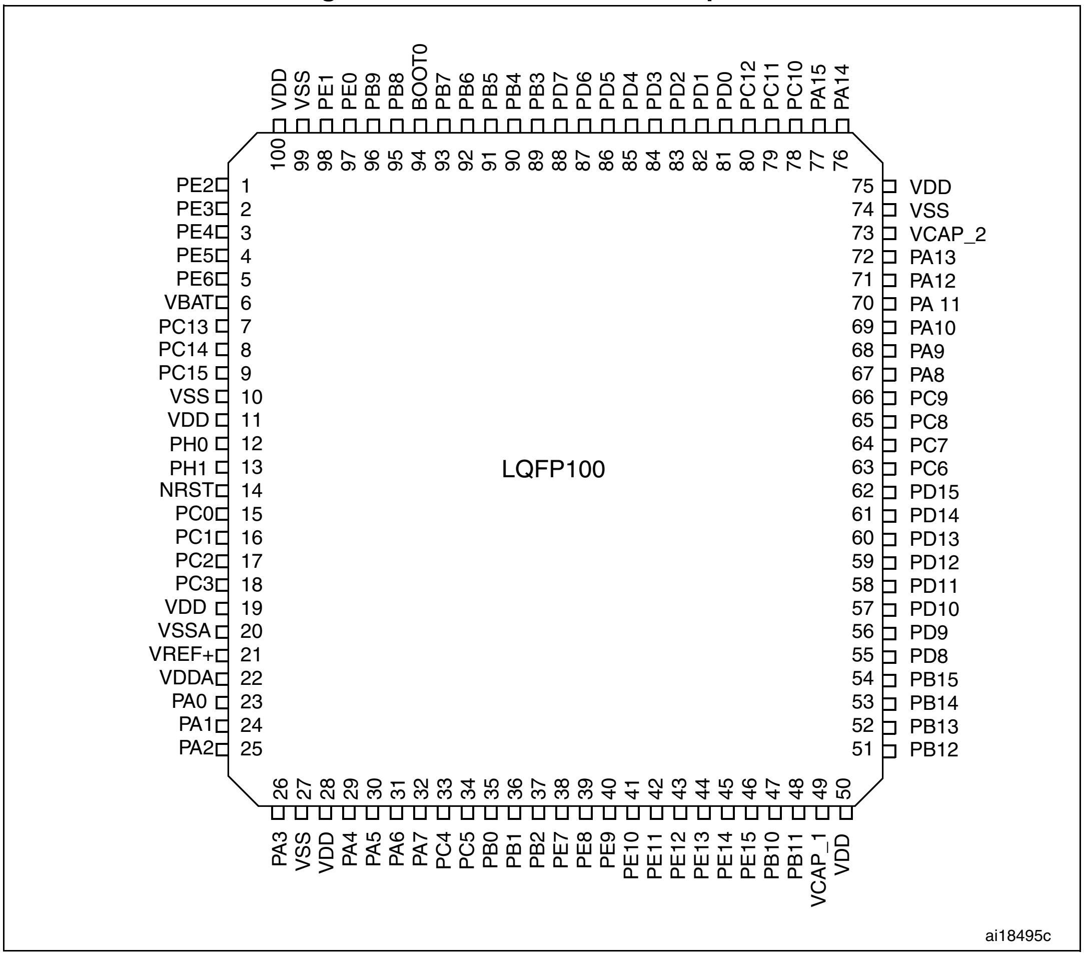
## 3.25 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

# 4 Pinouts and pin description

**Figure 11. STM32F42x LQFP100 pinout**



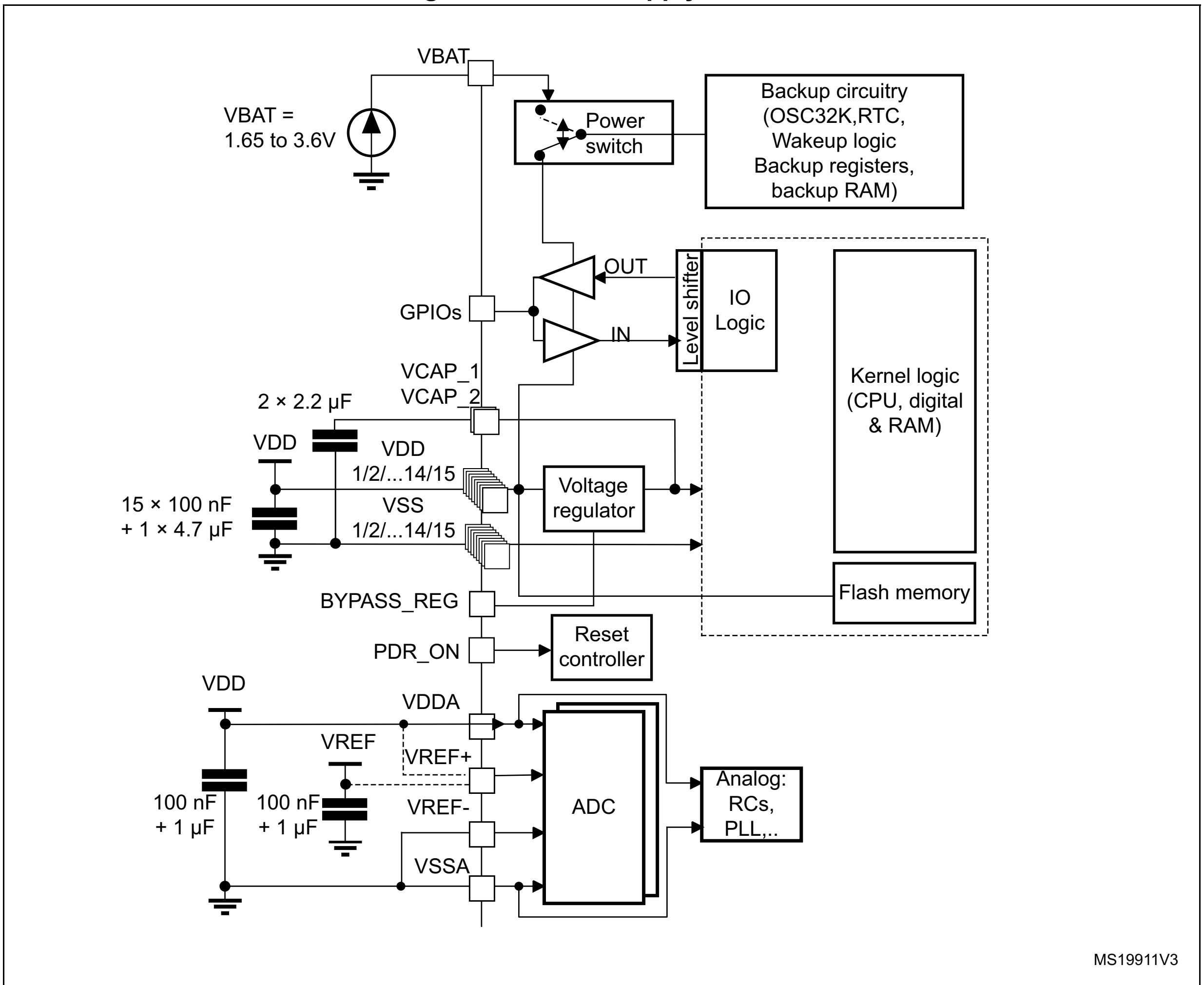

1. The above figure shows the package top view.

**Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)**

| Pin number | | | | | | | | Pin name (function after reset)(1) | Pin type | I / O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | UFBGA176 | LQFP176 | WLCSP143 | LQFP208 | TFBGA216 | | | | | | |
| - | 125 | C7 | B10 | 153 | C6 | 179 | C8 | PG10 | I/O | FT | - | LCD_G3, FMC_NCE4_1/FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT | - |
| - | 126 | B7 | B9 | 154 | B6 | 180 | B8 | PG11 | I/O | FT | - | ETH_MII_TX_EN/ETH_RMII_TX_EN, FMC_NCE4_2, DCMI_D3, LCD_B3, EVENTOUT | - |
| - | 127 | A7 | B8 | 155 | A6 | 181 | C7 | PG12 | I/O | FT | - | SPI6_MISO, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT | - |
| - | 128 | NC (2) | A8 | 156 | D6 | 182 | B3 | PG13 | I/O | FT | - | SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, EVENTOUT | - |
| - | 129 | NC (2) | A7 | 157 | F6 | 183 | A4 | PG14 | I/O | FT | - | SPI6_MOSI, USART6_TX, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, EVENTOUT | - |
| - | 130 | D7 | D7 | 158 | - | 184 | F7 | $V_{SS}$ | S | | - | - | - |
| - | 131 | L6 | C7 | 159 | E6 | 185 | E8 | $V_{DD}$ | S | | - | - | - |
| - | - | - | - | - | - | 186 | D8 | PK3 | I/O | FT | - | LCD_B4, EVENTOUT | - |
| - | - | - | - | - | - | 187 | D7 | PK4 | I/O | FT | - | LCD_B5, EVENTOUT | - |
| - | - | - | - | - | - | 188 | C6 | PK5 | I/O | FT | - | LCD_B6, EVENTOUT | - |
| - | - | - | - | - | - | 189 | C5 | PK6 | I/O | FT | - | LCD_B7, EVENTOUT | - |
| - | - | - | - | - | - | 190 | C4 | PK7 | I/O | FT | - | LCD_DE, EVENTOUT | - |
| - | 132 | C6 | B7 | 160 | A7 | 191 | B7 | PG15 | I/O | FT | - | USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT | - |

### 6.1.6 Power supply scheme

**Figure 22. Power supply scheme**




1. To connect BYPASS_REG and PDR_ON pins, refer to *Section 3.17: Power supply supervisor* and *Section 3.18: Voltage regulator*
2. The two 2.2 μF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 μF ceramic capacitor must be connected to one of the $V_{DD}$ pin.
4. $V_{DDA}$=$V_{DD}$ and $V_{SSA}$=$V_{SS}$.

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for $T_A$.

**Table 20. Operating conditions at power-up / power-down (regulator ON)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | 20 | ∞ | |

### 6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for $T_A$.

**Table 21. Operating conditions at power-up / power-down (regulator OFF)(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | Power-up | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | Power-down | 20 | ∞ | |
| $t_{VCAP}$ | $V_{CAP\_1}$ and $V_{CAP\_2}$ rise time rate | Power-up | 20 | ∞ | |
| | $V_{CAP\_1}$ and $V_{CAP\_2}$ fall time rate | Power-down | 20 | ∞ | |

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when $V_{DD}$ reach below 1.08 V.

### 6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 23: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to $f_{HCLK}$ frequency and $V_{DD}$ range (see *Table 18: Limitations depending on the operating power supply range*).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to $f_{HCLK}$ frequency as follows:
  – Scale 3 for $f_{HCLK} \leq 120$ MHz
  – Scale 2 for 120 MHz < $f_{HCLK} \leq 144$ MHz
  – Scale 1 for 144 MHz < $f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 4 MHz and PLL is ON when $f_{HCLK}$ is higher than 25 MHz.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and a maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

**Table 31. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)(1)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | VDD=3.3 V | | VDD=1.7 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $I_{DD12}$ | $I_{DD}$ | $I_{DD12}$ | $I_{DD}$ | |
| $I_{DD12}$ / $I_{DD}$ | Supply current in RUN mode from $V_{12}$ and $V_{DD}$ supply | All Peripherals enabled | 168 | 77.8 | 1.3 | 76.8 | 1.0 | mA |
| | | | 150 | 70.8 | 1.3 | 69.8 | 1.0 | |
| | | | 144 | 64.5 | 1.3 | 63.6 | 1.0 | |
| | | | 120 | 49.9 | 1.2 | 49.3 | 0.9 | |
| | | | 90 | 39.2 | 1.3 | 38.7 | 1.0 | |
| | | | 60 | 27.2 | 1.2 | 26.8 | 0.9 | |
| | | | 30 | 15.6 | 1.2 | 15.4 | 0.9 | |
| | | | 25 | 13.6 | 1.2 | 13.5 | 0.9 | |
| | | All Peripherals disabled | 168 | 38.2 | 1.3 | 37.0 | 1.0 | |
| | | | 150 | 34.6 | 1.3 | 33.4 | 1.0 | |
| | | | 144 | 31.3 | 1.3 | 30.3 | 1.0 | |
| | | | 120 | 24.0 | 1.2 | 23.2 | 0.9 | |
| | | | 90 | 18.1 | 1.4 | 18.0 | 1.0 | |
| | | | 60 | 12.9 | 1.2 | 12.5 | 0.9 | |
| | | | 30 | 7.2 | 1.2 | 6.9 | 0.9 | |
| | | | 25 | 6.3 | 1.2 | 6.1 | 0.9 | |

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

**Table 34. Switching output I/O current consumption[1]**

| Symbol | Parameter | Conditions | I/O toggling frequency (fsw) | Typ | Unit |
|---|---|---|---|---|---|
| $I_{DDIO}$ | I/O switching Current | $V_{DD}$ = 3.3 V<br>C= $C_{INT}$[2] | 2 MHz | 0.0 | mA |
| | | | 8 MHz | 0.2 | |
| | | | 25 MHz | 0.6 | |
| | | | 50 MHz | 1.1 | |
| | | | 60 MHz | 1.3 | |
| | | | 84 MHz | 1.8 | |
| | | | 90 MHz | 1.9 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 0 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.1 | |
| | | | 8 MHz | 0.4 | |
| | | | 25 MHz | 1.23 | |
| | | | 50 MHz | 2.43 | |
| | | | 60 MHz | 2.93 | |
| | | | 84 MHz | 3.86 | |
| | | | 90 MHz | 4.07 | |
| $I_{DDIO}$ | I/O switching Current | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 10 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.18 | mA |
| | | | 8 MHz | 0.67 | |
| | | | 25 MHz | 2.09 | |
| | | | 50 MHz | 3.6 | |
| | | | 60 MHz | 4.5 | |
| | | | 84 MHz | 7.8 | |
| | | | 90 MHz | 9.8 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 22 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.26 | |
| | | | 8 MHz | 1.01 | |
| | | | 25 MHz | 3.14 | |
| | | | 50 MHz | 6.39 | |
| | | | 60 MHz | 10.68 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 33 pF<br>C = $C_{INT}$ + Cext + $C_S$ | 2 MHz | 0.33 | |
| | | | 8 MHz | 1.29 | |
| | | | 25 MHz | 4.23 | |
| | | | 50 MHz | 11.02 | |

1. $C_S$ is the PCB board capacitance including the pad pin. $C_S$ = 7 pF (estimated value).
2. This test is performed by cutting the LQFP176 package pin (pad removal).

*Figure 33* and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is $f_{PLL\_OUT}$ nominal.

$T_{mode}$ is the modulation period.

md is the modulation depth.

**Figure 33. PLL output clock waveforms in center spread mode**

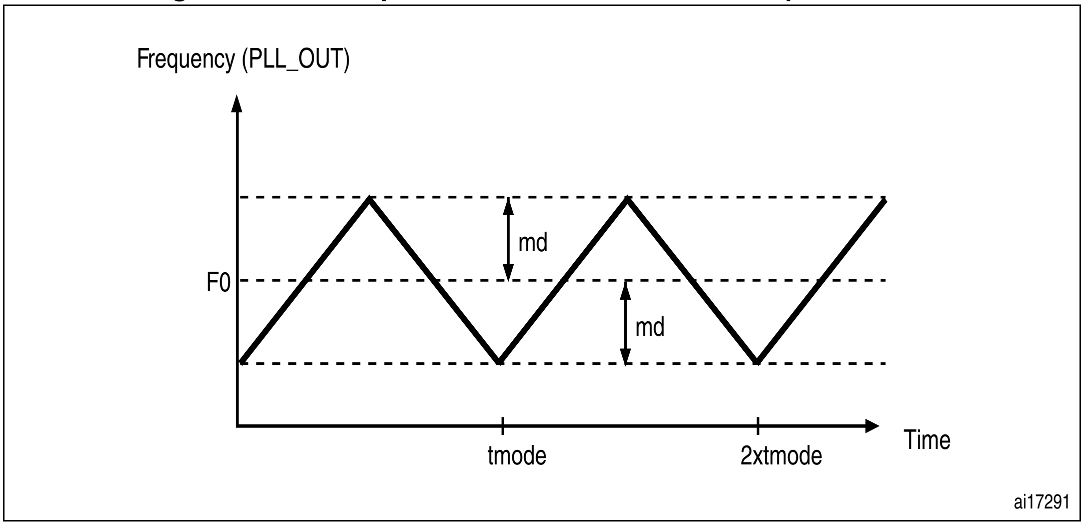
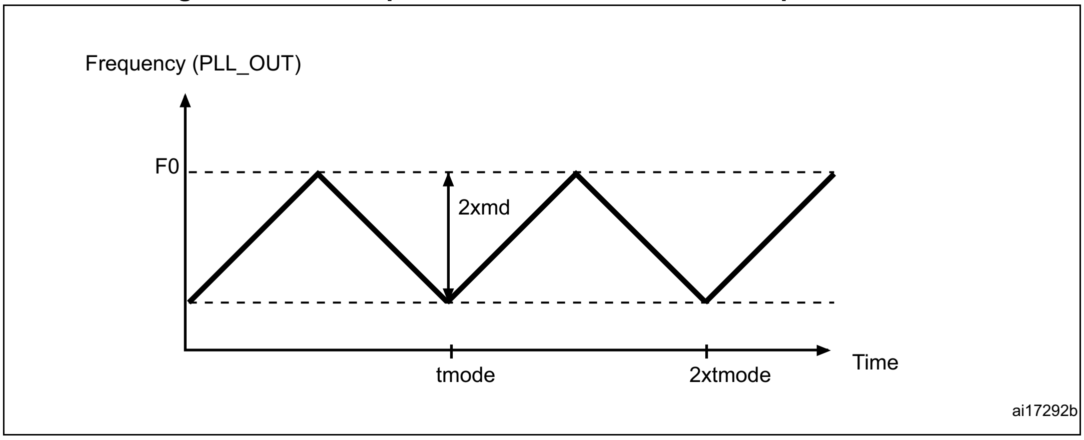



**Figure 34. PLL output clock waveforms in down spread mode**



### Output voltage levels

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

**Table 57. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | CMOS port(2)<br>$I_{IO}$ = +8 mA<br>2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$ − 0.4 | - | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | TTL port(2)<br>$I_{IO}$ =+ 8mA<br>2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA<br>2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 1.3(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$−1.3(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +6 mA<br>1.8 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$−0.4(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA<br>1.7 V ≤ $V_{DD}$ ≤ 3.6V | - | 0.4(5) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$−0.4(5) | - | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Based on characterization data.
5. Guaranteed by design.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 36* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 58. I/O AC characteristics[(1)(2)]**

| OSPEEDRy [1:0] bit value[(1)] | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency[(3)] | $C_L$ = 50 pF, $V_{DD} \geq$ 2.7 V | - | - | 4 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.7 V | - | - | 2 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 8 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.8 V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 3 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ = 1.7 V to 3.6 V | - | - | 100 | ns |
| 01 | $f_{max(IO)out}$ | Maximum frequency[(3)] | $C_L$ = 50 pF, $V_{DD} \geq$ 2.7 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.8 V | - | - | 12.5 | |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.8 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 12.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD} \geq$ 2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 6 | |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.7 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency[(3)] | $C_L$ = 40 pF, $V_{DD} \geq$ 2.7 V | - | - | 50[(4)] | MHz |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 100[(4)] | |
| | | | $C_L$ = 40 pF, $V_{DD} \geq$ 1.7 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.8 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 42.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD} \geq$ 2.7 V | - | - | 6 | ns |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 4 | |
| | | | $C_L$ = 40 pF, $V_{DD} \geq$ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 6 | |

### USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

**Table 65. USB OTG full speed startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$[(1)] | USB OTG full speed transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Table 66. USB OTG full speed DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min.[(1)] | Typ. | Max.[(1)] | Unit |
|---|---|---|---|---|---|---|---|
| Input levels | $V_{DD}$ | USB OTG full speed transceiver operating voltage | | 3.0[(2)] | - | 3.6 | V |
| | $V_{DI}$[(3)] | Differential input sensitivity | I(USB_FS_DP/DM, USB_HS_DP/DM) | 0.2 | - | - | V |
| | $V_{CM}$[(3)] | Differential common mode range | Includes $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{SE}$[(3)] | Single ended receiver threshold | | 1.3 | - | 2.0 | |
| Output levels | $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V[(4)] | - | - | 0.3 | V |
| | $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$[(4)] | 2.8 | - | 3.6 | |
| $R_{PD}$ | | PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM) | $V_{IN} = V_{DD}$ | 17 | 21 | 24 | kΩ |
| | | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | | 0.65 | 1.1 | 2.0 | |
| $R_{PU}$ | | PA12, PB15 (USB_FS_DP, USB_HS_DP) | $V_{IN} = V_{SS}$ | 1.5 | 1.8 | 2.1 | |
| | | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | $V_{IN} = V_{SS}$ | 0.25 | 0.37 | 0.55 | |

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.
3. Guaranteed by design.
4. $R_L$ is the load connected on the USB OTG full speed drivers.

*Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.*

### Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 71*, *Table 72* and *Table 73* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency summarized in *Table 17* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF for 2.7 V < $V_{DD}$ < 3.6 V
- Capacitive load C = 20 pF for 1.71 V < $V_{DD}$ < 3.6 V
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

*Table 71* gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 47* shows the corresponding timing diagram.

**Figure 47. Ethernet SMI timing diagram**

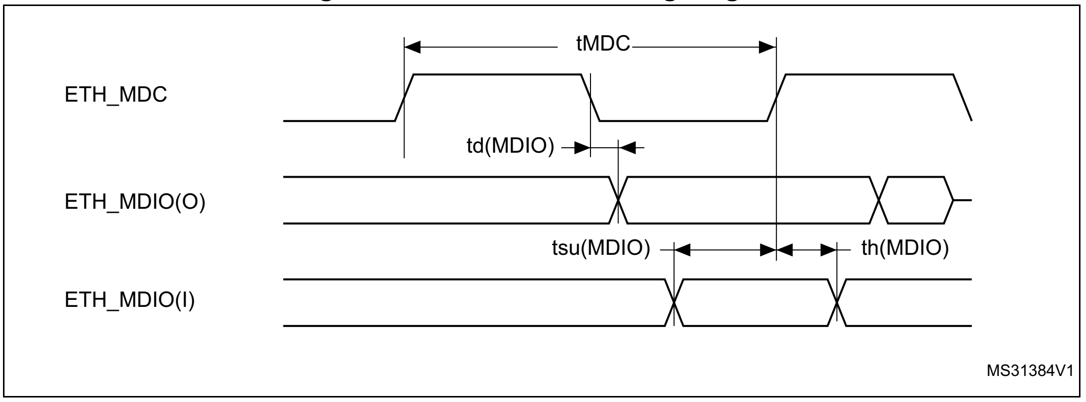



**Table 71. Dynamics characteristics: Ethernet MAC signals for SMI[(1)]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{MDC}$ | MDC cycle time(2.38 MHz) | 411 | 420 | 425 | ns |
| $T_{d(MDIO)}$ | Write data valid time | 6 | 10 | 13 | |
| $t_{su(MDIO)}$ | Read data setup time | 12 | - | - | |
| $t_{h(MDIO)}$ | Read data hold time | 0 | - | - | |

1. Guaranteed by characterization results.

**Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $9T_{HCLK}$ | $9T_{HCLK}+0.5$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $7T_{HCLK}$ | $7T_{HCLK}+2$ | ns |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK}+1.5$ | - | ns |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}-1$ | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

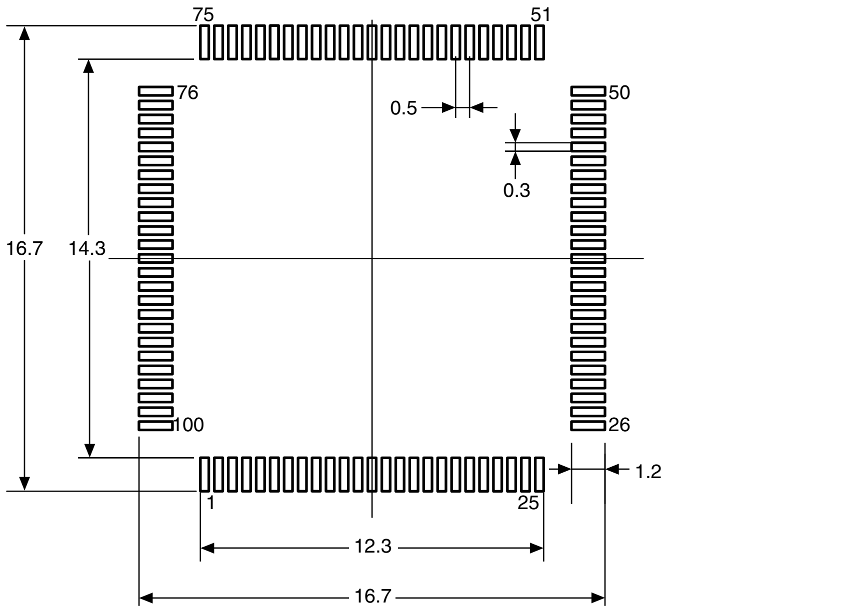
### Synchronous waveforms and timings

*Figure 59* through *Figure 62* represent synchronous waveforms and *Table 94* through *Table 97* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F4xx reference manual : RM0090)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the $T_{HCLK}$ is the HCLK clock period (with maximum FMC_CLK = 90 MHz).

**Figure 81. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**




1. Dimensions are expressed in millimeters.

**Table 111. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | 0.155 | 0.175 | 0.195 | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 4.486 | 4.521 | 4.556 | 0.1766 | 0.1780 | 0.1794 |
| E | 5.512 | 5.547 | 5.582 | 0.2170 | 0.2184 | 0.2198 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 4.000 | - | - | 0.1575 | - |
| e2 | - | 4.800 | - | - | 0.1890 | - |
| F | - | 0.2605 | - | - | 0.0103 | - |
| G | - | 0.3735 | - | - | 0.0147 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Figure 84. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint**

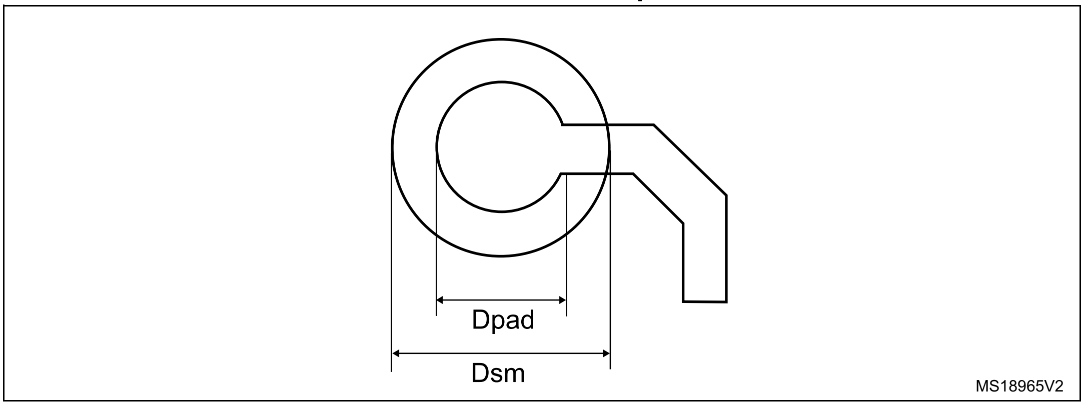


**Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| ZD | - | 1.250 | - | - | 0.0492 | - |
| E | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |
| HE | 25.900 | - | 26.100 | 1.0197 | - | 1.0276 |
| ZE | - | 1.250 | - | - | 0.0492 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L[2] | 0.450 | - | 0.750 | 0.0177 | - | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | - | 7° | 0° | - | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

**Table 124. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 21-Jan-2016 | 8 | Updated *Figure 22: Power supply scheme*.<br>Added $t_{d(TXD)}$ values corresponding to 1.71 V < $V_{DD}$ < 3.6 V in *Table 72: Dynamics characteristics: Ethernet MAC signals for RMII*. |
| 18-Jul-2016 | 9 | Updated *Figure 1: Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package*.<br>Added mission profile compliance with JEDEC JESD47 in *Section 6.2: Absolute maximum ratings*.<br>Changed *Figure 31 HSI deviation versus temperature to ACCHSI versus temperature.*<br>Updated $R_{LOAD}$ in *Table 85: DAC characteristics*.<br>Added note *2.* related to the position of the 0.1 µF capacitor below *Figure 37: Recommended NRST pin protection*.<br>Updated *Figure 40: SPI timing diagram - master mode*.<br>Added reference to optional marking or inset/upset marks in all package device marking sections. Updated *Figure 85: WLCSP143 marking example (package top view)*, *Figure 88: LQFP144 marking example (package top view)*, *Figure 91: LQFP176 marking (package top view)*, *Figure 94: LQFP208 marking example (package top view)*.<br>Updated *Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline* and *Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data*. |