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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	82
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427vit6tr

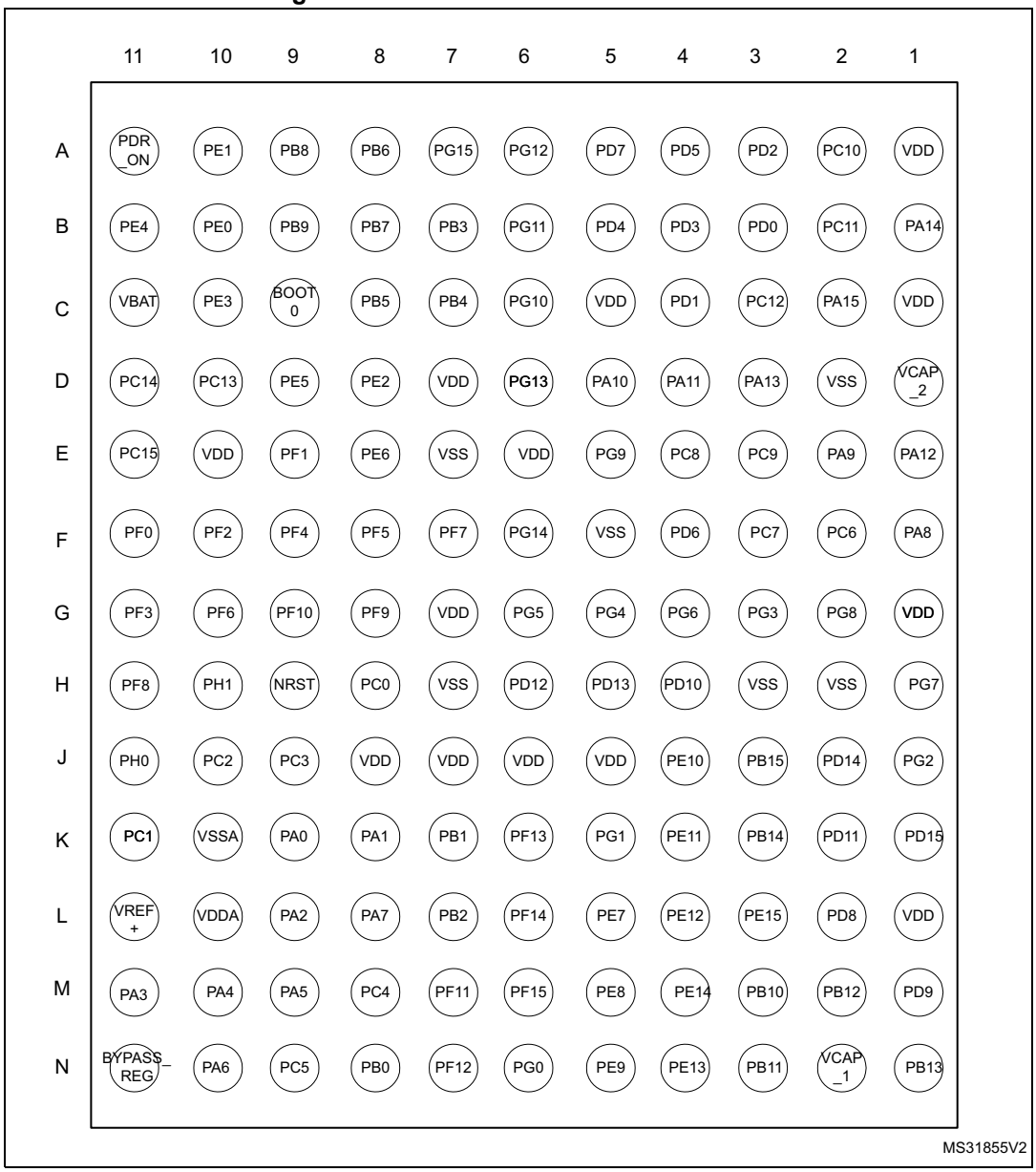
1 Introduction

This datasheet provides the description of the STM32F427xx and STM32F429xx line of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F427xx and STM32F429xx datasheet should be read in conjunction with the STM32F4xx reference manual.

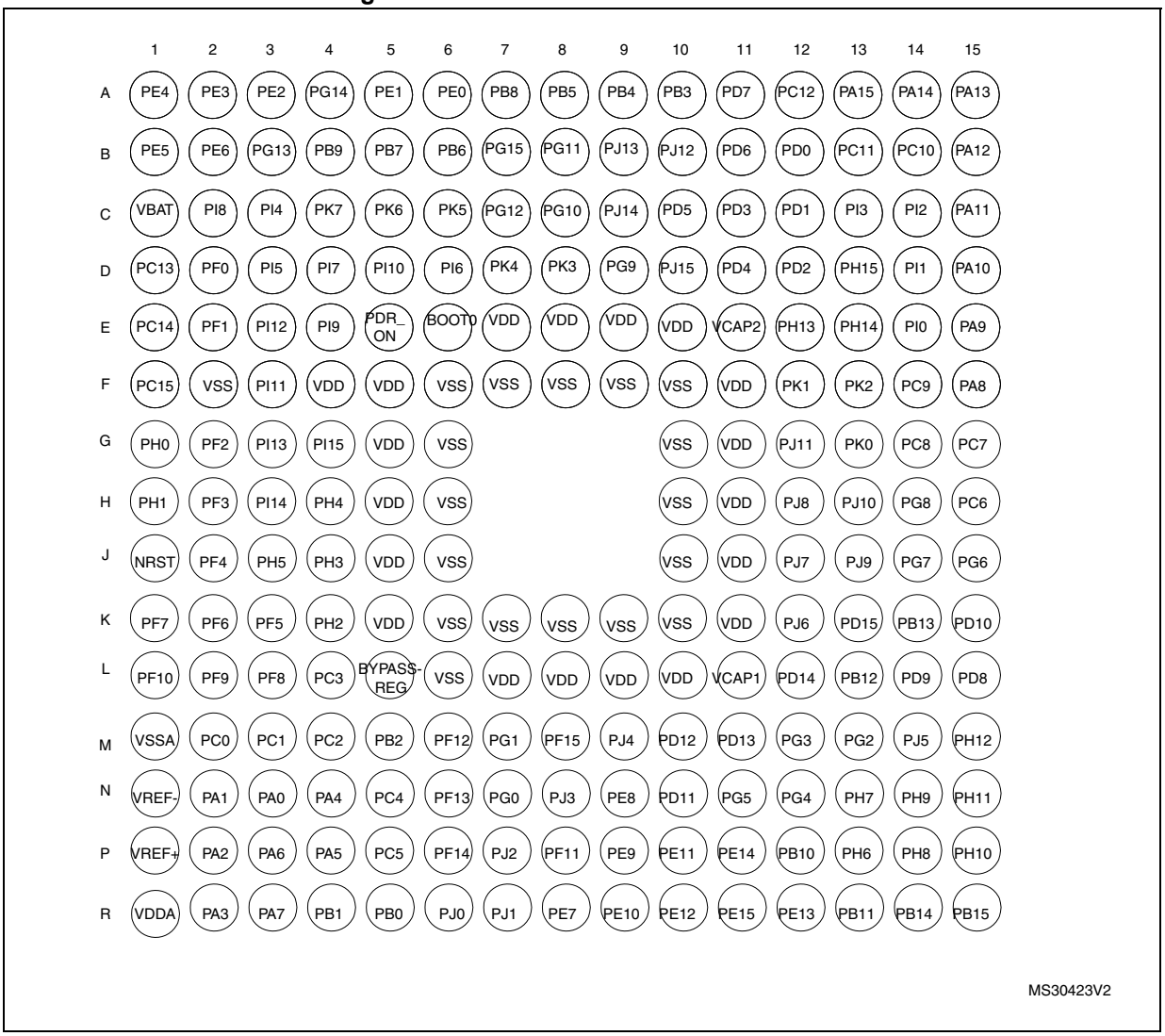
For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214), available from *www.st.com*.

Figure 12. STM32F42x WLCSP143 ballout



1. The above figure shows the package bump view.

Figure 18. STM32F42x TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
82	115	C9	C12	143	C4	165	C12	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-
83	116	B9	D12	144	A3	166	D12	PD2	I/O	FT	-	TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
84	117	A9	D11	145	B4	167	C11	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	118	D8	D10	146	B5	168	D11	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
86	119	C8	C11	147	A4	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	120	-	D8	148	-	170	F8	V_{SS}	S		-	-	-
-	121	D6	C8	149	C5	171	E9	V_{DD}	S		-	-	-
87	122	B8	B11	150	F4	172	B11	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	123	A8	A11	151	A5	173	A11	PD7	I/O	FT	-	USART2_CK, FMC_NE1/FMC_NCE2, EVENTOUT	-
-	-	-	-	-	-	174	B10	PJ12	I/O	FT	-	LCD_B0, EVENTOUT	-
-	-	-	-	-	-	175	B9	PJ13	I/O	FT	-	LCD_B1, EVENTOUT	-
-	-	-	-	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	124	NC (2)	C10	152	E5	178	D9	PG9	I/O	FT	-	USART6_RX, FMC_NE2/FMC_NCE3, DCMI_VSYNC(8), EVENTOUT	-

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port A	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	-	-	-	-	-	-	-	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK/I2S3_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	FMC_SDNE1	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port G	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FMC_NE2/FMC_NCE3	DCMI_VSYNC (1)	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	FMC_NCE4_1/FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_NCE4_2	DCMI_D3	LCD_B3	EVENTOUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENTOUT
	PG13	-	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	-	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	-	FMC_SDNE1	DCMI_D8	-	-

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	DMA2D
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0X4002 5000 - 0X4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0X4002 3400 - 0X4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0X4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	120	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	144	
			Over-drive ON		-	168	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	42	
		Over-drive ON		0	-	45	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	84	
		Over-drive ON		0	-	90	
V_{DD}	Standard operating voltage			1.7[2]	-	3.6	V
V_{DDA} [3][4]	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}[5]		1.7[2]	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)			2.4	-	3.6	
V_{BAT}	Backup operating voltage			1.65	-	3.6	
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 120 MHz HCLK max frequency		1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 144 MHz HCLK max frequency with over-drive OFF or 168 MHz with over-drive ON		1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON		1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins[6]	Max frequency 120 MHz		1.10	1.14	1.20	
		Max frequency 144 MHz		1.20	1.26	1.32	
		Max frequency 168 MHz		1.26	1.32	1.38	

Table 34. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
I_{DDIO}	I/O switching Current	V_{DD} = 3.3 V C= C_{INT}(2)	2 MHz	0.0	mA
			8 MHz	0.2	
			25 MHz	0.6	
			50 MHz	1.1	
			60 MHz	1.3	
			84 MHz	1.8	
			90 MHz	1.9	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.1	
			8 MHz	0.4	
			25 MHz	1.23	
			50 MHz	2.43	
			60 MHz	2.93	
			84 MHz	3.86	
			90 MHz	4.07	
I_{DDIO}	I/O switching Current	V_{DD} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.18	mA
			8 MHz	0.67	
			25 MHz	2.09	
			50 MHz	3.6	
			60 MHz	4.5	
			84 MHz	7.8	
			90 MHz	9.8	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.26	
			8 MHz	1.01	
			25 MHz	3.14	
			50 MHz	6.39	
			60 MHz	10.68	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + Cext + C_S	2 MHz	0.33	
			8 MHz	1.29	
			25 MHz	4.23	
			50 MHz	11.02	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP176 package pin (pad removal).

Table 44. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)			0.95(2)	1	2.10	MHz
f_{PLLSAI_OUT}	PLLSAI multiplier output clock			-	-	216	MHz
f_{VCO_OUT}	PLLSAI VCO output			100	-	432	MHz
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Main SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLSAI)}$(4)	PLLSAI power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}$(4)	PLLSAI power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 64* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 64. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256 x 8K	256xFs(2)	MHz
F_{SCK}	SAI clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{SCK}	SAI clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(FS)}$	FS valid time	Master mode	8	22	ns
$t_{su(FS)}$	FS setup time	Slave mode	2	-	
$t_{h(FS)}$	FS hold time	Master mode	8	-	
		Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD\_SR)}$		Slave receiver	3	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	22	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	8	-	

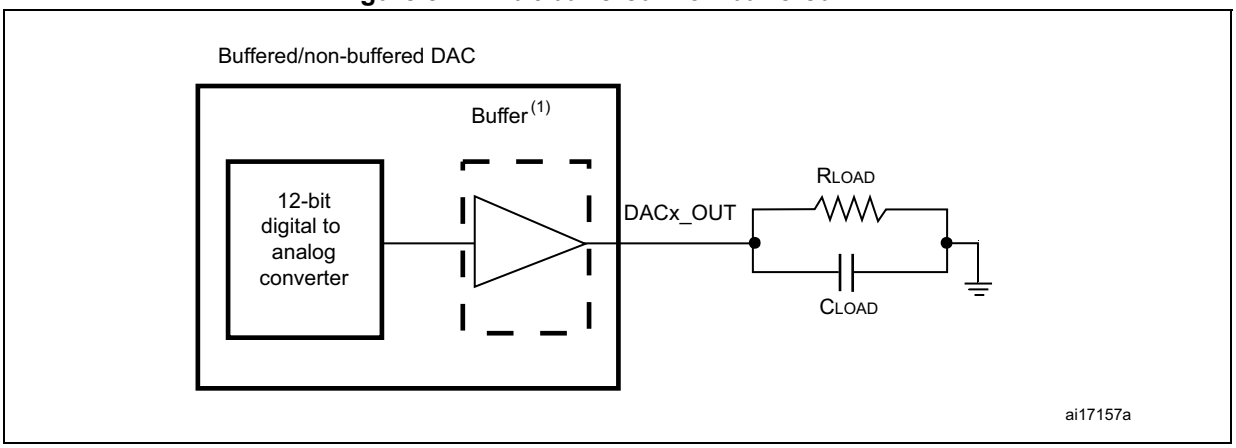
1. Guaranteed by characterization results.
2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)

Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

Figure 54. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+1$	$8T_{HCLK}+2$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK} - 1$	$6T_{HCLK}+2$	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$		ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Figure 57. Asynchronous multiplexed PSRAM/NOR read waveforms

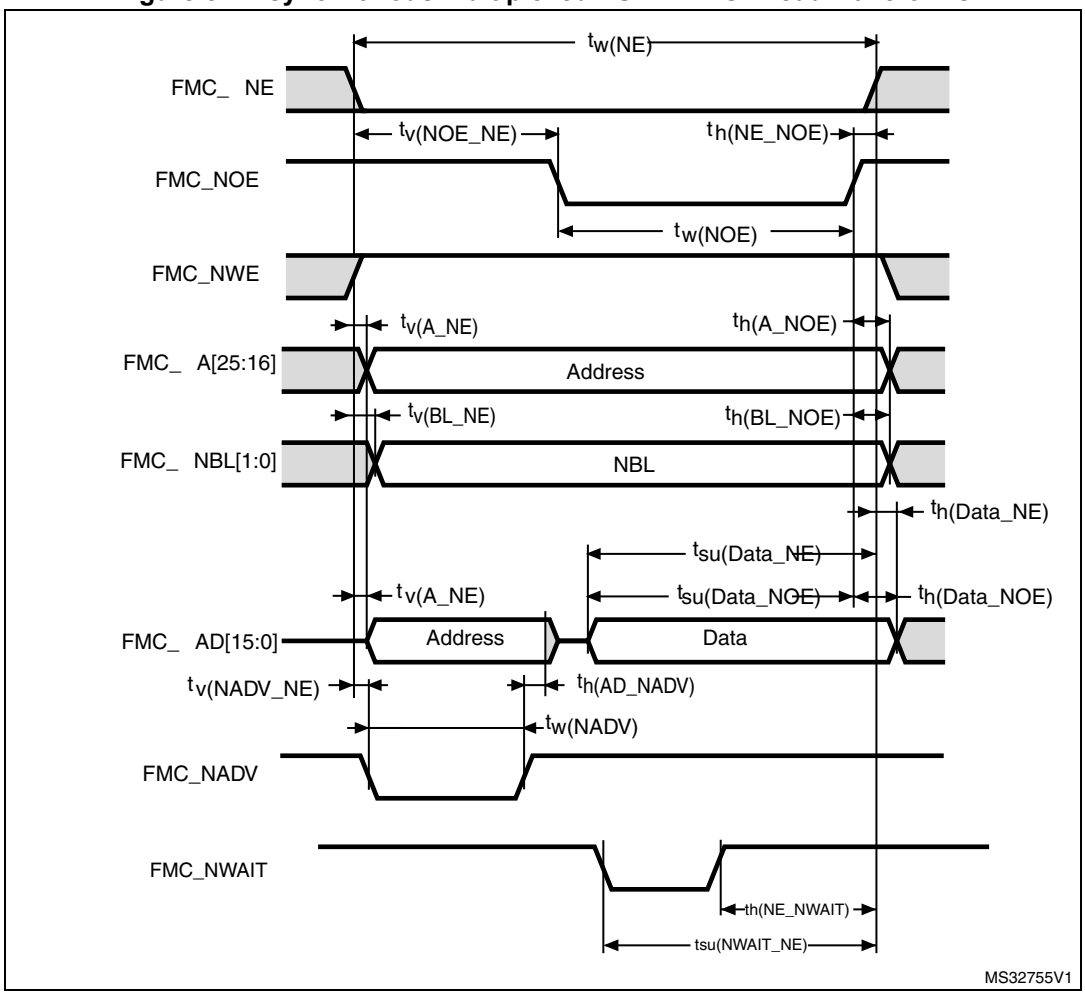


Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms

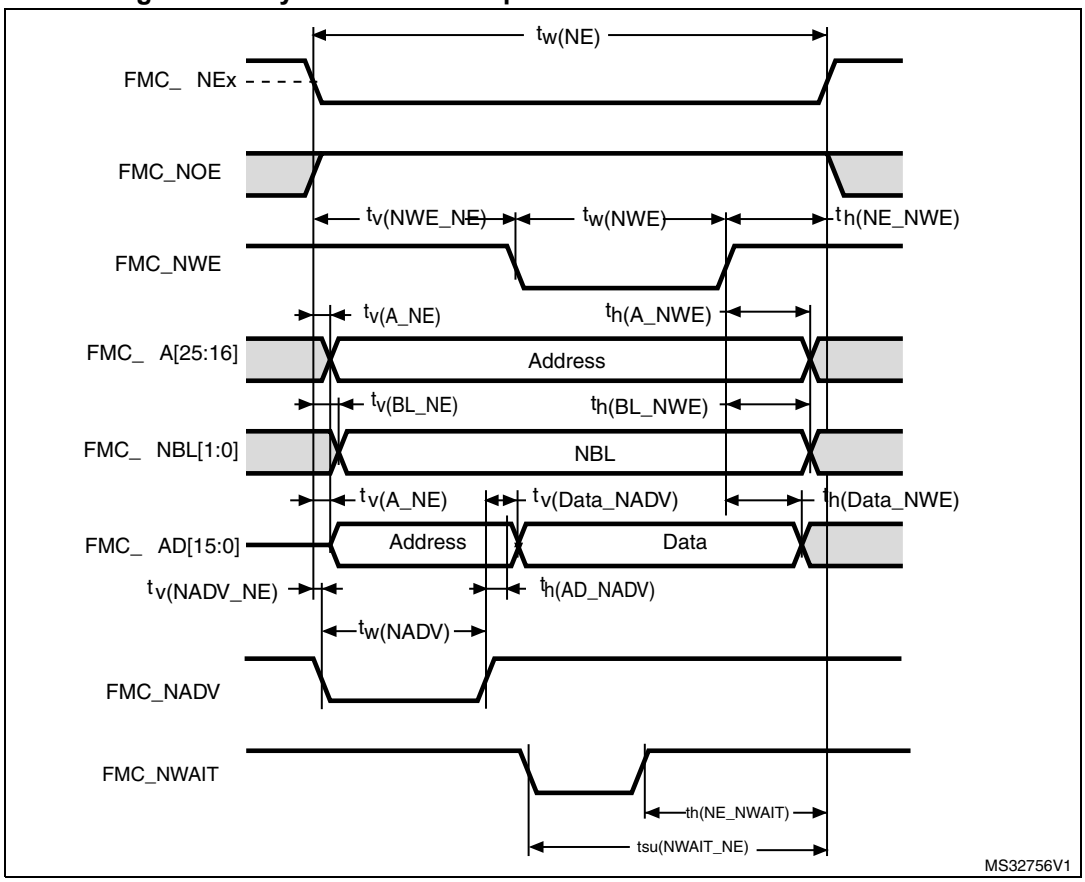


Table 92. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	ns
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{HCLK} - 2$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	ns
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK}+1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 94. Synchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	5	-	ns
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	0	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Figure 60. Synchronous multiplexed PSRAM write timings

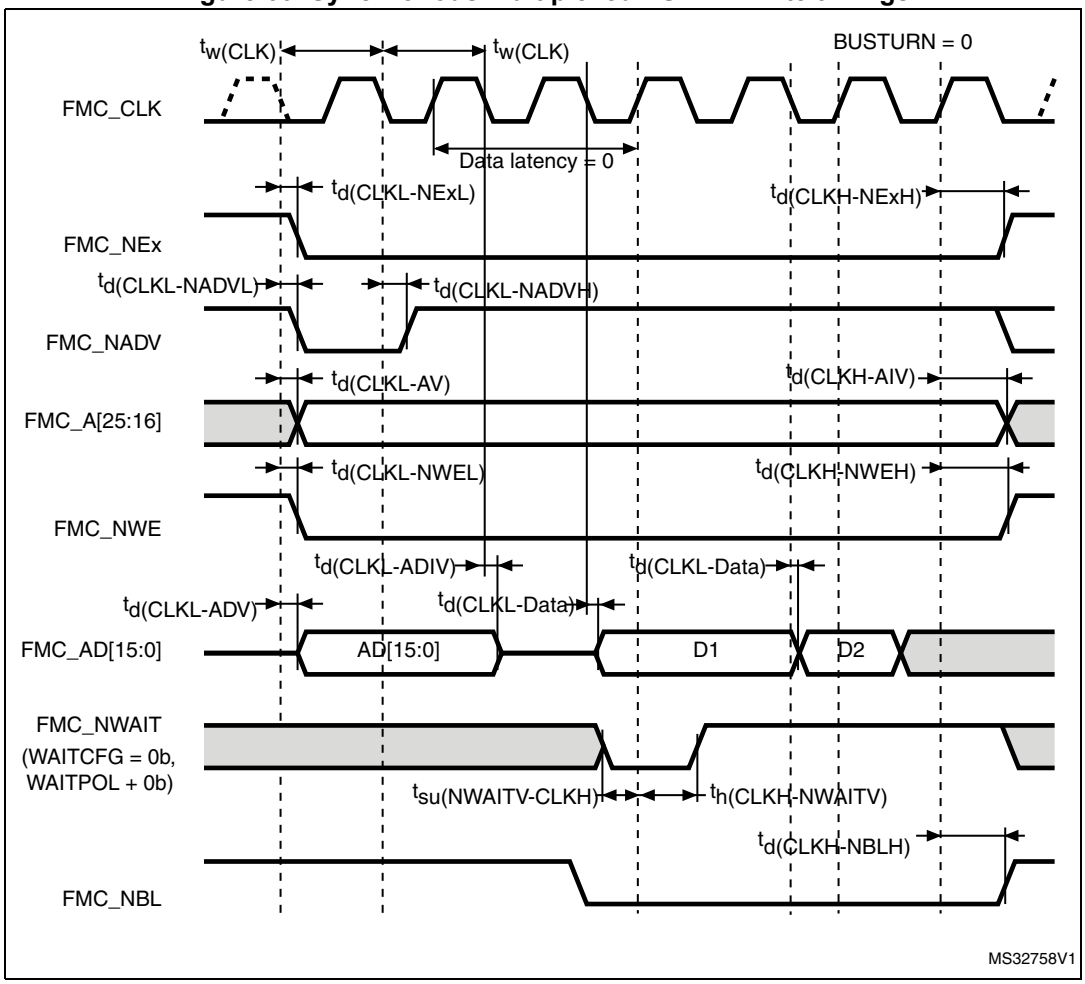
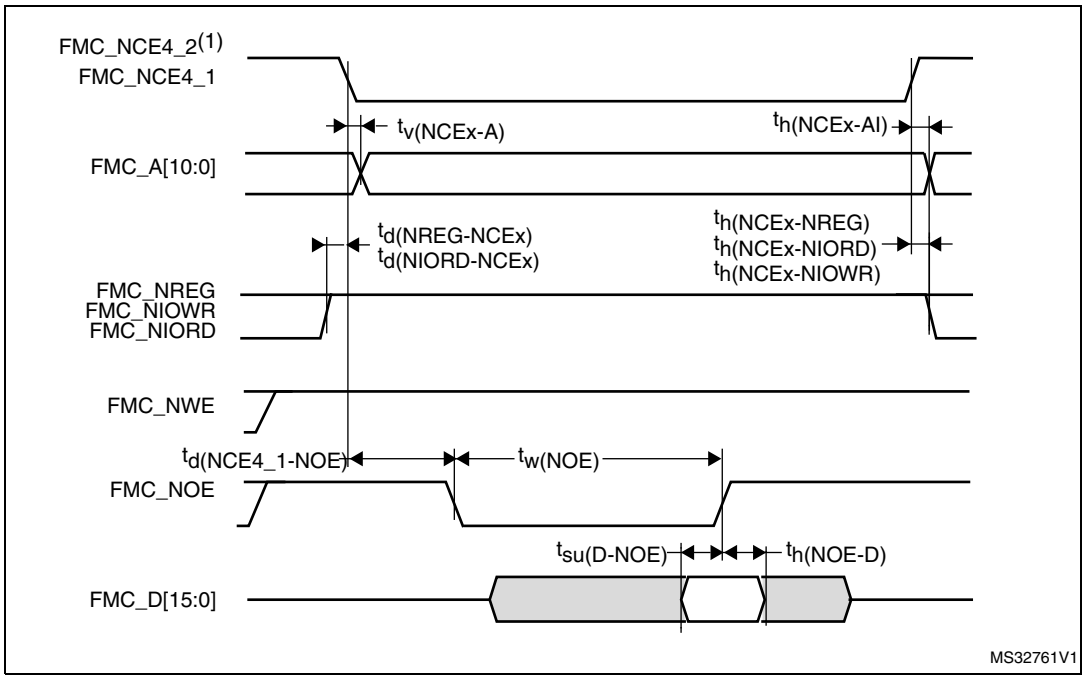
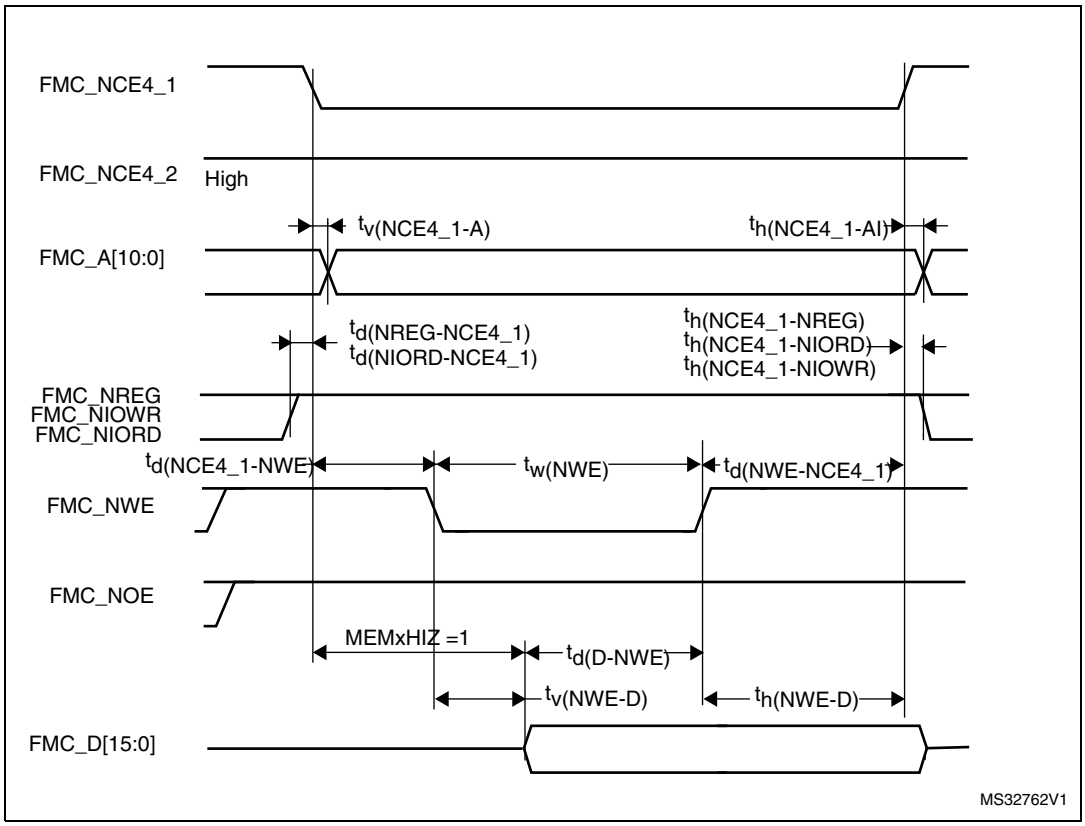


Figure 63. PC Card/CompactFlash controller waveforms for common memory read access



1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 64. PC Card/CompactFlash controller waveforms for common memory write access

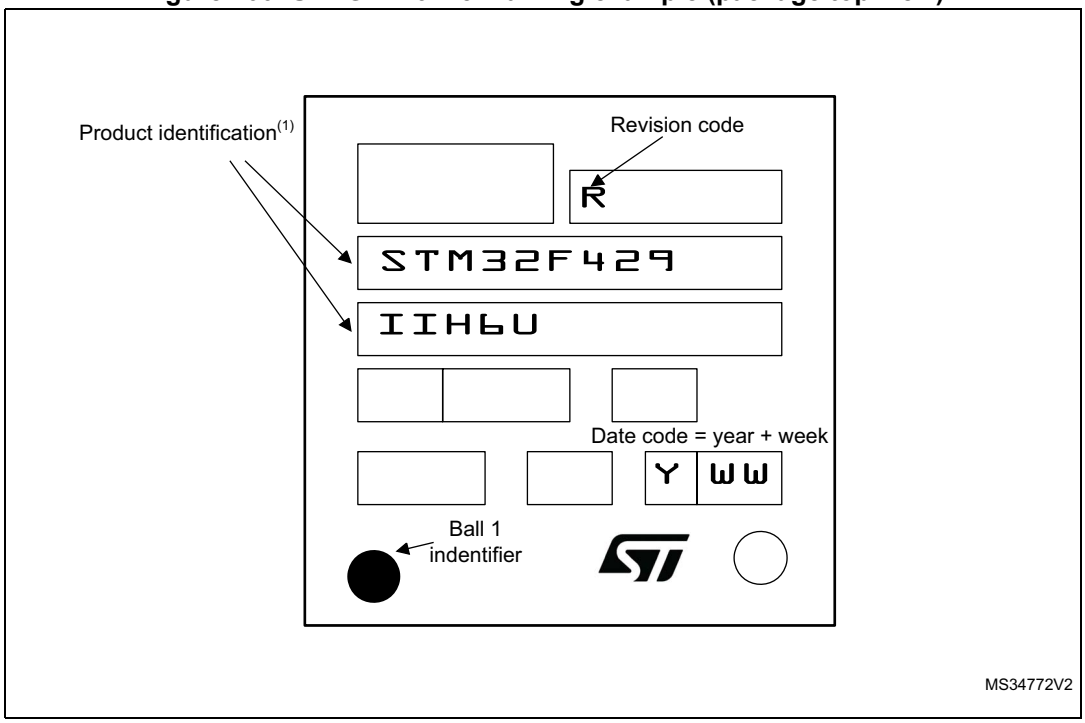


Device marking for UFBGA176+25

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 100. UFBGA176+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

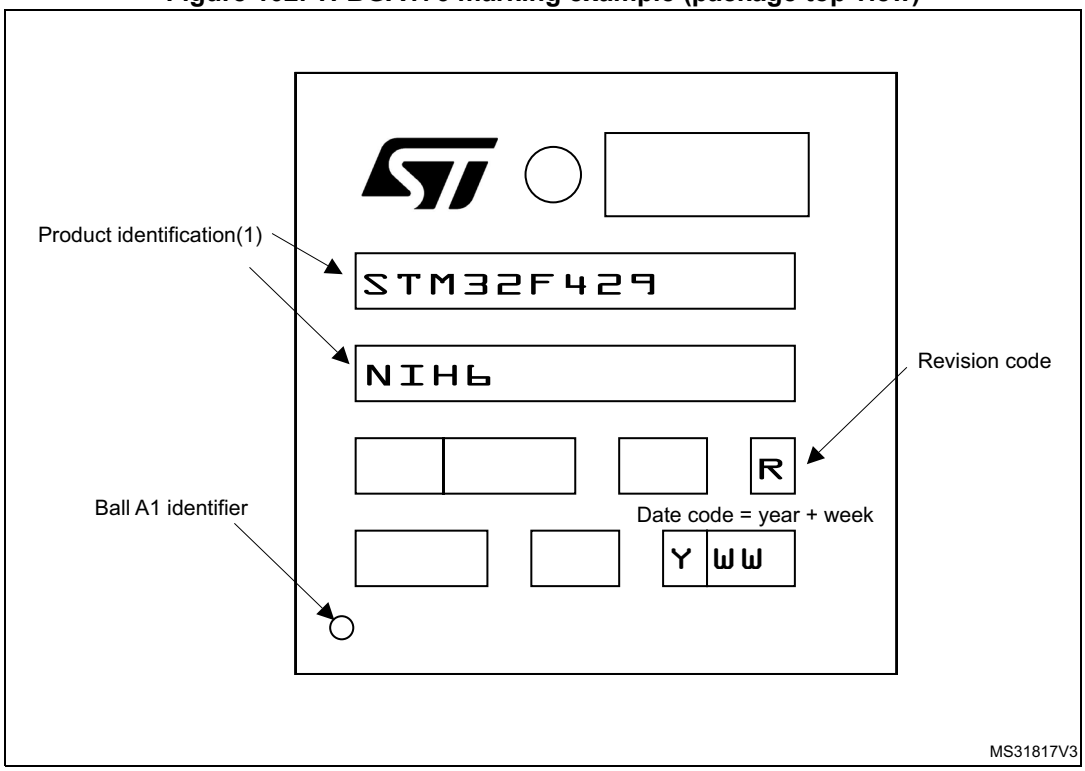
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for TFBGA176

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 102. TFBGA176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

9 Revision history

Table 124. Document revision history

Date	Revision	Changes
19-Mar-2013	1	Initial release.
10-Sep-2013	2	Added STM32F429xx part numbers and related informations. **STM32F427xx part numbers:** Replaced FSMC by FMC added Chrom-ART Accelerator and SAI interface. Increased core, timer, GPIOs, SPI maximum frequencies Updated *Figure 8*.Updated *Figure 9*. Removed note in *Section ·: Standby mode*. Updated *Figure 18*. Updated *Table 10: STM32F427xx and STM32F429xx pin and ball definitions* and *Table 12: STM32F427xx and STM32F429xx alternate function mapping*.. Modified *Figure 19: Memory map*. Updated *Table 17: General operating conditions*, *Table 18: Limitations depending on the operating power supply range*. Removed note 1 in *Table 22: reset and power control block characteristics*. Added *Table 23: Over-drive switching characteristics*. Updated *Section : Typical and maximum current consumption*, *Table 34: Switching output I/O current consumption*, *Table 35: Peripheral current consumption* and *Section : On-chip peripheral current consumption*. Updated *Table 36: Low-power mode wakeup timings*. Modified *Section : High-speed external user clock generated from an external source*, *Section : Low-speed external user clock generated from an external source*, and *Section 6.3.10: Internal clock source characteristics*. Updated *Table 43: Main PLL characteristics* and *Table 45: PLLISAI (audio and LCD-TFT PLL) characteristics*. Updated *Table 52: EMI characteristics*. Updated *Table 57: Output voltage characteristics* and *Table 58: I/O AC characteristics*. Updated *Table 60: TIMx characteristics*, *Table 61: I^2C characteristics*, *Table 62: SPI dynamic characteristics*, *Section : SAI characteristics*. Updated *Table 102: SDRAM read timings* and *Table 104: SDRAM write timings*.

Table 124. Document revision history

Date	Revision	Changes
19-Feb-2015	5	Update SPI/IS2 in *Table 2: STM32F427xx and STM32F429xx features and peripheral counts*. Updated LQFP208 in *Table 4: Regulator ON/OFF and internal reset ON/OFF availability*. Updated *Figure 19: Memory map*. Changed PLS[2:0]=101 (falling edge) maximum value in *Table 22: reset and power control block characteristics*. Updated current consumption with all peripherals disabled in *Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM*. Updated note *1.* in *Table 28: Typical and maximum current consumptions in Standby mode*. Updated t_{WUSTOP} in *Table 36: Low-power mode wakeup timings*. Updated ESD standards and *Table 53: ESD absolute maximum ratings*. Updated *Table 56: I/O static characteristics*. *Section : I2C interface characteristics*: updated section introduction, removed Table *I2C characteristics*, Figure *I2C bus AC waveforms and measurement circuit* and Table *SCL frequency*; added *Table 61: I2C analog filter characteristics*. Updated measurement conditions in *Table 62: SPI dynamic characteristics*. Updated *Figure 51: Typical connection diagram using the ADC*. Updated *Section : Device marking for LQFP100*. Updated *Figure 83: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline* and *Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data*; added *Figure 84: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint* and *Table 112: WLCSP143 recommended PCB design rules (0.4 mm pitch)*. Updated *Figure 85: WLCSP143 marking example (package top view)* and related note. Updated *Section : Device marking for WLCSP143*. Updated *Section : Device marking for LQFP144*. Updated *Section : Device marking for LQFP176*. Updated *Figure 92: LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline*; Updated *Section : Device marking for LQFP208*. Modified UFBGA169 pitch, updated *Figure 95: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 116: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*; updated *Section : Device marking for LQFP208*. updated *Section : Device marking for UFBGA169*, *Section : Device marking for UFBGA176+25* and *Section : Device marking for TFBGA176*. Updated Z pin count in *Table 122: Ordering information scheme*.