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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f427zit6tr

Table 1. Device summary

Reference	Part number
STM32F427xx	STM32F427VG, STM32F427ZG, STM32F427IG, STM32F427AG, STM32F427VI, STM32F427ZI, STM32F427II, STM32F427AI
STM32F429xx	STM32F429VG, STM32F429ZG, STM32F429IG, STM32F429BG, STM32F429NG, STM32F429AG, STM32F429VI, STM32F429ZI, STM32F429II,, STM32F429BI, STM32F429NI, STM32F429AI, STM32F429VE, STM32F429ZE, STM32F429IE, STM32F429BE, STM32F429NE

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reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit.

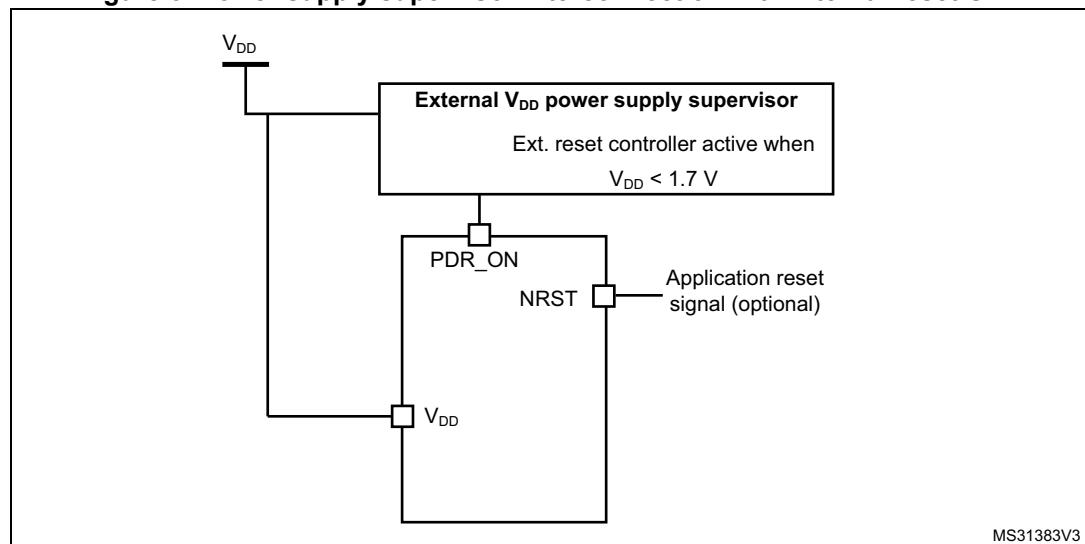
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to [Figure 6: Power supply supervisor interconnection with internal reset OFF](#).

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see [Figure 7](#)).

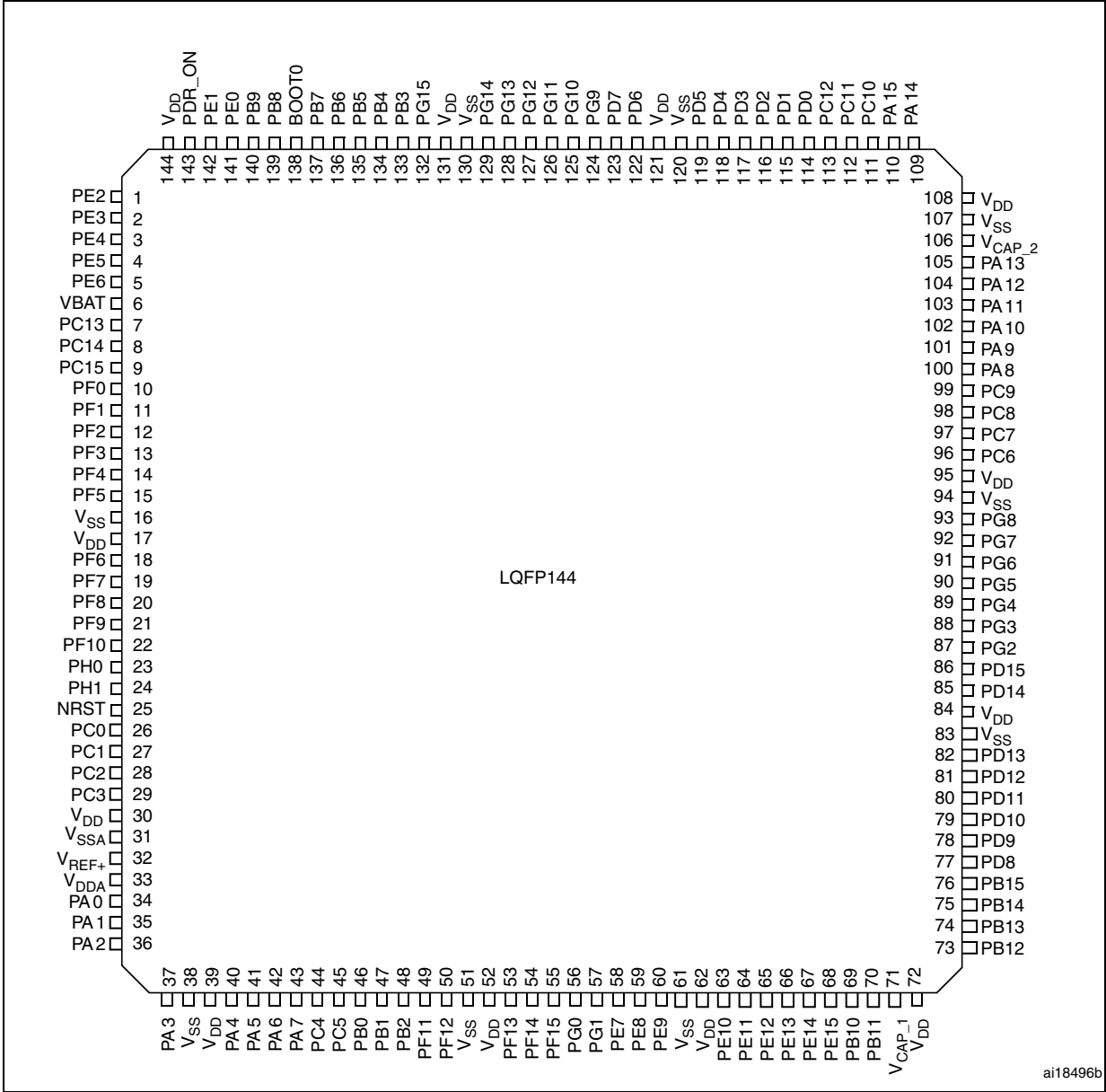
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .

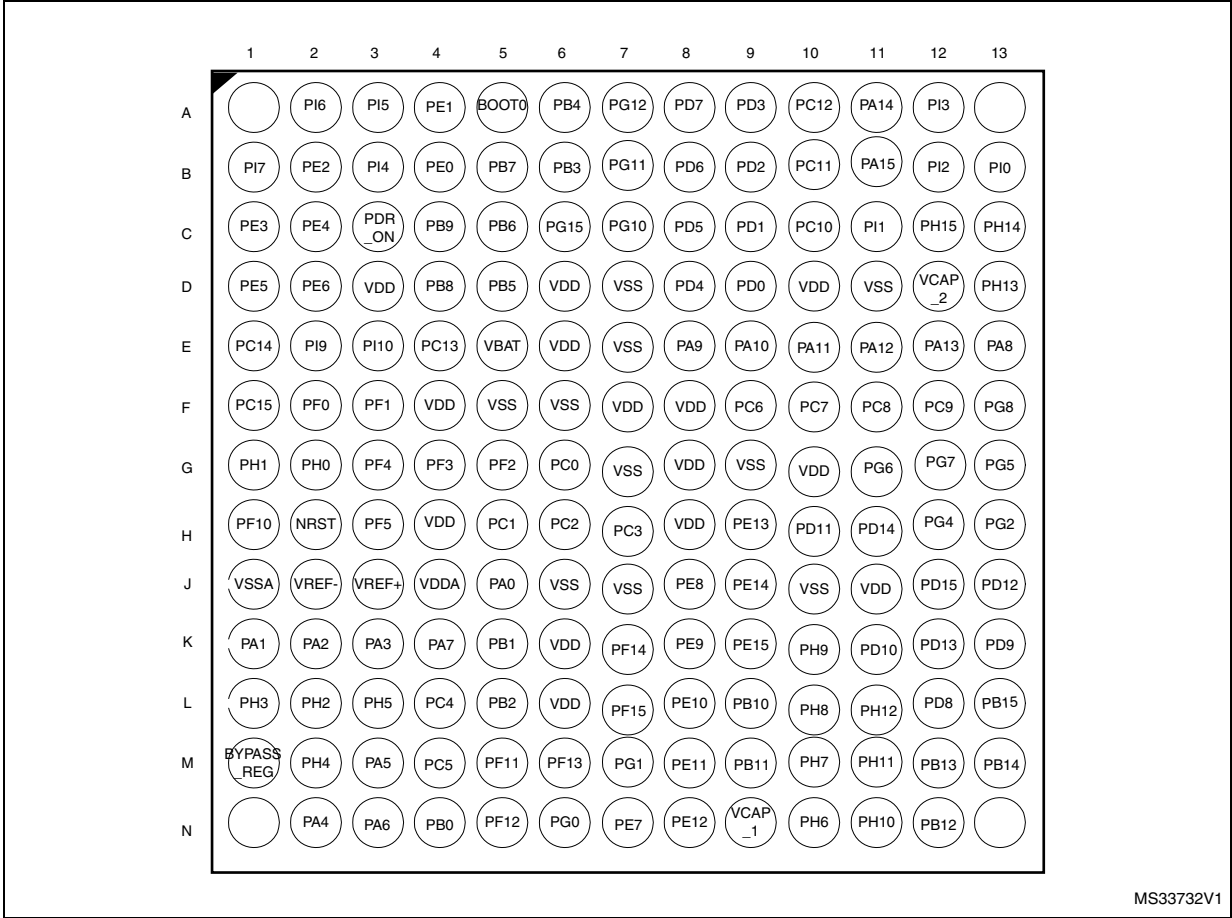
All packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal.

Figure 13. STM32F42x LQFP144 pinout



1. The above figure shows the package top view.

Figure 16. STM32F42x UFBGA169 ballout



MS33732V1

1. The above figure shows the package top view.
2. The 4 corners balls, A1,A13, N1 and N13, are not bonded internally and should be left not connected on the PCB.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	-	M1	L4	48	N11	-	L5	BYPASS_ REG	I	FT	-	-	-
28	39	J11	K4	49	J8	52	K5	V _{DD}	S	-	-	-	-
29	40	N2	N4	50	M10	53	N4	PA4	I/O	TTa	(5)	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_ IN4 /DAC_ OUT1
30	41	M3	P4	51	M9	54	P4	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, EVENTOUT	ADC12_ IN5/DAC_ OUT2
31	42	N3	P3	52	N10	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_ IN6
32	43	K4	R3	53	L8	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_ RMII_CRS_DV, EVENTOUT	ADC12_ IN7
33	44	L4	N5	54	M8	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_ RMII_RXD0, EVENTOUT	ADC12_ IN14
34	45	M4	P5	55	N9	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_ RMII_RXD1, EVENTOUT	ADC12_ IN15
-	-	-	-	-	J7	59	L7	V _{DD}	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
35	46	N4	R5	56	N8	61	R5	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_ IN8
36	47	K5	R4	57	K7	62	R4	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_ IN9
37	48	L5	M6	58	L7	63	M5	PB2-BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	M5	R6	59	M7	70	P8	PF11	I/O	FT	-	SPI5_MOSI, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	N5	P6	60	N7	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	51	G9	M8	61	-	72	K7	V _{SS}	S		-	-	-
-	52	D10	N8	62	-	73	L8	V _{DD}	S		-	-	-
-	53	M6	N6	63	K6	74	N6	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	54	K7	R7	64	L6	75	P6	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	55	L7	P7	65	M6	76	M8	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	56	N6	N7	66	N6	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	M7	67	K5	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
51	73	N12	P12	92	M2	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_R MII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	M12	P13	93	N1	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_R MII_TXD1, EVENTOUT	OTG_HS_ VBUS
53	75	M13	R14	94	K3	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	76	L13	R15	95	J3	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	77	L12	P15	96	L2	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
56	78	K13	P14	97	M1	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	79	K11	N15	98	H4	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port I	PI7	-	-	-	TIM8_ CH3	-	-	-	-	-	-	-	-	FMC_D29	DCMI_ D7	LCD_B7	EVEN TOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D30	-	LCD_ VSYNC	EVEN TOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ RX_ER	FMC_D31	-	LCD_ HSYNC	EVEN TOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ ULPI_DIR	-	-	-	-	EVEN TOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ HSYNC	EVEN TOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ VSYNC	EVEN TOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ CLK	EVEN TOUT
	PI15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R0	EVEN TOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R1	EVEN TOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVEN TOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVEN TOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVEN TOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVEN TOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVEN TOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVEN TOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVEN TOUT

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4000 8000 - 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

Table 35. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
AHB2 (up to 180 MHz)	OTG_FS	25.67	26.67	23.58	μA/MHz
	DCMI	3.72	3.40	3.00	
	RNG	2.28	2.36	2.17	
AHB3 (up to 180 MHz)	FMC	21.39	19.79	17.50	μA/MHz
Bus matrix ⁽²⁾		14.06	13.19	11.75	μA/MHz
APB1 (up to 45 MHz)	TIM2	17.56	16.42	14.47	μA/MHz
	TIM3	14.22	13.36	11.80	
	TIM4	14.89	13.64	12.13	
	TIM5	17.33	16.42	14.47	
	TIM6	2.89	2.53	2.47	
	TIM7	3.11	2.81	2.47	
	TIM12	7.33	6.97	6.13	
	TIM13	4.89	4.47	4.13	
	TIM14	5.56	5.31	4.80	
	PWR	11.11	10.31	9.13	
	USART2	4.22	3.92	3.47	
	USART3	4.44	4.19	3.80	
	UART4	4.00	3.92	3.47	
	UART5	4.00	3.92	3.47	
	UART7	4.00	3.92	3.47	
	UART8	3.78	3.92	3.47	
	I2C1	4.00	3.92	3.47	
	I2C2	4.00	3.92	3.47	
	I2C3	4.00	3.92	3.47	
	SPI2 ⁽³⁾	3.11	3.08	2.80	
	SPI3 ⁽³⁾	3.56	3.36	3.13	
	I2S2	2.89	2.81	2.47	
	I2S3	3.33	3.08	2.80	
	CAN1	6.89	6.42	5.80	
	CAN2	6.67	6.14	5.47	
	DAC ⁽⁴⁾	2.89	2.25	2.13	
	WWDG	0.89	0.86	0.80	

6.3.8 Wakeup time from low-power modes

The wakeup times given in [Table 36](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}=3.3\text{ V}$.

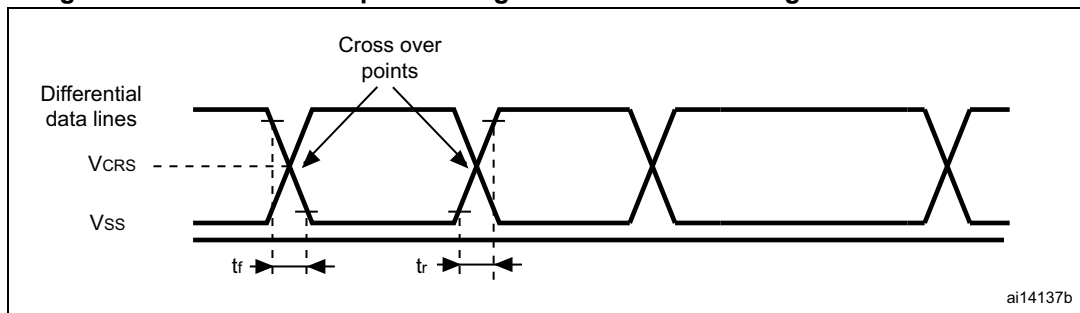
Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	6	-	CPU clock cycle
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	13.6	-	μs
		Main regulator is ON and Flash memory in Deep power down mode	93	111	
		Low power regulator is ON	22	32	
		Low power regulator is ON and Flash memory in Deep power down mode	103	126	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	105	128	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	125	155	
$t_{WUSTDBY}^{(2)(3)}$	Wakeup from Standby mode		318	412	

1. Guaranteed by characterization results.

2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

3. $t_{WUSTDBY}$ maximum value is given at $-40\text{ }^{\circ}\text{C}$.

Figure 45. USB OTG full speed timings: definition of data signal rise and fall time**Table 67. USB OTG full speed electrical characteristics⁽¹⁾**

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V
Z_{DRV}	Output driver impedance ⁽³⁾	Driving high or low	28	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

USB high speed (HS) characteristics

Unless otherwise specified, the parameters given in [Table 70](#) for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 69](#) and V_{DD} supply voltage conditions summarized in [Table 68](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$, unless otherwise specified
- Capacitive load $C = 30 \text{ pF}$, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

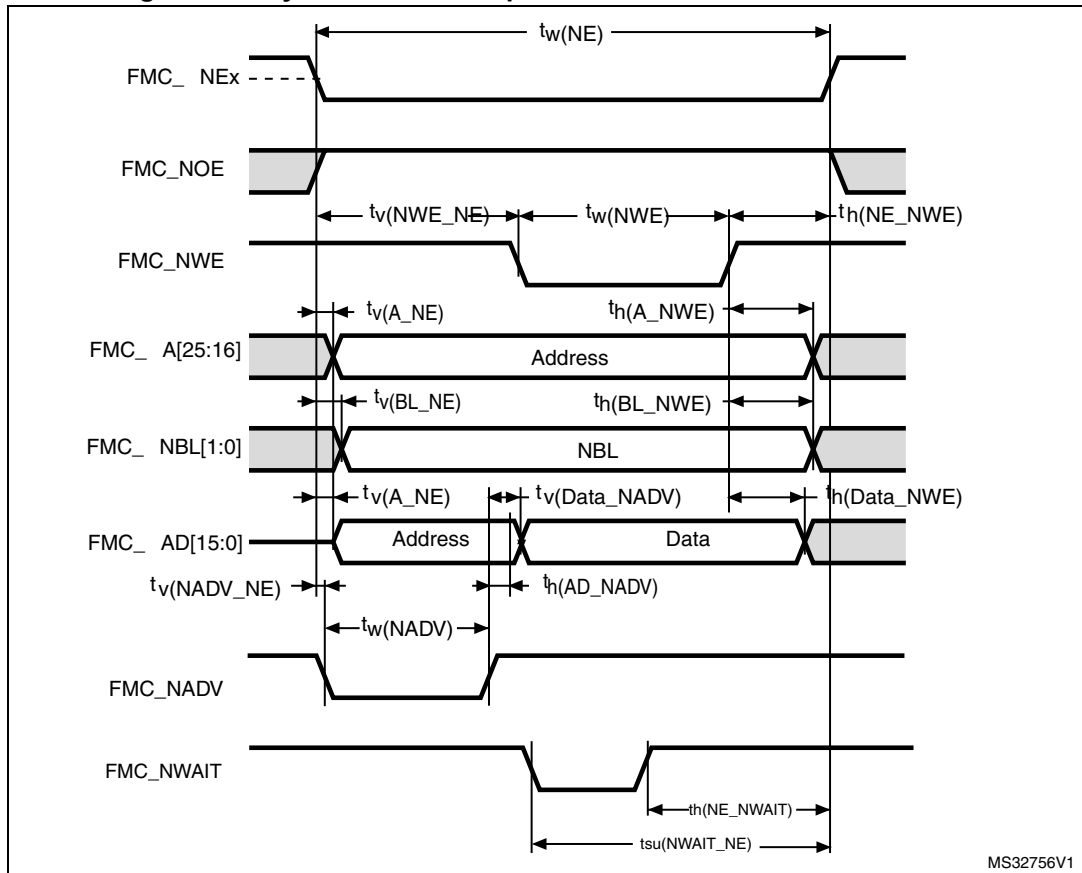
Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

Table 68. USB HS DC electrical characteristics

Symbol		Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level	V_{DD}	USB OTG HS operating voltage	1.7	3.6	V

1. All the voltages are measured from the local ground potential.

Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms



MS32756V1

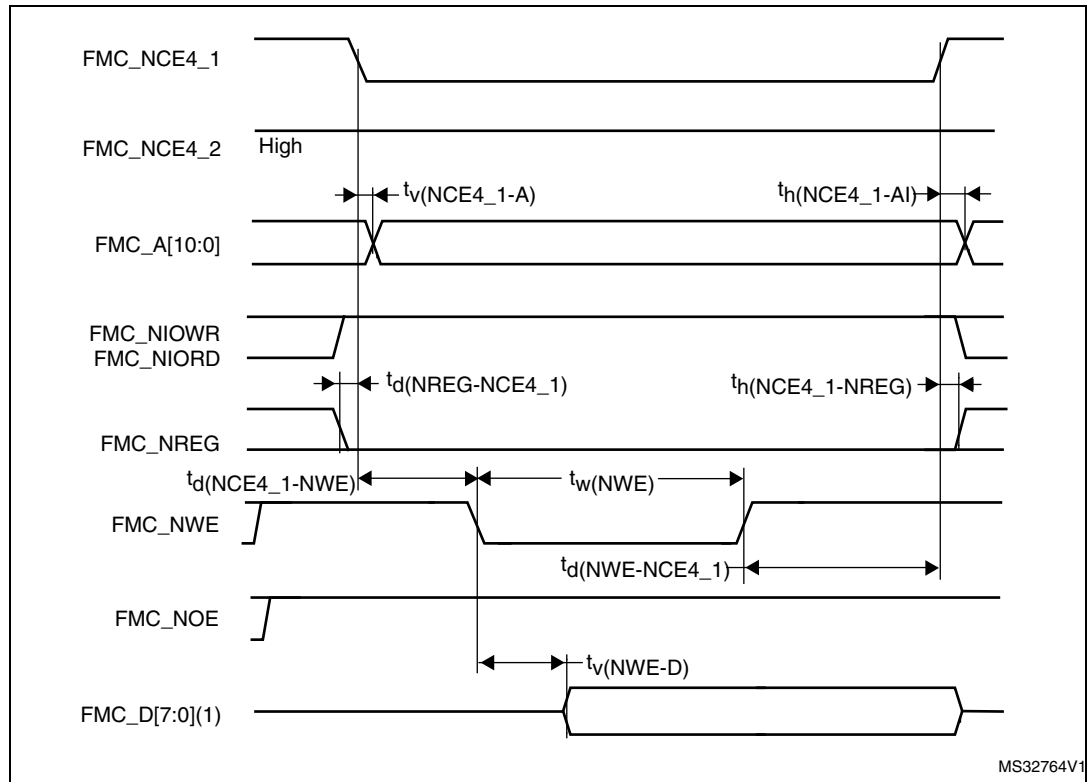
Table 92. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_v(NWE_NE)$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_w(NWE)$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_h(NE_NWE)$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	ns
$t_v(A_NE)$	FMC_NEx low to FMC_A valid	-	0	ns
$t_v(NADV_NE)$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_w(NADV)$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	ns
$t_h(AD_NADV)$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 2$	-	ns
$t_h(A_NWE)$	Address hold time after FMC_NWE high	T_{HCLK}	-	ns
$t_h(BL_NWE)$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_v(BL_NE)$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_v(Data_NADV)$	FMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	ns
$t_h(Data_NWE)$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Figure 66. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Figure 67. PC Card/CompactFlash controller waveforms for I/O space read access

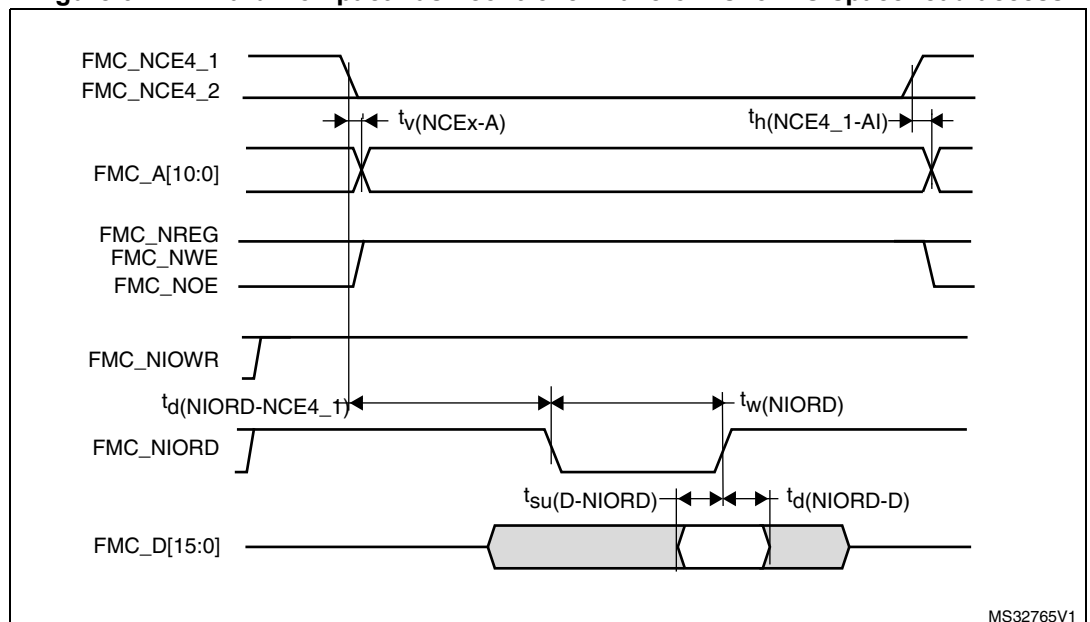


Table 108. Dynamic characteristics: SD / MMC characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode		0		48	MHz
-	SDIO_CLK/fPCLK2 frequency ratio		-	-	8/3	-
t _{W(CKL)}	Clock low time	fpp =48 MHz	8.5	9	-	ns
t _{W(CKH)}	Clock high time	fpp =48 MHz	8.3	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t _{ISU}	Input setup time HS	fpp =48 MHz	3.5	-	-	ns
t _{IH}	Input hold time HS	fpp =48 MHz	0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t _{OV}	Output valid time HS	fpp =48 MHz	-	4.5	7	ns
t _{OH}	Output hold time HS	fpp =48 MHz	3	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t _{ISUD}	Input setup time SD	fpp =24 MHz	1.5	-	-	ns
t _{IHD}	Input hold time SD	fpp =24 MHz	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t _{OVD}	Output valid default time SD	fpp =24 MHz	-	4.5	6.5	ns
t _{OHD}	Output hold default time SD	fpp =24 MHz	3.5	-	-	

1. Guaranteed by characterization results.

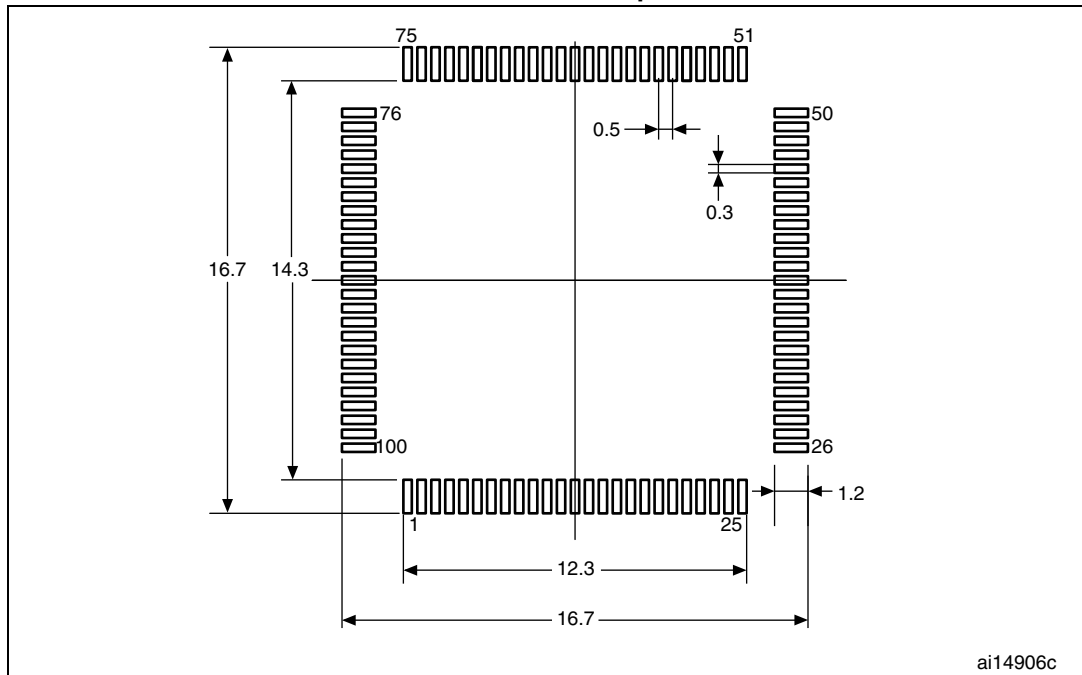
2. $V_{DD} = 2.7$ to 3.6 V.

6.3.30 RTC characteristics

Table 109. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	$f_{PCLK1}/RTCCLK$ frequency ratio	Any read/write operation from/to an RTC register	4	-

Figure 81. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 112. WLCSP143 recommended PCB design rules (0.4 mm pitch)

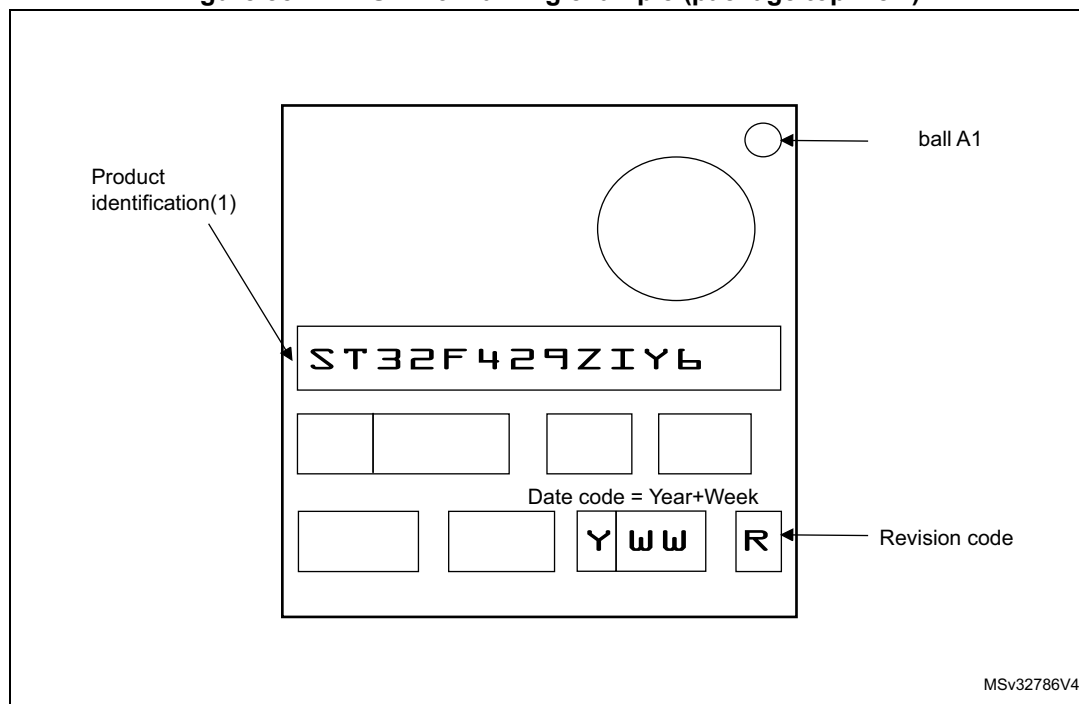
Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Device marking for WLCSP143

The following figure gives an example of topside marking orientation versus ball A 1 identifier location.

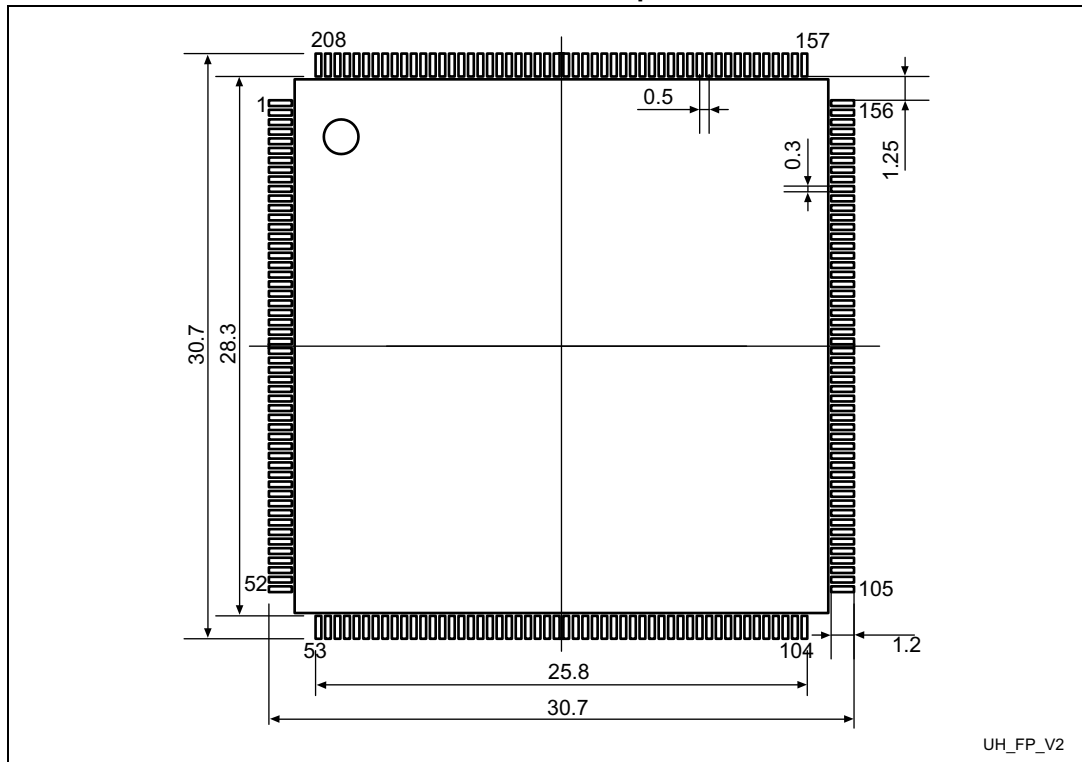
Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 85. WLCSP143 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Figure 93. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package
recommended footprint**



1. Dimensions are expressed in millimeters.

7.9 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 121. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient WLCSP143	31.2	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA169 - 7 × 7mm / 0.5 mm pitch	52	
	Thermal resistance junction-ambient UFBGA176 - 10 × 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.