Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429igt6

communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison(1)

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

1. X = feature supported.

3.25 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
22	33	J4	R1	39	L10	42	R1	V_{DDA}	S	-	-	-	-
23	34	J5	N3	40	K9	43	N3	PA0-WKUP (PA0)	I/O	FT	(6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII_CRS, EVENTOUT	ADC123_IN0/WKUP (5)
24	35	K1	N2	41	K8	44	N2	PA1	I/O	FT	(5)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, EVENTOUT	ADC123_IN1
25	36	K2	P2	42	L9	45	P2	PA2	I/O	FT	(5)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, ETH_MDIO, EVENTOUT	ADC123_IN2
-	-	L2	F4	43	-	46	K4	PH2	I/O	FT	-	ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	L1	G4	44	-	47	J4	PH3	I/O	FT	-	ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	M2	H4	45	-	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	L3	J4	46	-	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
26	37	K3	R2	47	M11	50	R2	PA3	I/O	FT	(5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
27	38	-	-		-	51	K6	V_{SS}	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
96	140	C4	B4	168	B9	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	B4	A4	169	B10	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_RX, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A4	A3	170	A10	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	F5	D5	-	-	202	F6	V_{SS}	S		-		-
-	143	C3	C6	171	A11	203	E5	PDR_ON	S		-		-
100	144	K6	C5	172	D7	204	E7	V_{DD}	S		-		-
-	-	B3	D4	173	-	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A3	C4	174	-	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A2	C3	175	-	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	C2	176	-	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. Function availability depends on the chosen device.
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port H	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	-
Port H	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENTOUT
Port H	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENTOUT
Port H	PH10	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENTOUT
Port H	PH11	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVENTOUT
Port H	PH12	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENTOUT
Port H	PH13	-	-	-	TIM8_CH1N	-	-	-	-	-	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT
Port H	PH14	-	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENTOUT
Port H	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENTOUT
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
Port I	PI1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
Port I	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
Port I	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD							FMC_D27	DCMI_D10		EVENTOUT
Port I	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
Port I	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
Port I	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4001 6C00- 0x4001 FFFF	Reserved
APB2	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 5C00 - 0x4001 67FF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 23: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 18: Limitations depending on the operating power supply range*).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 120$ MHz
  - Scale 2 for 120 MHz < $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 4 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Figure 25. Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM OFF)

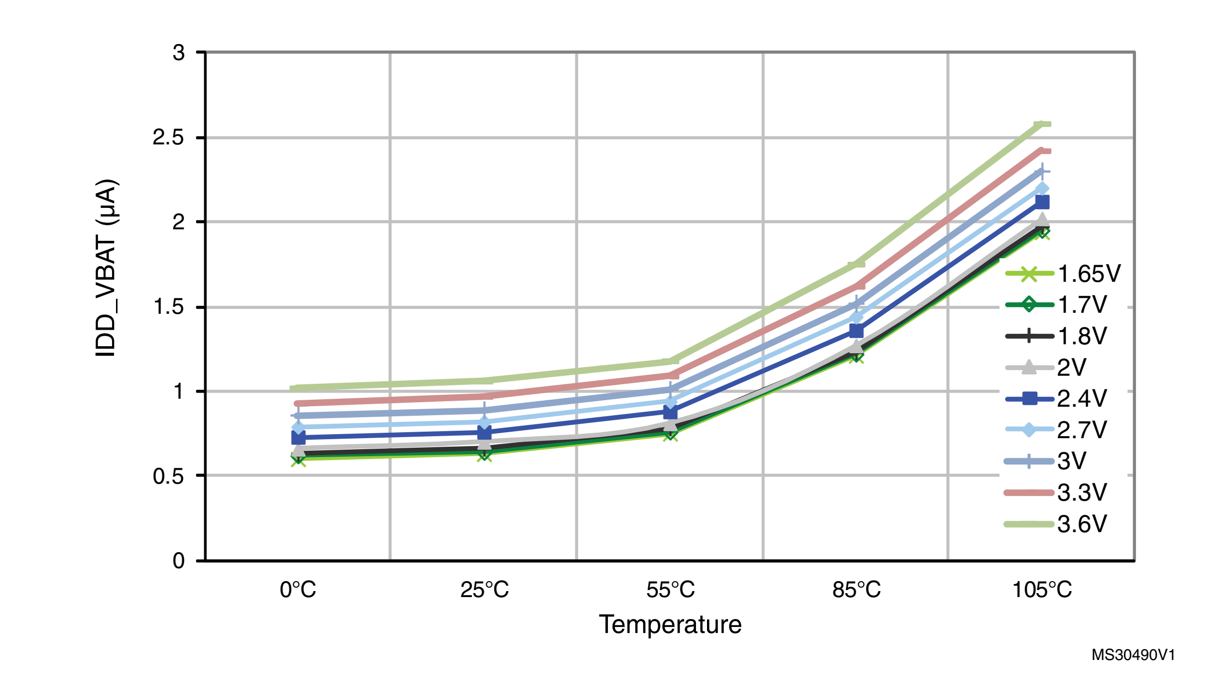


Figure 26. Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM ON)

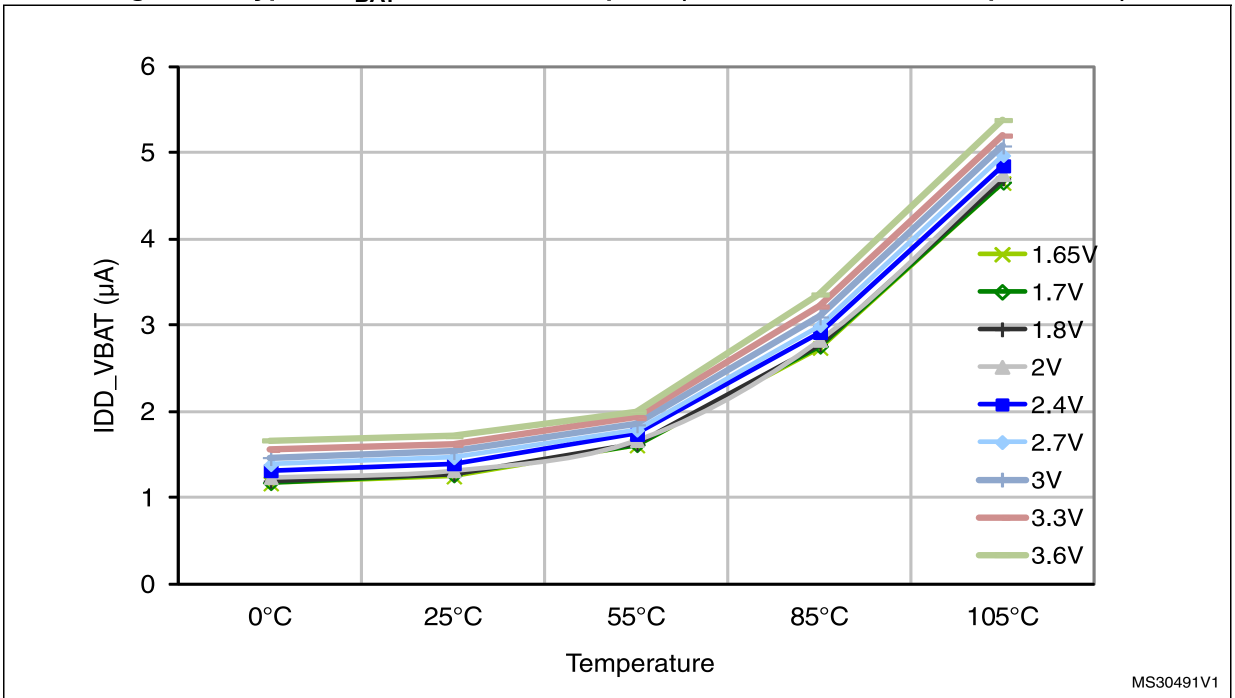


Table 35. Peripheral current consumption (continued)

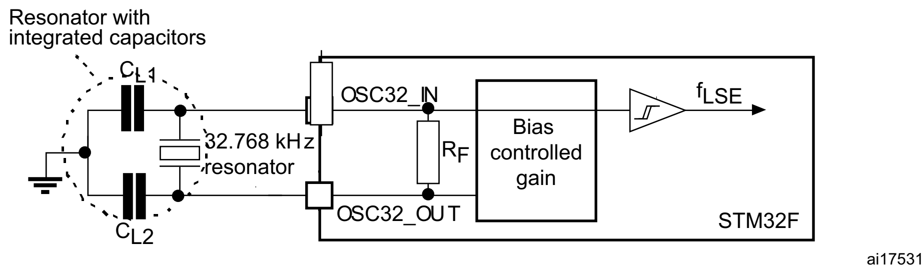
Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
AHB2 (up to 180 MHz)	OTG_FS	25.67	26.67	23.58	µA/MHz
	DCMI	3.72	3.40	3.00	
	RNG	2.28	2.36	2.17	
AHB3 (up to 180 MHz)	FMC	21.39	19.79	17.50	µA/MHz
Bus matrix(2)		14.06	13.19	11.75	µA/MHz
APB1 (up to 45 MHz)	TIM2	17.56	16.42	14.47	µA/MHz
	TIM3	14.22	13.36	11.80	
	TIM4	14.89	13.64	12.13	
	TIM5	17.33	16.42	14.47	
	TIM6	2.89	2.53	2.47	
	TIM7	3.11	2.81	2.47	
	TIM12	7.33	6.97	6.13	
	TIM13	4.89	4.47	4.13	
	TIM14	5.56	5.31	4.80	
	PWR	11.11	10.31	9.13	
	USART2	4.22	3.92	3.47	
	USART3	4.44	4.19	3.80	
	UART4	4.00	3.92	3.47	
	UART5	4.00	3.92	3.47	
	UART7	4.00	3.92	3.47	
	UART8	3.78	3.92	3.47	
	I2C1	4.00	3.92	3.47	
	I2C2	4.00	3.92	3.47	
	I2C3	4.00	3.92	3.47	
	SPI2(3)	3.11	3.08	2.80	
	SPI3(3)	3.56	3.36	3.13	
	I2S2	2.89	2.81	2.47	
	I2S3	3.33	3.08	2.80	
	CAN1	6.89	6.42	5.80	
	CAN2	6.67	6.14	5.47	
	DAC(4)	2.89	2.25	2.13	
	WWDG	0.89	0.86	0.80	

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 90 MHz)	SDIO	8.11	8.75	7.83	µA/MHz
	TIM1	17.11	15.97	14.17	
	TIM8	17.33	16.11	14.33	
	TIM9	7.22	6.67	6.00	
	TIM10	4.56	4.31	3.83	
	TIM11	4.78	4.44	4.00	
	ADC1(5)	4.67	4.31	3.83	
	ADC2(5)	4.78	4.44	4.00	
	ADC3(5)	4.56	4.17	3.67	
	SPI1	1.44	1.39	1.17	
	USART1	4.00	3.75	3.33	
	USART6	4.00	3.75	3.33	
	SPI4	1.44	1.39	1.17	
	SPI5	1.44	1.39	1.17	
	SPI6	1.44	1.39	1.17	
	SYSCFG	0.78	0.69	0.67	
	LCD_TFT	39.89	37.22	33.17	
	SAI1	3.78	3.47	3.17	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Figure 30. Typical application with a 32.768 kHz crystal



6.3.10 Internal clock source characteristics

The parameters given in *Table 41* and *Table 42* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics [(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user-trimming step [(2)]	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C[(3)]	– 8	-	4.5	%
		T_A = –10 to 85 °C[(3)]	– 4	-	4	%
		T_A = 25 °C[(4)]	– 1	-	1	%
$t_{su(HSI)}$[(2)]	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$[(2)]	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

6.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESD S5.3.1 standards.

Table 53. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD S5.3.1, LQFP100/144/176, UFBGA169/176, TFBGA176 and WLCSP143 packages	C3	250	
		T_A = +25 °C conforming to ANSI/ESD S5.3.1, LQFP208 package	C3	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 54. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

Table 61. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 62* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 62. SPI dynamic characteristics(1)

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="5">f_{SCK}
$1/t_{c(SCK)}$</td><td rowspan="5">SPI clock frequency</td><td colspan="2">Master mode, SPI1/4/5/6,
2.7 V≤V_{DD}≤3.6 V</td><td rowspan="3">-</td><td rowspan="3">-</td><td>45</td><td rowspan="5">MHz</td></tr>
<tr><td rowspan="2">Slave mode,
SPI1/4/5/6,
2.7 V≤V_{DD}≤3.6 V</td><td>Receiver</td><td>45</td></tr>
<tr><td>Transmitter/
full-duplex</td><td>38(2)</td></tr>
<tr><td colspan="2">Master mode, SPI1/2/3/4/5/6,
1.7 V≤V_{DD}≤3.6 V</td><td rowspan="2">-</td><td rowspan="2">-</td><td>22.5</td></tr>
<tr><td colspan="2">Slave mode, SPI1/2/3/4/5/6,
1.7 V≤V_{DD}≤3.6 V</td><td>22.5</td></tr>
<tr><td>Duty(SCK)</td><td>Duty cycle of SPI clock frequency</td><td colspan="2">Slave mode</td><td>30</td><td>50</td><td>70</td><td>%</td></tr>
</table>

6.3.25 DAC electrical characteristics

Table 85. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	-	1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	-	1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	-	0	-	0	V	-
R_{LOAD}(2)	Resistive load	DAC output buffer ON, R_{LOAD} connected to V_{SSA}	5	-	-	kΩ	-
R_{LOAD}(2)	Resistive load	DAC output buffer ON, R_{LOAD} connected to V_{DDA}	25			kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	-	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	-	V_{DDA} – 0.2	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	-	V_{REF+} – 1LSB	V	It gives the maximum output excursion of the DAC.
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	-	50	75	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Table 99. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
tw(NIOWR)	FMC_NIOWR low width	$8T_{HCLK} - 0.5$	-	ns
tv(NIOWR-D)	FMC_NIOWR low to FMC_D[15:0] valid	-	0	ns
th(NIOWR-D)	FMC_NIOWR high to FMC_D[15:0] invalid	$9T_{HCLK} - 2$	-	ns
td(NCE4_1-NIOWR)	FMC_NCE4_1 low to FMC_NIOWR valid	-	$5T_{HCLK}$	ns
th(NCEx-NIOWR)	FMC_NCEx high to FMC_NIOWR invalid	$5T_{HCLK}$	-	ns
td(NIORD-NCEx)	FMC_NCEx low to FMC_NIORD valid	-	$5T_{HCLK}$	ns
th(NCEx-NIORD)	FMC_NCEx high to FMC_NIORD) valid	$6T_{HCLK}+2$	-	ns
tw(NIORD)	FMC_NIORD low width	$8T_{HCLK} - 0.5$	$8T_{HCLK}+0.5$	ns
tsu(D-NIORD)	FMC_D[15:0] valid before FMC_NIORD high	T_{HCLK}	-	ns
td(NIORD-D)	FMC_D[15:0] valid after FMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

NAND controller waveforms and timings

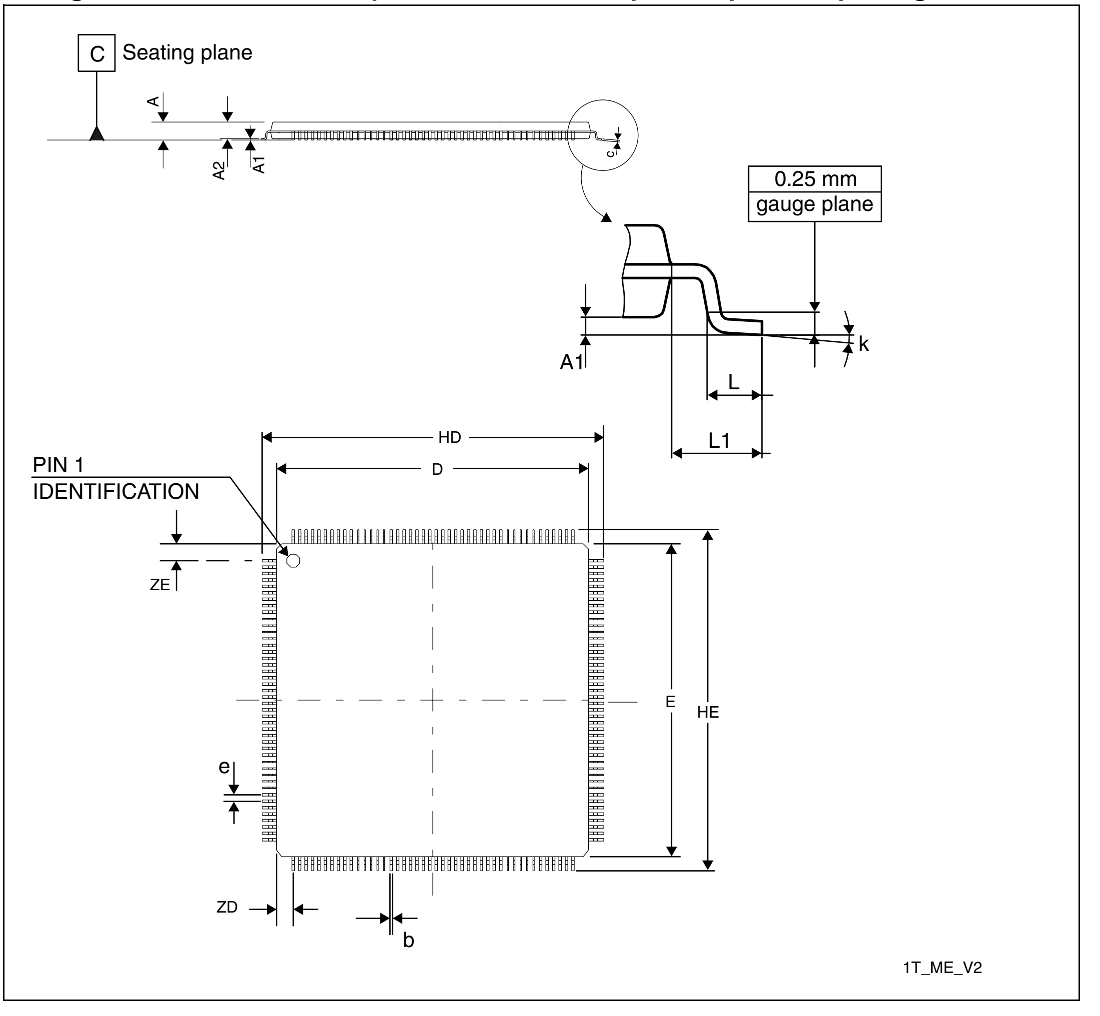
Figure 69 through *Figure 72* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

7.4 LQFP176 package information

Figure 89. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
HD	25.900	-	26.100	1.0197	-	1.0276

Table 116. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 96. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint

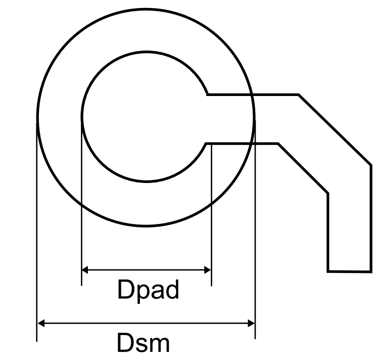


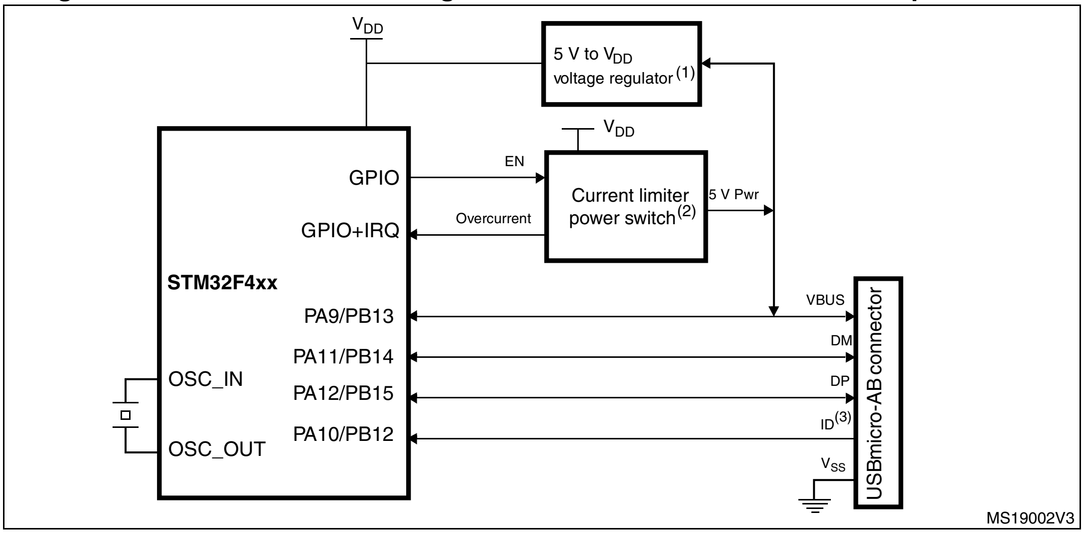
Table 117. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

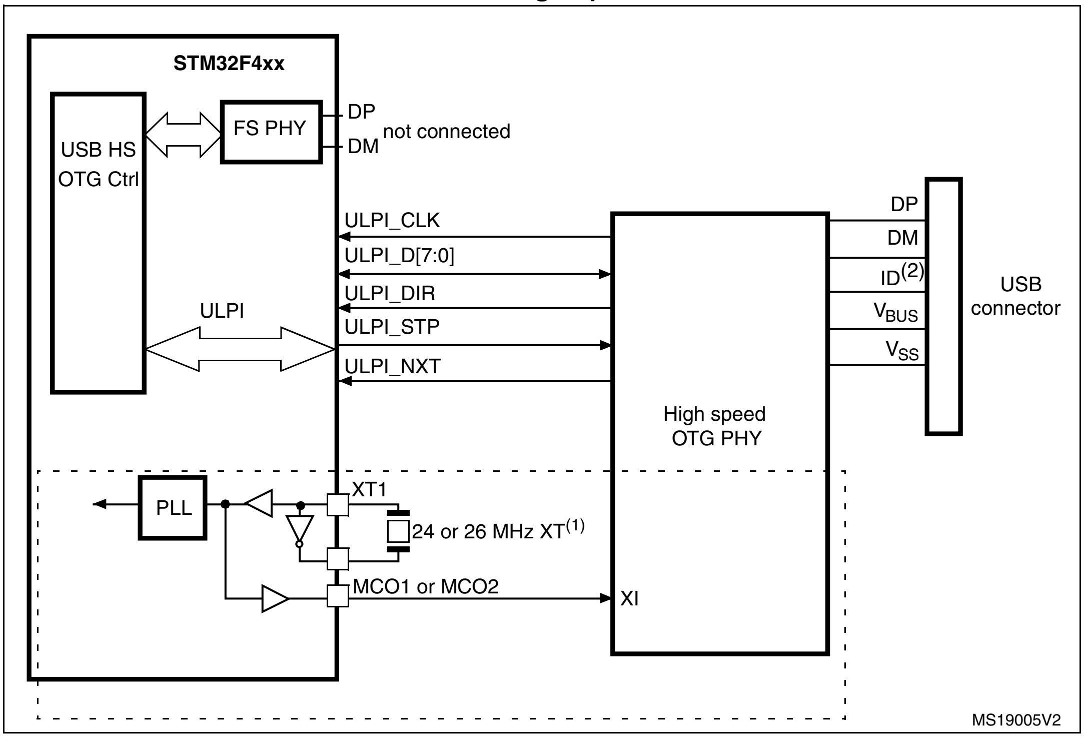
Figure 105. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

B.2 USB OTG high speed (HS) interface solutions

Figure 106. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F42x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

Table 124. Document revision history

Date	Revision	Changes
17-Sep-2015	6	Updated notes related to the minimum and maximum values guaranteed by design, characterization or test in production. Updated $I_{DD\_STOP\_UDM}$ in *Table 27: Typical and maximum current consumptions in Stop mode*. Removed note related to tests in production in *Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM* and *Table 26: Typical and maximum current consumption in Sleep mode*. Updated *Table 41: HSI oscillator characteristics*. *Figure 31* renamed *ACCHSI accuracy versus temperature* and updated. Updated *Figure 38: SPI timing diagram - slave mode and CPHA = 0*. Updated *Section : Ethernet characteristics*. Updated *Table 43: Main PLL characteristics*, *Table 44: PLLI2S (audio PLL) characteristics* and *Table 45: PLLISAI (audio and LCD-TFT PLL) characteristics*. Removed note 1 in *Table 75: ADC static accuracy at fADC = 18 MHz*, *Table 76: ADC static accuracy at fADC = 30 MHz* and *Table 77: ADC static accuracy at fADC = 36 MHz*. Updated $t_{d(SDCLKL\_Data)}$ and $t_{h(SDCLKL\_Data)}$ in *Table 104: SDRAM write timings*. Added *Figure 96: UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint* and *Table 117: UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 99: UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint* and *Table 119: UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)*.
30-Nov-2015	7	Updated $\|V_{SSX} - V_{SS}\|$ in *Table 14: Voltage characteristics* to add V_{REF-}. Updated $t_{d(TXEN)}$ and $t_{d(TXD)}$ minimum value in *Table 72: Dynamics characteristics: Ethernet MAC signals for RMII* and *Table 73: Dynamics characteristics: Ethernet MAC signals for MII*. Added V_{REF-} in *Table 74: ADC characteristics*. Added A1 minimum and maximum values in *Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data*. Updated *Figure 86: LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline*. Updated *Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline* and *Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data*. Updated *Figure 101: TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline* and *Table 120: TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data*.