E·XFL

STMicroelectronics - STM32F429IIT6E Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429iit6e

reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

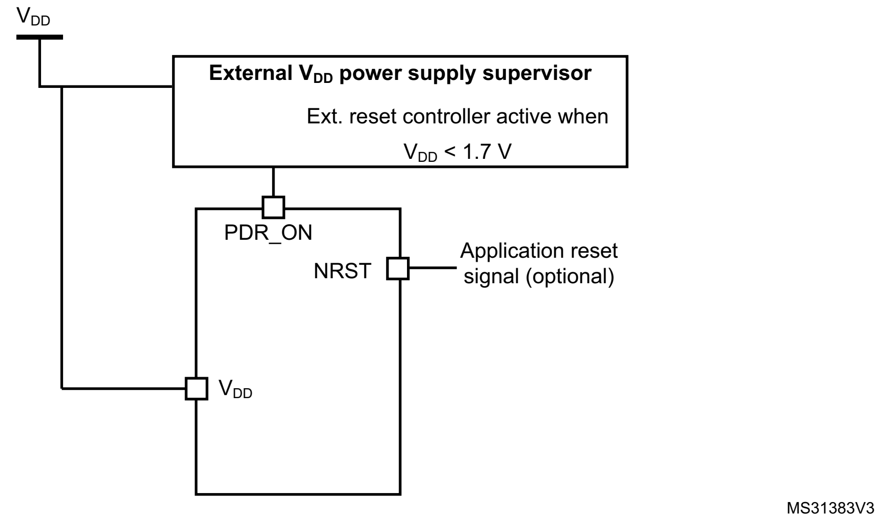
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 6: Power supply supervisor interconnection with internal reset OFF*.

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 7*).

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal.

The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.

- In Stop modes

  The MR can be configured in two ways during stop mode:

  MR operates in normal mode (default mode of MR in stop mode)

  MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:
  - LPR operates in normal mode (default mode when LPR is ON)
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 22: Power supply scheme* and *Table 19: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

3.18.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Table 17: General operating conditions*.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 22: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	21	NC (2)	L2	27	G8	30	L2	PF9	I/O	FT	(5)	SPI5_MOSI, SAI1_FS_B, TIM14_CH1, FMC_CD, EVENTOUT	ADC3_IN7
-	22	H1	L1	28	G9	31	L1	PF10	I/O	FT	(5)	FMC_INTR, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
12	23	G2	G1	29	J11	32	G1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN(5)
13	24	G1	H1	30	H10	33	H1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT (5)
14	25	H2	J1	31	H9	34	J1	NRST	I/O	RST	-	-	-
15	26	G6	M2	32	H8	35	M2	PC0	I/O	FT	(5)	OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC123_IN10
16	27	H5	M3	33	K11	36	M3	PC1	I/O	FT	(5)	ETH_MDC, EVENTOUT	ADC123_IN11
17	28	H6	M4	34	J10	37	M4	PC2	I/O	FT	(5)	SPI2_MISO, I2S2ext_SD, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_IN12
18	29	H7	M5	35	J9	38	L4	PC3	I/O	FT	(5)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC123_IN13
19	30	-	-	36	G7	39	J5	V_{DD}	S	-	-	-	-
-	-	-	-	-	-	-	J6	V_{SS}	S	-	-	-	-
20	31	J1	M1	37	K10	40	M1	V_{SSA}	S	-	-	-	-
-	-	J2	N1	-	-	-	N1	V_{REF-}	S	-	-	-	-
21	32	J3	P1	38	L11	41	P1	V_{REF+}	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
22	33	J4	R1	39	L10	42	R1	V_{DDA}	S	-	-	-	-
23	34	J5	N3	40	K9	43	N3	PA0-WKUP (PA0)	I/O	FT	(6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII_CRS, EVENTOUT	ADC123_ IN0/WKUP (5)
24	35	K1	N2	41	K8	44	N2	PA1	I/O	FT	(5)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, EVENTOUT	ADC123_ IN1
25	36	K2	P2	42	L9	45	P2	PA2	I/O	FT	(5)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, ETH_MDIO, EVENTOUT	ADC123_ IN2
-	-	L2	F4	43	-	46	K4	PH2	I/O	FT	-	ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	L1	G4	44	-	47	J4	PH3	I/O	FT	-	ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	M2	H4	45	-	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	L3	J4	46	-	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
26	37	K3	R2	47	M11	50	R2	PA3	I/O	FT	(5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_ IN3
27	38	-	-		-	51	K6	V_{SS}	S	-	-	-	-

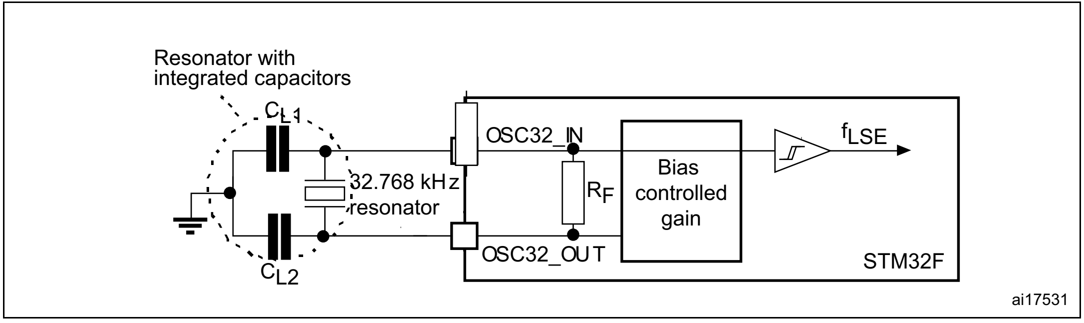
Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	125	C7	B10	153	C6	179	C8	PG10	I/O	FT	-	LCD_G3, FMC_NCE4_1/FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	126	B7	B9	154	B6	180	B8	PG11	I/O	FT	-	ETH_MII_TX_EN/ETH_RMII_TX_EN, FMC_NCE4_2, DCMI_D3, LCD_B3, EVENTOUT	-
-	127	A7	B8	155	A6	181	C7	PG12	I/O	FT	-	SPI6_MISO, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT	-
-	128	NC (2)	A8	156	D6	182	B3	PG13	I/O	FT	-	SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, EVENTOUT	-
-	129	NC (2)	A7	157	F6	183	A4	PG14	I/O	FT	-	SPI6_MOSI, USART6_TX, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, EVENTOUT	-
-	130	D7	D7	158	-	184	F7	V_{SS}	S		-	-	-
-	131	L6	C7	159	E6	185	E8	V_{DD}	S		-	-	-
-	-	-	-	-	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	-	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	-	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	-	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	-	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	132	C6	B7	160	A7	191	B7	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	**TIM1/2**	**TIM3/4/5**	**TIM8/9/10/11**	**I2C1/2/3**	**SPI1/2/3/4/5/6**	**SPI2/3/SAI1**	**SPI3/USART1/2/3**	**USART6/UART4/5/7/8**	**CAN1/2/TIM12/13/14/LCD**	**OTG2_HS/OTG1_FS**	**ETH**	**FMC/SDIO/OTG2_FS**	**DCMI**	**LCD**	**SYS**
Port D	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1/FMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	FMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	FMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	UART8_Rx	-	-	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	-	-	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	-	-	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	-	-	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	-	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT

Figure 30. Typical application with a 32.768 kHz crystal



6.3.10 Internal clock source characteristics

The parameters given in *Table 41* and *Table 42* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

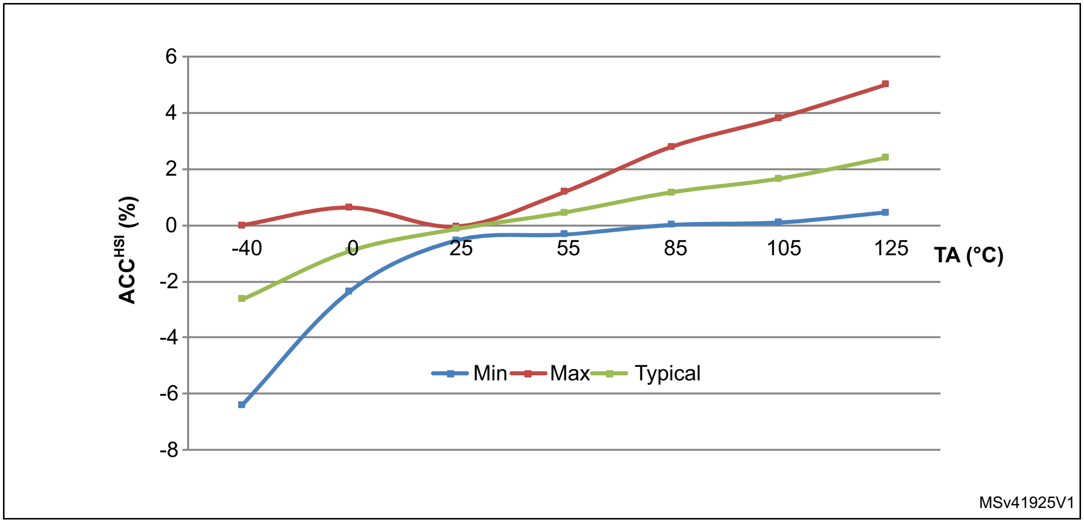
High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user-trimming step (2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	– 8	-	4.5	%
		T_A = –10 to 85 °C(3)	– 4	-	4	%
		T_A = 25 °C(4)	– 1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 31. ACCHSI accuracy versus temperature



1. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Table 44. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$[4]	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$[4]	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock[1]			0.95[2]	1	2.10	MHz
f_{PLLSAI_OUT}	PLLSAI multiplier output clock			-	-	216	MHz
f_{VCO_OUT}	PLLSAI VCO output			100	-	432	MHz
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter[3]	Main SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLSAI)}$[4]	PLLSAI power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}$[4]	PLLSAI power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 48. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{BE}	Bank erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 49. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
t_{BE}	Bank erase time		-	6.9	-	s
V_{prog}	Programming voltage		2.7	-	3.6	V
V_{PP}	V_{PP} voltage range		7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin		10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied		-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

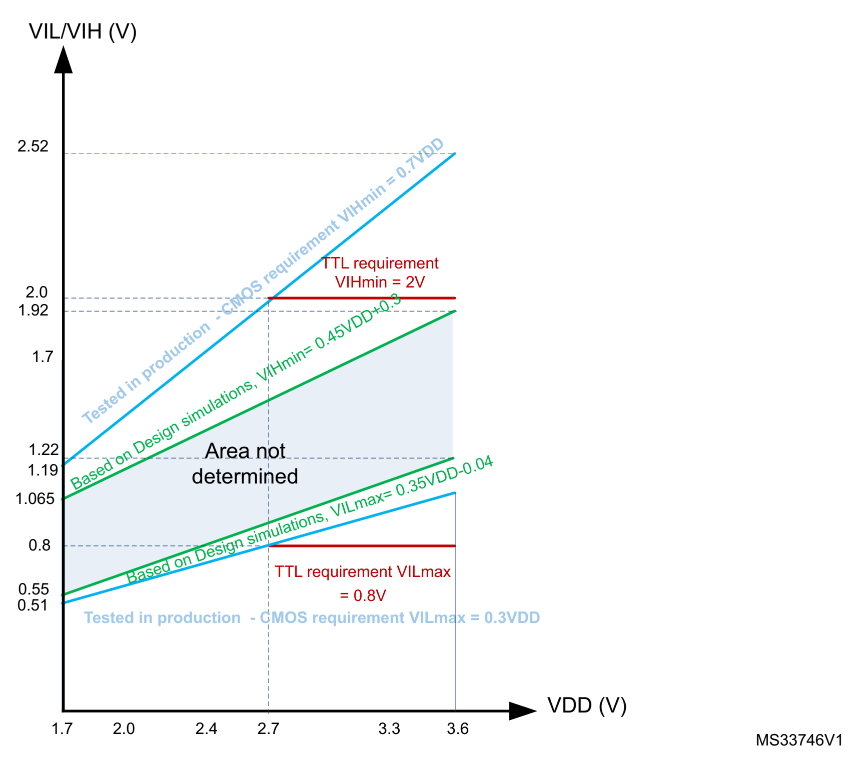
Table 56. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor[6]	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor[7]	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
C_{IO}[8]	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 55: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 55: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 35*.

Figure 35. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14, PC15 and PI8 which can sink or source up to ±3mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 15*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 15*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V $\leq V_{DD} \leq$ 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD} − 0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V $\leq V_{DD} \leq$ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V $\leq V_{DD} \leq$ 3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V $\leq V_{DD} \leq$ 3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V $\leq V_{DD} \leq$ 3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 36* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 58. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DD} \geq 2.7$ V	-	-	4	MHz
			C_L = 50 pF, $V_{DD} \geq 1.7$ V	-	-	2	
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	8	
			C_L = 10 pF, $V_{DD} \geq 1.8$ V	-	-	4	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DD} \geq 2.7$ V	-	-	25	MHz
			C_L = 50 pF, $V_{DD} \geq 1.8$ V	-	-	12.5	
			C_L = 50 pF, $V_{DD} \geq 1.7$ V	-	-	10	
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	50	
			C_L = 10 pF, $V_{DD} \geq 1.8$ V	-	-	20	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, $V_{DD} \geq 2.7$ V	-	-	10	ns
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	6	
			C_L = 50 pF, $V_{DD} \geq 1.7$ V	-	-	20	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, $V_{DD} \geq 2.7$ V	-	-	50(4)	MHz
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	100(4)	
			C_L = 40 pF, $V_{DD} \geq 1.7$ V	-	-	25	
			C_L = 10 pF, $V_{DD} \geq 1.8$ V	-	-	50	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, $V_{DD} \geq 2.7$ V	-	-	6	ns
			C_L = 10 pF, $V_{DD} \geq 2.7$ V	-	-	4	
			C_L = 40 pF, $V_{DD} \geq 1.7$ V	-	-	10	
			C_L = 10 pF, $V_{DD} \geq 1.7$ V	-	-	6	

Table 69. USB HS clock timing parameters(1)

Symbol	Parameter		Min	Typ	Max	Unit
	f_{HCLK} value to guarantee proper operation of USB HS interface		30	-	-	MHz
F_{START_8BIT}	Frequency (first transition)	8-bit ±10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm		59.97	60	60.03	MHz
D_{START_8BIT}	Duty cycle (first transition)	8-bit ±10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm		49.975	50	50.025	%
t_{STEADY}	Time to reach the steady state frequency and duty cycle after the first transition		-	-	1.4	ms
t_{START_DEV}	Clock startup time after the de-assertion of SuspendM	Peripheral	-	-	5.6	ms
t_{START_HOST}		Host	-	-	-	
t_{PREP}	PHY preparation time after the first transition of the input clock		-	-	-	µs

1. Guaranteed by design.

Figure 46. ULPI timing diagram

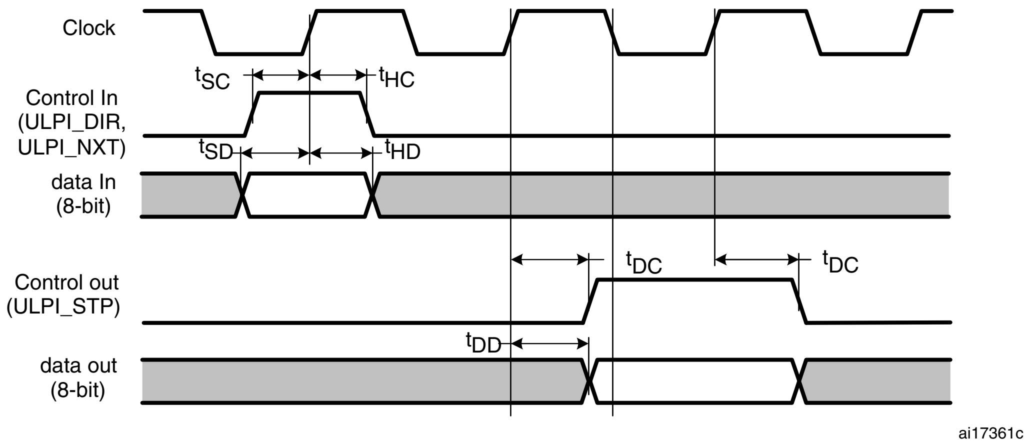


Table 74. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S[2]	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}[2]	ADC V_{REF} DC current consumption in conversion mode		-	300	500	µA
I_{VDDA}[2]	ADC V_{DDA} DC current consumption in conversion mode		-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 74*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k-0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

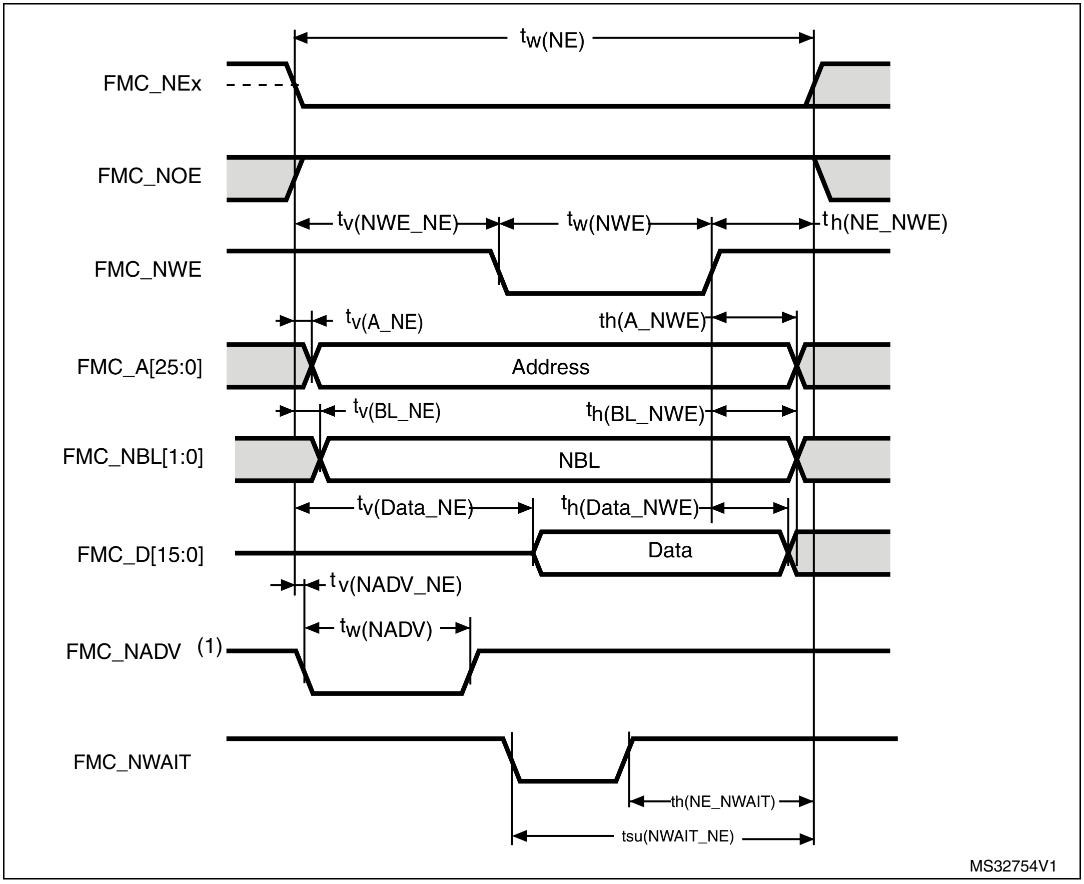
The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 75. ADC static accuracy at f_{ADC} = 18 MHz

Symbol	Parameter	Test conditions	Typ	Max[1]	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Guaranteed by characterization results.

Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

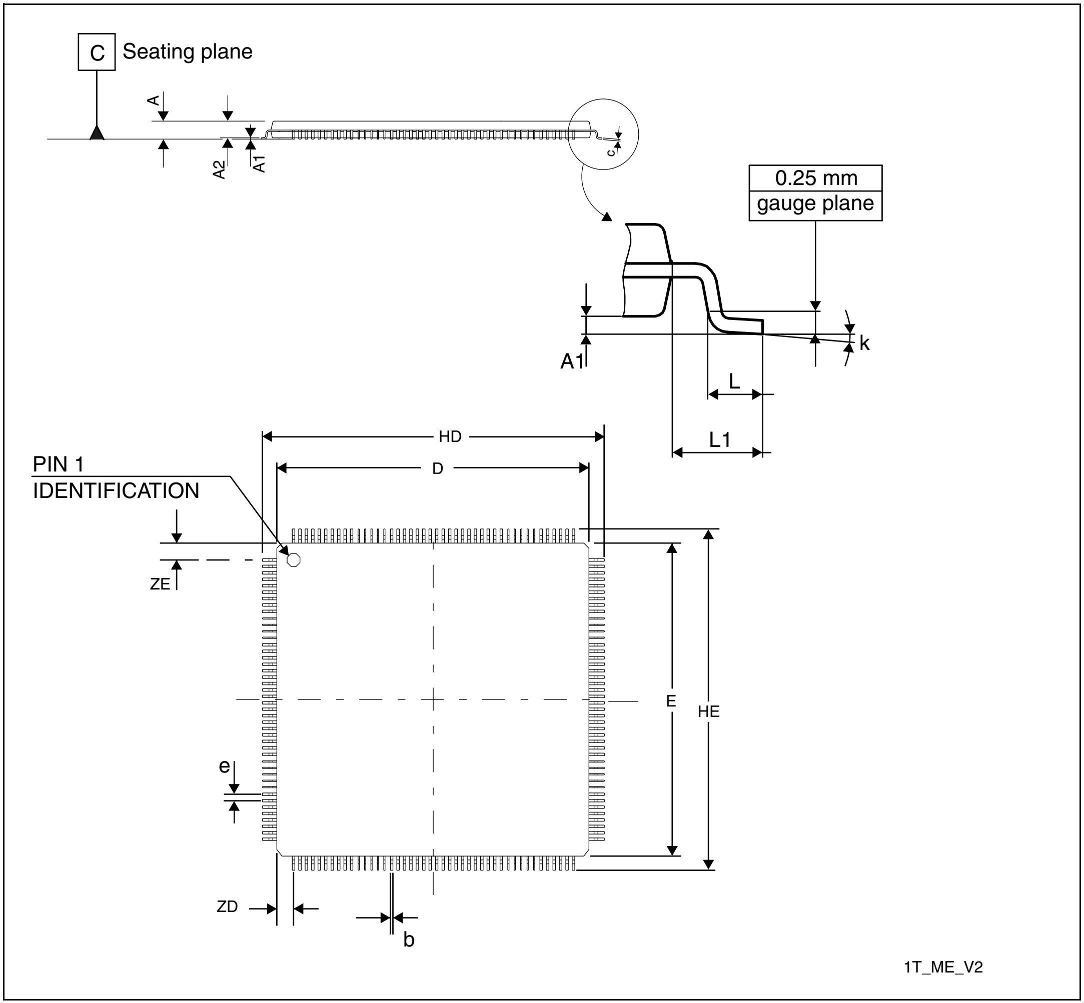
Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	$T_{HCLK}+ 0.5$	ns
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} +1.5$	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+ 2$	ns
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	ns
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+ 0.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

7.4 LQFP176 package information

Figure 89. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
HD	25.900	-	26.100	1.0197	-	1.0276

Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L[2]	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Table 116. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 96. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint

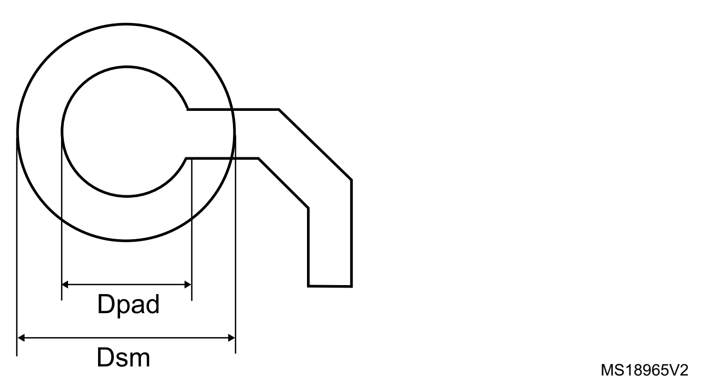


Table 117. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: *Non-solder mask defined (NSMD) pads are recommended.*

4 to 6 mils solder paste screen printing process.