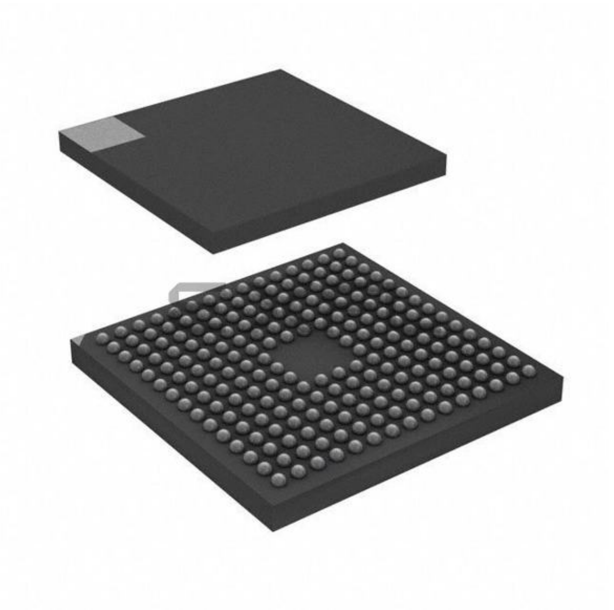
STMicroelectronics - STM32F429NIH6 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429nih6

3 Functional overview

3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F42x family is compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F42x family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

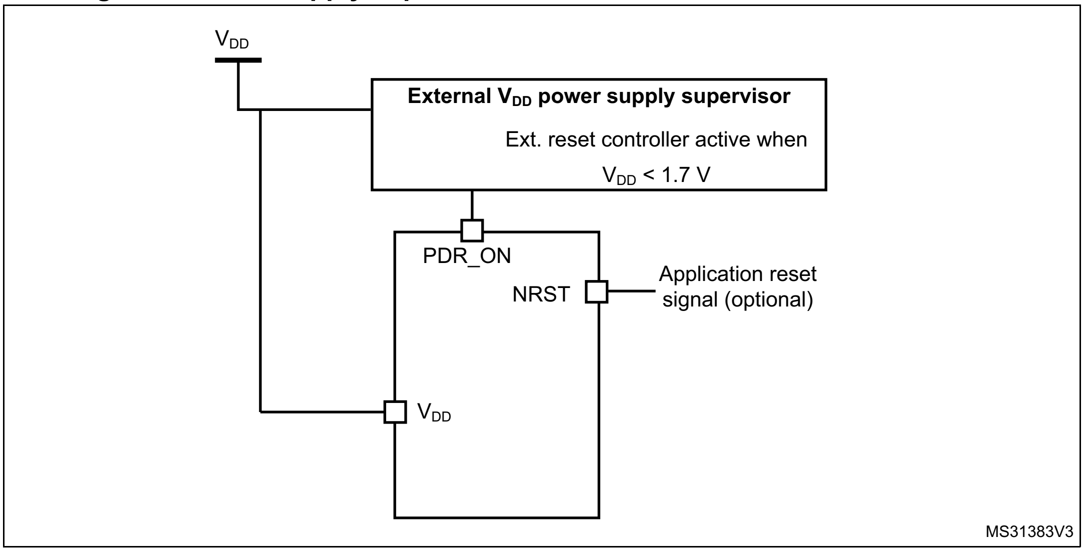
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 6: Power supply supervisor interconnection with internal reset OFF*.

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 7*).

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal.

Figure 18. STM32F42x TFBGA216 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE4	PE3	PE2	PG14	PE1	PE0	PB8	PB5	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE5	PE6	PG13	PB9	PB7	PB6	PG15	PG11	PJ13	PJ12	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI8	PI4	PK7	PK6	PK5	PG12	PG10	PJ14	PD5	PD3	PD1	PI3	PI2	PA11
D	PC13	PF0	PI5	PI7	PI10	PI6	PK4	PK3	PG9	PJ15	PD4	PD2	PH15	PI1	PA10
E	PC14	PF1	PI12	PI9	PDR_ON	BOOT0	VDD	VDD	VDD	VDD	VCAP2	PH13	PH14	PI0	PA9
F	PC15	VSS	PI11	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PK1	PK2	PC9	PA8
G	PH0	PF2	PI13	PI15	VDD	VSS				VSS	VDD	PJ11	PK0	PC8	PC7
H	PH1	PF3	PI14	PH4	VDD	VSS				VSS	VDD	PJ8	PJ10	PG8	PC6
J	NRST	PF4	PH5	PH3	VDD	VSS				VSS	VDD	PJ7	PJ9	PG7	PG6
K	PF7	PF6	PF5	PH2	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PJ6	PD15	PB13	PD10
L	PF10	PF9	PF8	PC3	BYPASS-REG	VSS	VDD	VDD	VDD	VDD	VCAP1	PD14	PB12	PD9	PD8
M	VSSA	PC0	PC1	PC2	PB2	PF12	PG1	PF15	PJ4	PD12	PD13	PG3	PG2	PJ5	PH12
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	PJ3	PE8	PD11	PG5	PG4	PH7	PH9	PH11
P	VREF+	PA2	PA6	PA5	PC5	PF14	PJ2	PF11	PE9	PE11	PE14	PB10	PH6	PH8	PH10
R	VDDA	PA3	PA7	PB1	PB0	PJ0	PJ1	PE7	PE10	PE12	PE15	PE13	PB11	PB14	PB15

MS30423V2

1. The above figure shows the package top view.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	21	NC (2)	L2	27	G8	30	L2	PF9	I/O	FT	(5)	SPI5_MOSI, SAI1_FS_B, TIM14_CH1, FMC_CD, EVENTOUT	ADC3_IN7
-	22	H1	L1	28	G9	31	L1	PF10	I/O	FT	(5)	FMC_INTR, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
12	23	G2	G1	29	J11	32	G1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN(5)
13	24	G1	H1	30	H10	33	H1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT (5)
14	25	H2	J1	31	H9	34	J1	NRST	I/O	RST	-	-	-
15	26	G6	M2	32	H8	35	M2	PC0	I/O	FT	(5)	OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC123_IN10
16	27	H5	M3	33	K11	36	M3	PC1	I/O	FT	(5)	ETH_MDC, EVENTOUT	ADC123_IN11
17	28	H6	M4	34	J10	37	M4	PC2	I/O	FT	(5)	SPI2_MISO, I2S2ext_SD, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_IN12
18	29	H7	M5	35	J9	38	L4	PC3	I/O	FT	(5)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC123_IN13
19	30	-	-	36	G7	39	J5	V_{DD}	S	-	-	-	-
-	-	-	-	-	-	-	J6	V_{SS}	S	-	-	-	-
20	31	J1	M1	37	K10	40	M1	V_{SSA}	S	-	-	-	-
-	-	J2	N1	-	-	-	N1	V_{REF-}	S	-	-	-	-
21	32	J3	P1	38	L11	41	P1	V_{REF+}	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
58	80	H10	N14	99	K2	111	N10	PD11	I/O	FT	-	USART3_CTS, FMC_A16, EVENTOUT	-
59	81	J13	N13	100	H6	112	M10	PD12	I/O	FT	-	TIM4_CH1, USART3_RTS, FMC_A17, EVENTOUT	-
60	82	K12	M15	101	H5	113	M11	PD13	I/O	FT	-	TIM4_CH2, FMC_A18, EVENTOUT	-
-	83	-	-	102	-	114	J10	V_{SS}	S		-	-	-
-	84	F7	J13	103	L1	115	J11	V_{DD}	S		-	-	-
61	85	H11	M14	104	J2	116	L12	PD14	I/O	FT	-	TIM4_CH3, FMC_D0, EVENTOUT	-
62	86	J12	L14	105	K1	117	K13	PD15	I/O	FT	-	TIM4_CH4, FMC_D1, EVENTOUT	-
-	-	-	-	-	-	118	K12	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	-	-	119	J12	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-
-	-	-	-	-	-	120	H12	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-
-	-	-	-	-	-	121	J13	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-
-	-	-	-	-	-	122	H13	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-
-	-	-	-	-	-	123	G12	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-
-	-	-	-	-	-	124	H11	VDD	I/O	FT	-	-	-
-	-	-	-	-	-	125	H10	VSS	I/O	FT	-	-	-
-	-	-	-	-	-	126	G13	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-
-	-	-	-	-	-	127	F12	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-
-	-	-	-	-	-	128	F13	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-
-	87	H13	L15	106	J1	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	88	NC (2)	K15	107	G3	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	89	H12	K14	108	G5	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	90	G13	K13	109	G6	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
96	140	C4	B4	168	B9	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	B4	A4	169	B10	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_RX, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A4	A3	170	A10	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	F5	D5	-	-	202	F6	V_{SS}	S		-		-
-	143	C3	C6	171	A11	203	E5	PDR_ON	S		-		-
100	144	K6	C5	172	D7	204	E7	V_{DD}	S		-		-
-	-	B3	D4	173	-	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A3	C4	174	-	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A2	C3	175	-	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	C2	176	-	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. Function availability depends on the chosen device.
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).

4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: *www.st.com*.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
6. If the device is delivered in an WLCSP143, UFBGA169, UFBGA176, LQFP176 or TFBGA216 package, and the BYPASS_REG pin is set to V_{DD} (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).
7. PI0 and PI1 cannot be used for I2S2 full-duplex mode.
8. The DCMI_VSYNC alternate function on PG9 is only available on silicon revision 3.

Table 11. FMC pin definition

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	A0			A0
PF1	A1	A1			A1
PF2	A2	A2			A2
PF3	A3	A3			A3
PF4	A4	A4			A4
PF5	A5	A5			A5
PF12	A6	A6			A6
PF13	A7	A7			A7
PF14	A8	A8			A8
PF15	A9	A9			A9
PG0	A10	A10			A10
PG1		A11			A11
PG2		A12			A12
PG3		A13			
PG4		A14			BA0
PG5		A15			BA1
PD11		A16	A16	CLE	
PD12		A17	A17	ALE	
PD13		A18	A18		
PE3		A19	A19		
PE4		A20	A20		
PE5		A21	A21		
PE6		A22	A22		
PE2		A23	A23		
PG13		A24	A24		
PG14		A25	A25		
PD14	D0	D0	DA0	D0	D0
PD15	D1	D1	DA1	D1	D1
PD0	D2	D2	DA2	D2	D2
PD1	D3	D3	DA3	D3	D3
PE7	D4	D4	DA4	D4	D4
PE8	D5	D5	DA5	D5	D5
PE9	D6	D6	DA6	D6	D6
PE10	D7	D7	DA7	D7	D7

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)[1]	270	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)[1]	− 270	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)[1]	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)[1]	− 100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/Os and control pin	− 25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins [2]	120	
	Total output current sourced by sum of all I/Os and control pins[2]	− 120	
$I_{INJ(PIN)}$ [3]	Injected current on FT pins [4]	− 5/+0	
	Injected current on NRST and BOOT0 pins [4]		
	Injected current on TTa pins[5]	±5	
$\Sigma I_{INJ(PIN)}$[5]	Total injected current (sum of all I/O and control pins)[6]	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.21: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14* for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	°C

Table 22. reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are sbject to general operating conditions for T_A.

Table 23. Over-drive switching characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	µs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

Table 31. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	
I_{DD12} / I_{DD}	Supply current in RUN mode from V_{12} and V_{DD} supply	All Peripherals enabled	168	77.8	1.3	76.8	1.0	mA
			150	70.8	1.3	69.8	1.0	
			144	64.5	1.3	63.6	1.0	
			120	49.9	1.2	49.3	0.9	
			90	39.2	1.3	38.7	1.0	
			60	27.2	1.2	26.8	0.9	
			30	15.6	1.2	15.4	0.9	
			25	13.6	1.2	13.5	0.9	
		All Peripherals disabled	168	38.2	1.3	37.0	1.0	
			150	34.6	1.3	33.4	1.0	
			144	31.3	1.3	30.3	1.0	
			120	24.0	1.2	23.2	0.9	
			90	18.1	1.4	18.0	1.0	
			60	12.9	1.2	12.5	0.9	
			30	7.2	1.2	6.9	0.9	
			25	6.3	1.2	6.1	0.9	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

Table 44. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics

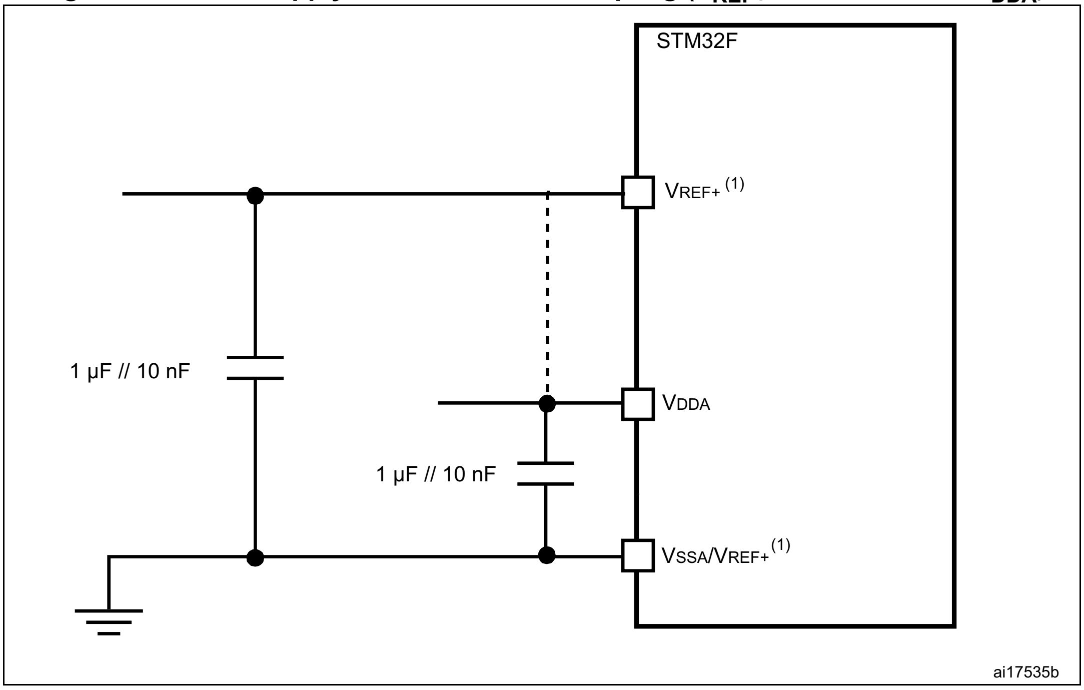
<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>f_{PLLSAI_IN}</td><td>PLLSAI input clock(1)</td><td colspan="2"></td><td>0.95(2)</td><td>1</td><td>2.10</td><td>MHz</td></tr>
<tr><td>f_{PLLSAI_OUT}</td><td>PLLSAI multiplier output clock</td><td colspan="2"></td><td>-</td><td>-</td><td>216</td><td>MHz</td></tr>
<tr><td>f_{VCO_OUT}</td><td>PLLSAI VCO output</td><td colspan="2"></td><td>100</td><td>-</td><td>432</td><td>MHz</td></tr>
<tr><td rowspan="2">t_{LOCK}</td><td rowspan="2">PLLSAI lock time</td><td colspan="2">VCO freq = 100 MHz</td><td>75</td><td>-</td><td>200</td><td rowspan="2">µs</td></tr>
<tr><td colspan="2">VCO freq = 432 MHz</td><td>100</td><td>-</td><td>300</td></tr>
<tr><td rowspan="4">Jitter(3)</td><td rowspan="3">Main SAI clock jitter</td><td rowspan="2">Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5</td><td>RMS</td><td>-</td><td>90</td><td>-</td><td></td></tr>
<tr><td>peak to peak</td><td>-</td><td>±280</td><td>-</td><td>ps</td></tr>
<tr><td colspan="2">Average frequency of 12.288 MHz
N = 432, R = 5
on 1000 samples</td><td>-</td><td>90</td><td>-</td><td>ps</td></tr>
<tr><td>FS clock jitter</td><td colspan="2">Cycle to cycle at 48 KHz
on 1000 samples</td><td>-</td><td>400</td><td>-</td><td>ps</td></tr>
<tr><td>$I_{DD(PLLSAI)}$(4)</td><td>PLLSAI power consumption on V_{DD}</td><td colspan="2">VCO freq = 100 MHz
VCO freq = 432 MHz</td><td>0.15
0.45</td><td>-</td><td>0.40
0.75</td><td>mA</td></tr>
<tr><td>$I_{DDA(PLLSAI)}$(4)</td><td>PLLSAI power consumption on V_{DDA}</td><td colspan="2">VCO freq = 100 MHz
VCO freq = 432 MHz</td><td>0.30
0.55</td><td>-</td><td>0.40
0.85</td><td>mA</td></tr>
</table>

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 52* or *Figure 53*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 52. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 102. SDRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. CL = 30 pF on data and address lines. CL=15pF on FMC_SDCLK.
2. Guaranteed by characterization results.

Table 103. LPSDR SDRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	1	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	1	-	

1. CL = 10 pF.
2. Guaranteed by characterization results.

6.3.27 Camera interface (DCMI) timing specifications

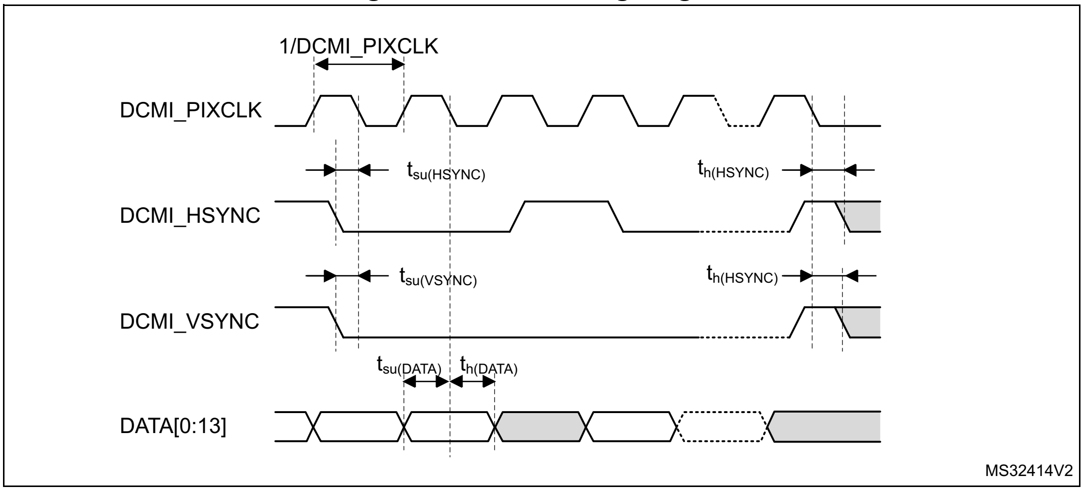
Unless otherwise specified, the parameters given in Table 106 for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in Table 17, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 106. DCMI characteristics

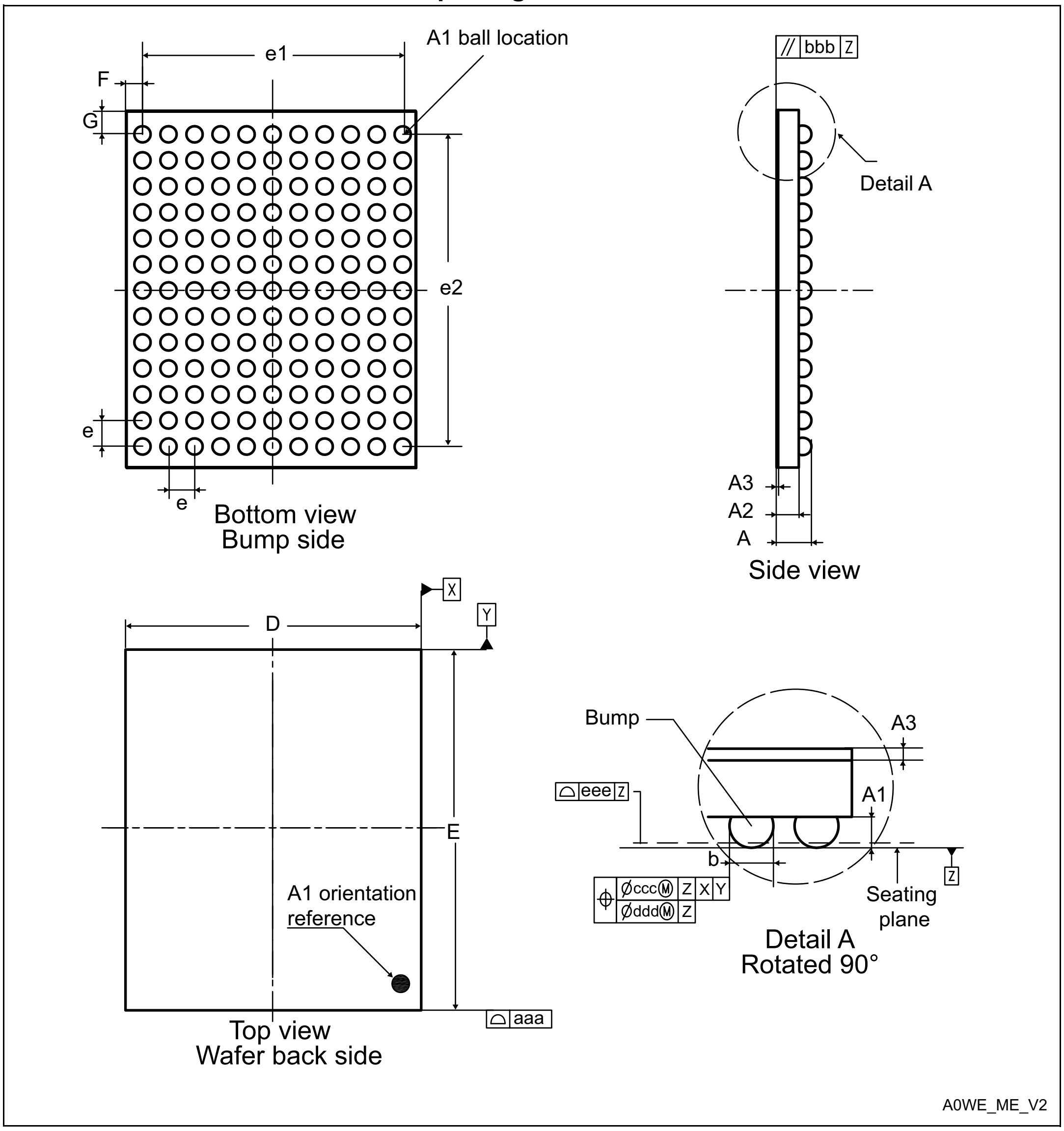
Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data input hold time	2.5	-	ns
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	0.5	-	ns
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	ns

Figure 75. DCMI timing diagram



7.2 WLCSP143 package information

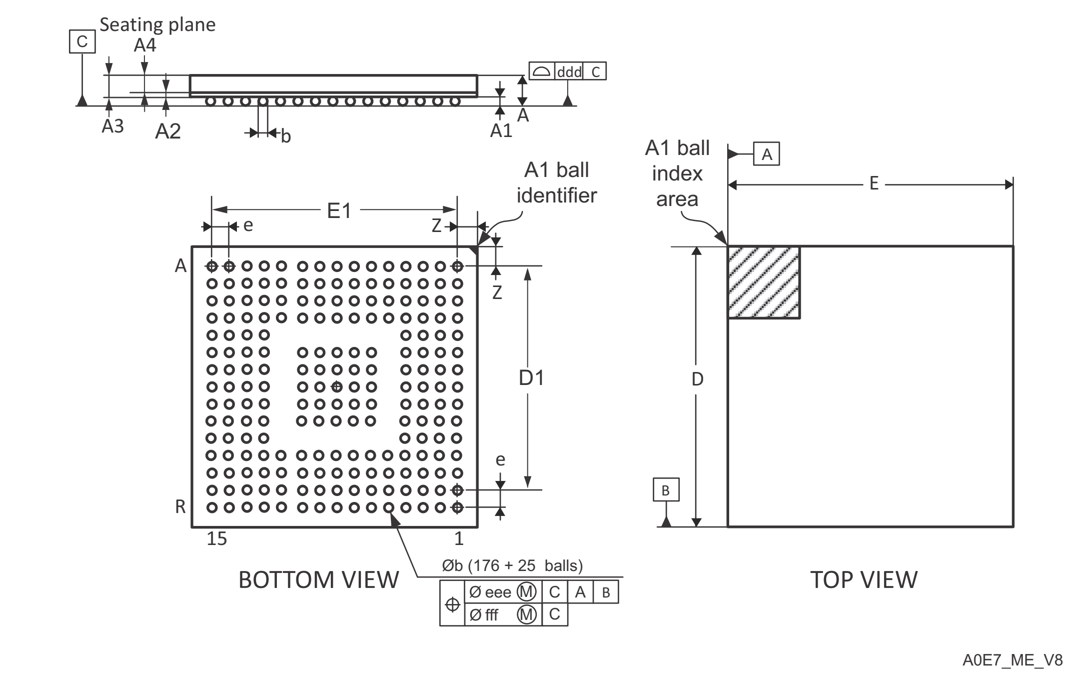
Figure 83. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

7.7 UFBGA176+25 package information

Figure 98. UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline

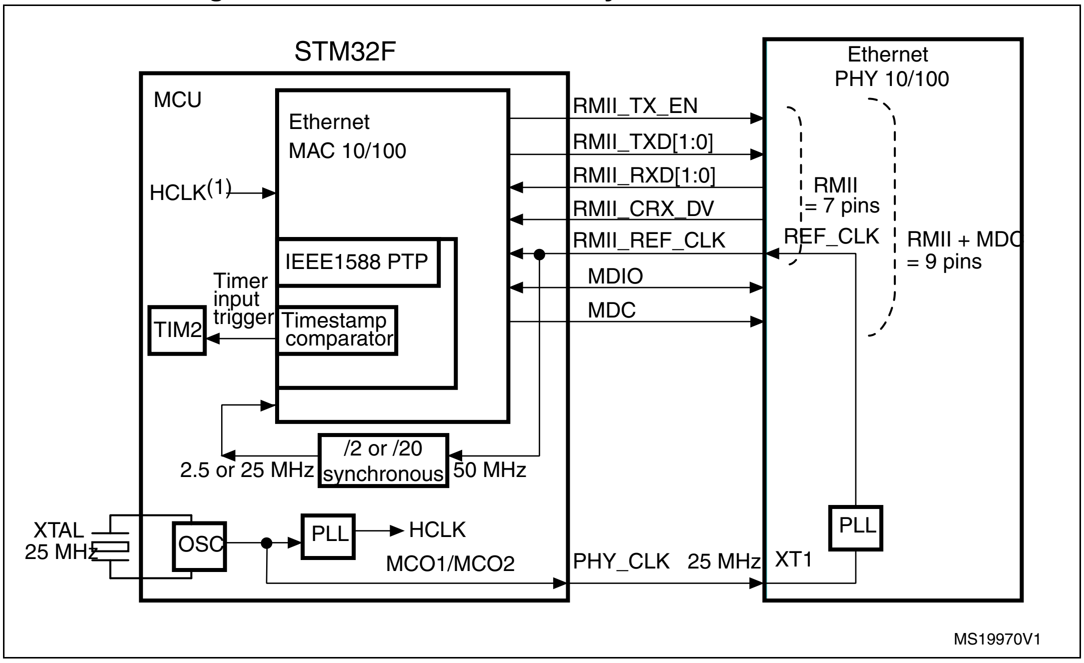


1. Drawing is not to scale.

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Figure 109. RMII with a 25 MHz crystal and PHY with PLL



1. f_{HCLK} must be greater than 25 MHz.
2. The 25 MHz (PHY_CLK) must be derived directly from the HSE oscillator, before the PLL block.

Table 124. Document revision history

Date	Revision	Changes
19-Feb-2015	5	Update SPI/IS2 in *Table 2: STM32F427xx and STM32F429xx features and peripheral counts*. Updated LQFP208 in *Table 4: Regulator ON/OFF and internal reset ON/OFF availability*. Updated *Figure 19: Memory map*. Changed PLS[2:0]=101 (falling edge) maximum value in *Table 22: reset and power control block characteristics*. Updated current consumption with all peripherals disabled in *Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM*. Updated note *1.* in *Table 28: Typical and maximum current consumptions in Standby mode*. Updated t_{WUSTOP} in *Table 36: Low-power mode wakeup timings*. Updated ESD standards and *Table 53: ESD absolute maximum ratings*. Updated *Table 56: I/O static characteristics*. *Section : I2C interface characteristics*: updated section introduction, removed Table *I2C characteristics*, Figure *I2C bus AC waveforms and measurement circuit* and Table *SCL frequency*; added *Table 61: I2C analog filter characteristics*. Updated measurement conditions in *Table 62: SPI dynamic characteristics*. Updated *Figure 51: Typical connection diagram using the ADC*. Updated *Section : Device marking for LQFP100*. Updated *Figure 83: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline* and *Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data*; added *Figure 84: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint* and *Table 112: WLCSP143 recommended PCB design rules (0.4 mm pitch)*. Updated *Figure 85: WLCSP143 marking example (package top view)* and related note. Updated *Section : Device marking for WLCSP143*. Updated *Section : Device marking for LQFP144*. Updated *Section : Device marking for LQFP176*. Updated *Figure 92: LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline*; Updated *Section : Device marking for LQFP208*. Modified UFBGA169 pitch, updated *Figure 95: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 116: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*; updated *Section : Device marking for LQFP208*. updated *Section : Device marking for UFBGA169*, *Section : Device marking for UFBGA176+25* and *Section : Device marking for TFBGA176*. Updated Z pin count in *Table 122: Ordering information scheme*.