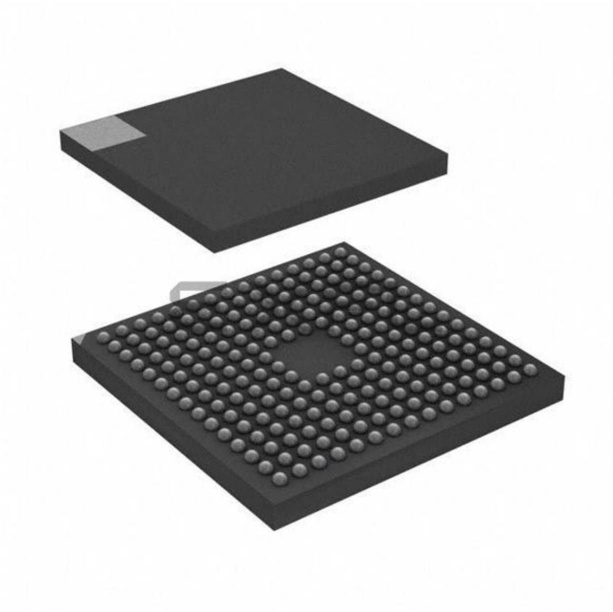

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429nih6e

communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison[1]

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

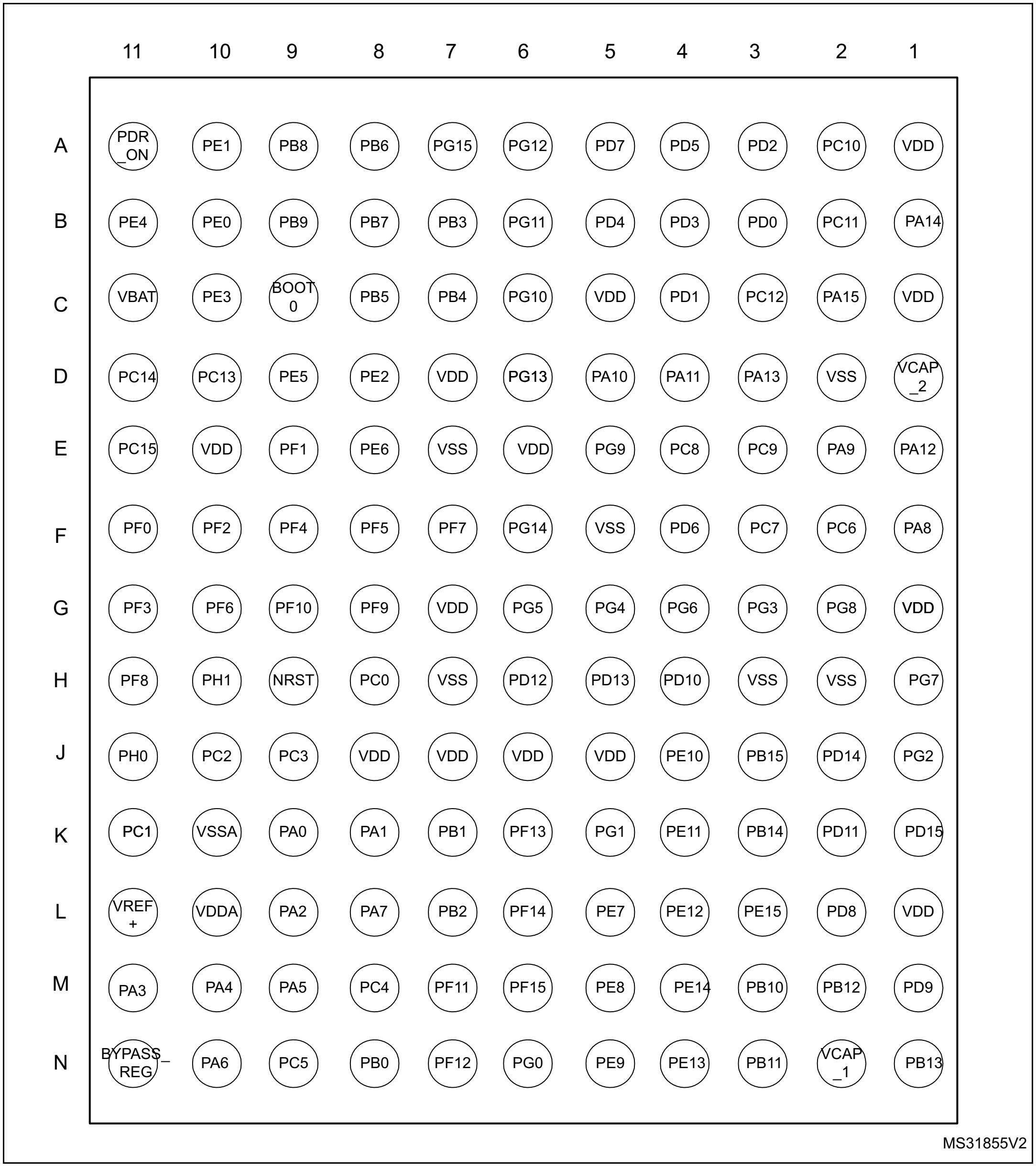
1. X = feature supported.

3.25 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

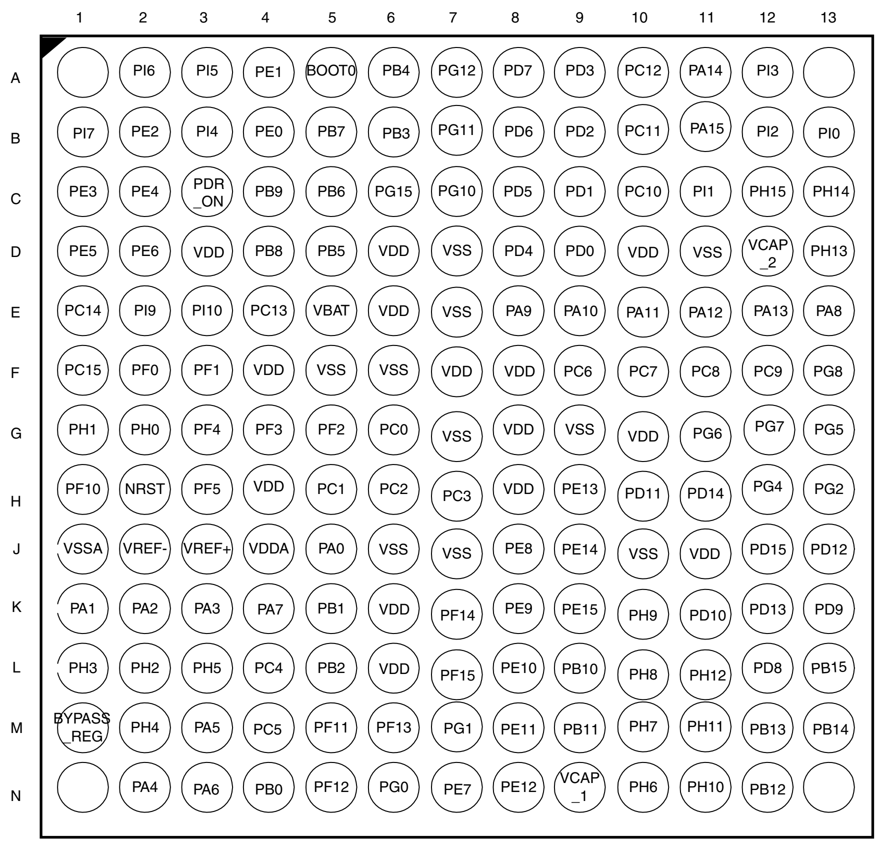
Figure 12. STM32F42x WLCSP143 ballout



	11	10	9	8	7	6	5	4	3	2	1
A	PDR_ON	PE1	PB8	PB6	PG15	PG12	PD7	PD5	PD2	PC10	VDD
B	PE4	PE0	PB9	PB7	PB3	PG11	PD4	PD3	PD0	PC11	PA14
C	VBAT	PE3	BOOT0	PB5	PB4	PG10	VDD	PD1	PC12	PA15	VDD
D	PC14	PC13	PE5	PE2	VDD	PG13	PA10	PA11	PA13	VSS	VCAP_2
E	PC15	VDD	PF1	PE6	VSS	VDD	PG9	PC8	PC9	PA9	PA12
F	PF0	PF2	PF4	PF5	PF7	PG14	VSS	PD6	PC7	PC6	PA8
G	PF3	PF6	PF10	PF9	VDD	PG5	PG4	PG6	PG3	PG8	VDD
H	PF8	PH1	NRST	PC0	VSS	PD12	PD13	PD10	VSS	VSS	PG7
J	PH0	PC2	PC3	VDD	VDD	VDD	VDD	PE10	PB15	PD14	PG2
K	PC1	VSSA	PA0	PA1	PB1	PF13	PG1	PE11	PB14	PD11	PD15
L	VREF+	VDDA	PA2	PA7	PB2	PF14	PE7	PE12	PE15	PD8	VDD
M	PA3	PA4	PA5	PC4	PF11	PF15	PE8	PE14	PB10	PB12	PD9
N	BYPASS_REG	PA6	PC5	PB0	PF12	PG0	PE9	PE13	PB11	VCAP_1	PB13

1. The above figure shows the package bump view.

Figure 16. STM32F42x UFBGA169 ballout



	1	2	3	4	5	6	7	8	9	10	11	12	13
A		PI6	PI5	PE1	BOOT0	PB4	PG12	PD7	PD3	PC12	PA14	PI3	
B	PI7	PE2	PI4	PE0	PB7	PB3	PG11	PD6	PD2	PC11	PA15	PI2	PI0
C	PE3	PE4	PDR_ON	PB9	PB6	PG15	PG10	PD5	PD1	PC10	PI1	PH15	PH14
D	PE5	PE6	VDD	PB8	PB5	VDD	VSS	PD4	PD0	VDD	VSS	VCAP_2	PH13
E	PC14	PI9	PI10	PC13	VBAT	VDD	VSS	PA9	PA10	PA11	PA12	PA13	PA8
F	PC15	PF0	PF1	VDD	VSS	VSS	VDD	VDD	PC6	PC7	PC8	PC9	PG8
G	PH1	PH0	PF4	PF3	PF2	PC0	VSS	VDD	VSS	VDD	PG6	PG7	PG5
H	PF10	NRST	PF5	VDD	PC1	PC2	PC3	VDD	PE13	PD11	PD14	PG4	PG2
J	VSSA	VREF-	VREF+	VDDA	PA0	VSS	VSS	PE8	PE14	VSS	VDD	PD15	PD12
K	PA1	PA2	PA3	PA7	PB1	VDD	PF14	PE9	PE15	PH9	PD10	PD13	PD9
L	PH3	PH2	PH5	PC4	PB2	VDD	PF15	PE10	PB10	PH8	PH12	PD8	PB15
M	BYPASS_REG	PH4	PA5	PC5	PF11	PF13	PG1	PE11	PB11	PH7	PH11	PB13	PB14
N		PA4	PA6	PB0	PF12	PG0	PE7	PE12	VCAP_1	PH6	PH10	PB12	

1. The above figure shows the package top view.
2. The 4 corners balls, A1,A13, N1 and N13, are not bonded internally and should be left not connected on the PCB.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions

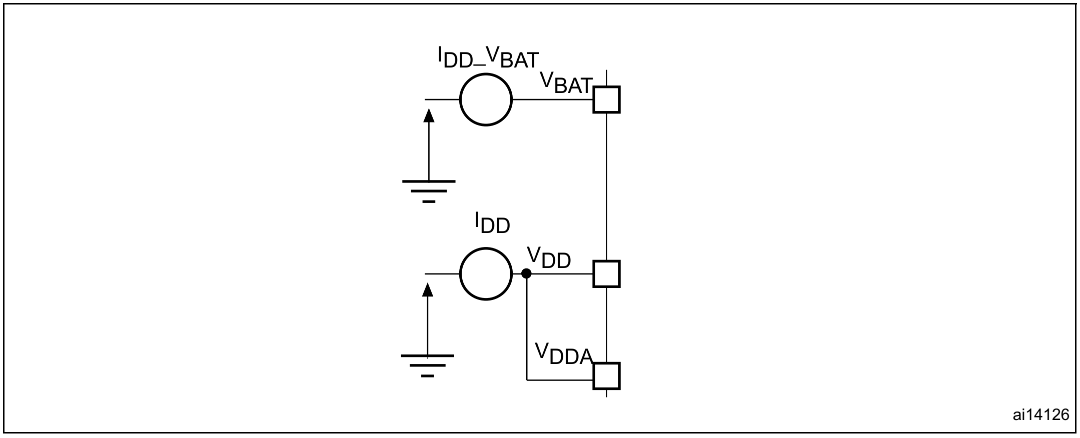
Pin number								Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
1	1	B2	A2	1	D8	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	C1	A1	2	C10	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
3	3	C2	B1	3	B11	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-

Table 12. STM32F427xx and STM32F429xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT

6.1.7 Current consumption measurement

Figure 23. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{DD} and VBAT)(1)	– 0.3	4.0	V
V_{IN}	Input voltage on FT pins(2)	V_{SS} – 0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.15: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 15* for the values of the maximum allowed injected current.

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 27*.

The characteristics given in *Table 37* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 37. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Table 44. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$[4]	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$[4]	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>f_{PLLSAI_IN}</td><td>PLLSAI input clock[1]</td><td colspan="2"></td><td>0.95[2]</td><td>1</td><td>2.10</td><td>MHz</td></tr>
<tr><td>f_{PLLSAI_OUT}</td><td>PLLSAI multiplier output clock</td><td colspan="2"></td><td>-</td><td>-</td><td>216</td><td>MHz</td></tr>
<tr><td>f_{VCO_OUT}</td><td>PLLSAI VCO output</td><td colspan="2"></td><td>100</td><td>-</td><td>432</td><td>MHz</td></tr>
<tr><td rowspan="2">t_{LOCK}</td><td rowspan="2">PLLSAI lock time</td><td colspan="2">VCO freq = 100 MHz</td><td>75</td><td>-</td><td>200</td><td rowspan="2">µs</td></tr>
<tr><td colspan="2">VCO freq = 432 MHz</td><td>100</td><td>-</td><td>300</td></tr>
<tr><td rowspan="4">Jitter[3]</td><td rowspan="3">Main SAI clock jitter</td><td rowspan="2">Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5</td><td>RMS</td><td>-</td><td>90</td><td>-</td><td></td></tr>
<tr><td>peak to peak</td><td>-</td><td>±280</td><td>-</td><td>ps</td></tr>
<tr><td colspan="2">Average frequency of 12.288 MHz
N = 432, R = 5
on 1000 samples</td><td>-</td><td>90</td><td>-</td><td>ps</td></tr>
<tr><td>FS clock jitter</td><td colspan="2">Cycle to cycle at 48 KHz
on 1000 samples</td><td>-</td><td>400</td><td>-</td><td>ps</td></tr>
<tr><td>$I_{DD(PLLSAI)}$[4]</td><td>PLLSAI power consumption on V_{DD}</td><td colspan="2">VCO freq = 100 MHz
VCO freq = 432 MHz</td><td>0.15
0.45</td><td>-</td><td>0.40
0.75</td><td>mA</td></tr>
<tr><td>$I_{DDA(PLLSAI)}$[4]</td><td>PLLSAI power consumption on V_{DDA}</td><td colspan="2">VCO freq = 100 MHz
VCO freq = 432 MHz</td><td>0.30
0.55</td><td>-</td><td>0.40
0.85</td><td>mA</td></tr>
</table>

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Figure 33 and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

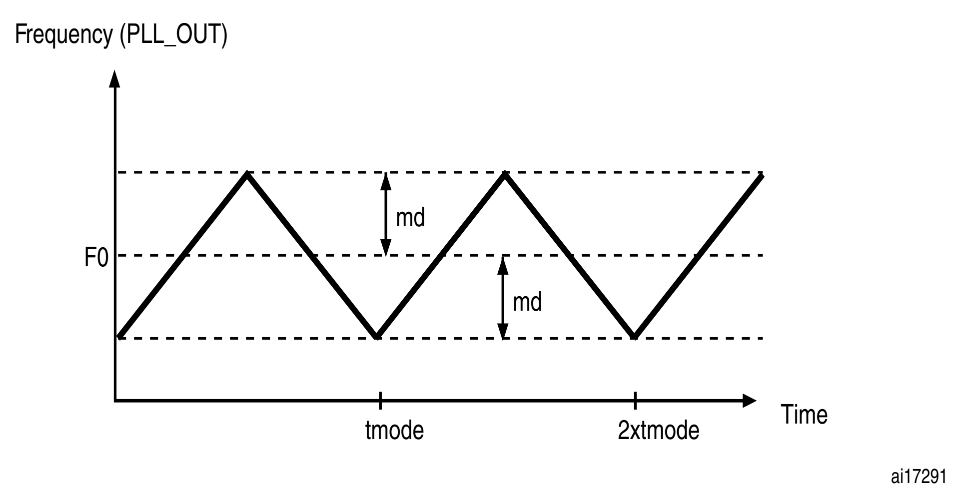


Figure 34. PLL output clock waveforms in down spread mode

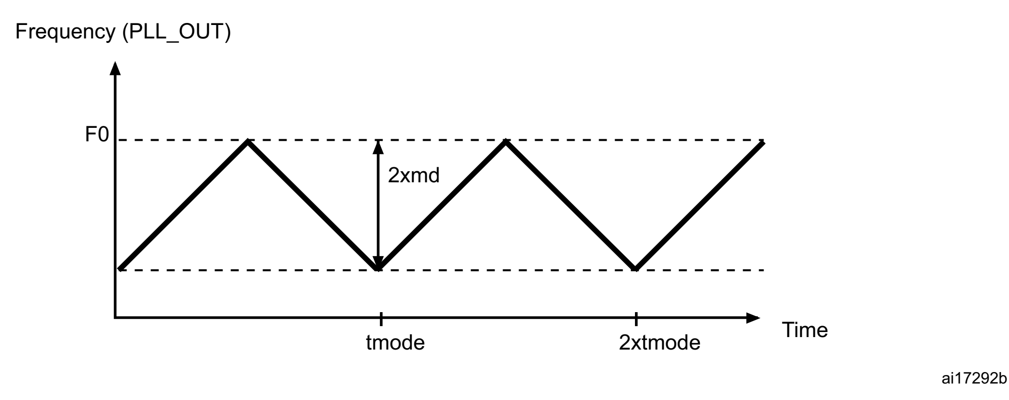
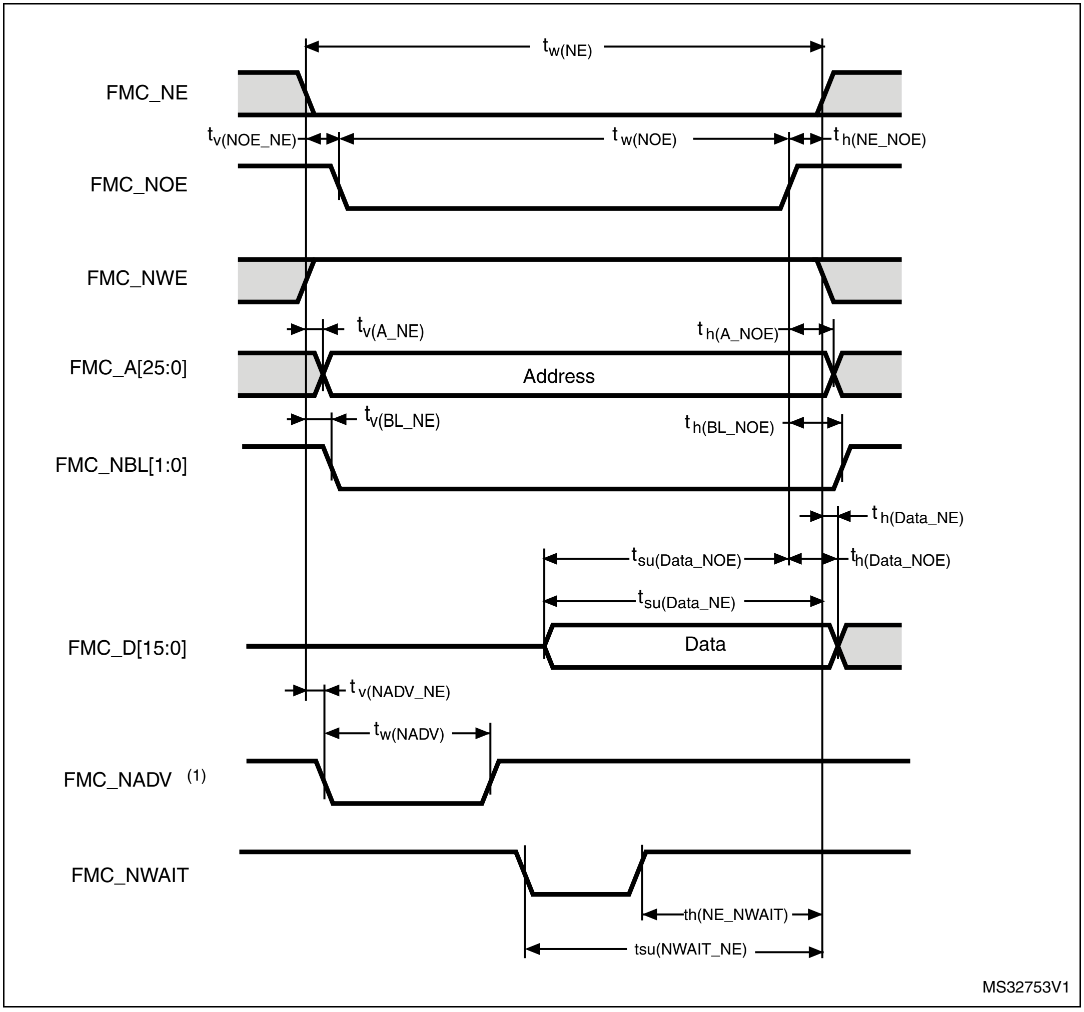


Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

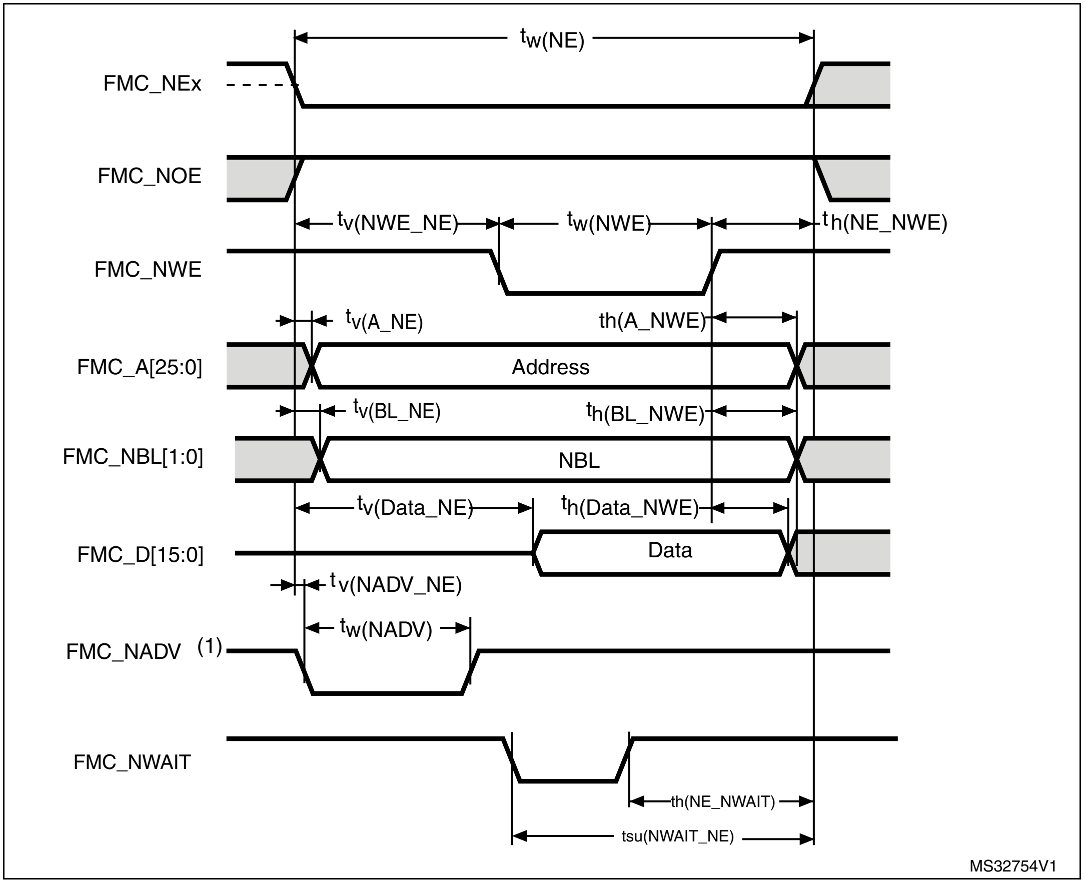


1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 0.5$	$2\ T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	ns
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$	$2T_{HCLK}+ 0.5$	ns
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	ns
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 2.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} +2$	-	ns

Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



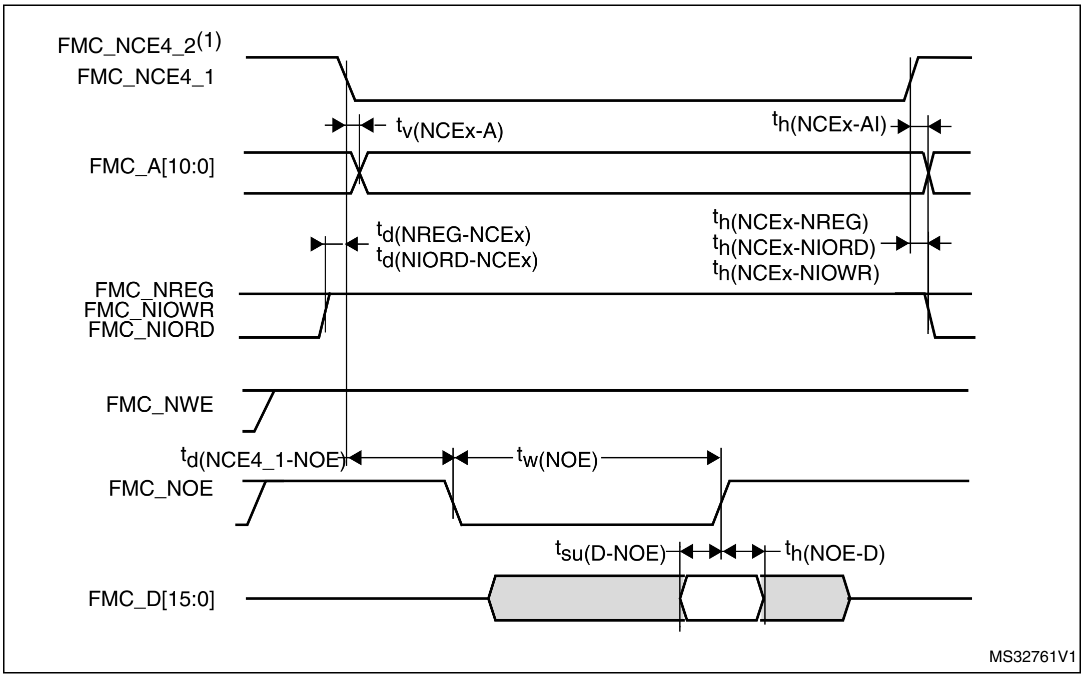
1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	$T_{HCLK}+ 0.5$	ns
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} +1.5$	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+ 2$	ns
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	ns
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+ 0.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Figure 63. PC Card/CompactFlash controller waveforms for common memory read access



1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 64. PC Card/CompactFlash controller waveforms for common memory write access

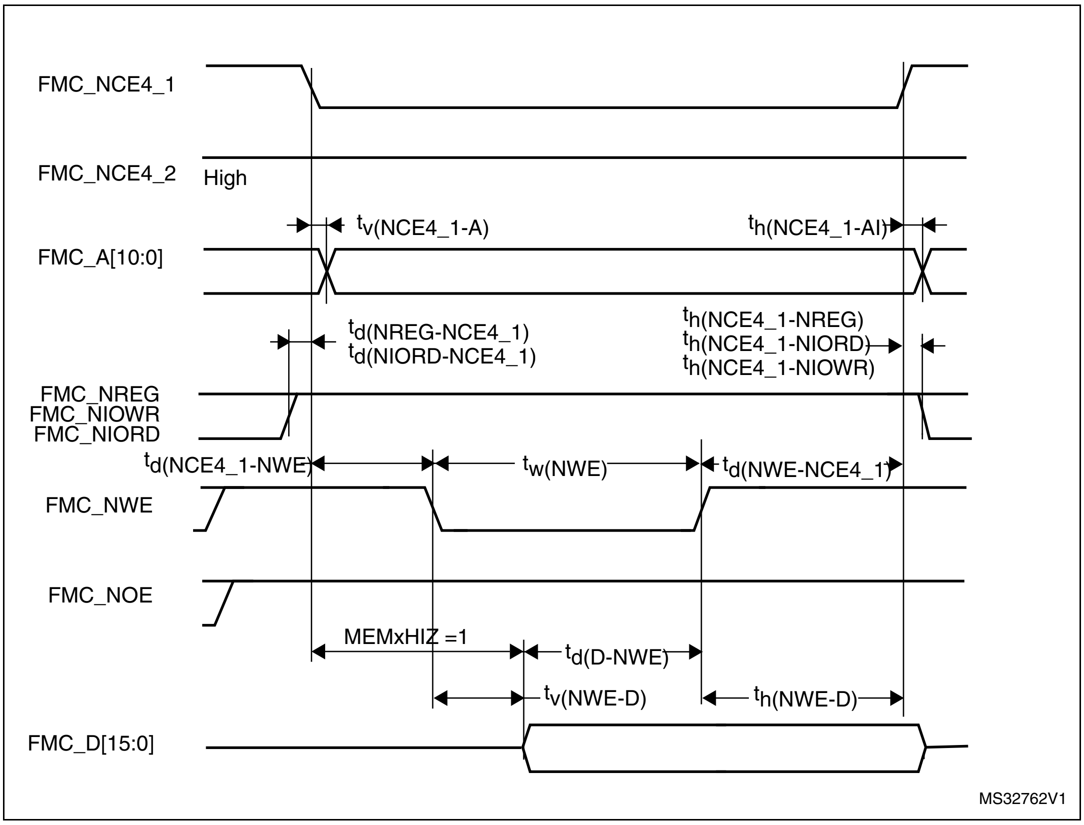
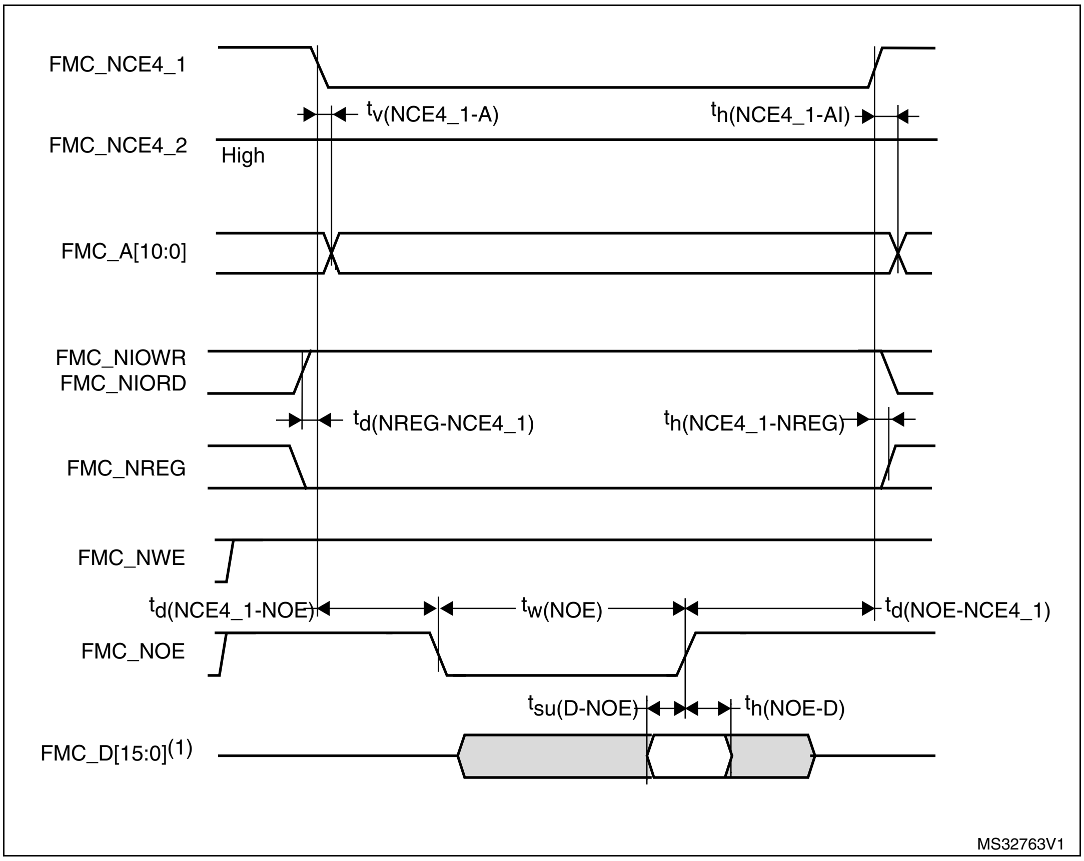


Figure 65. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

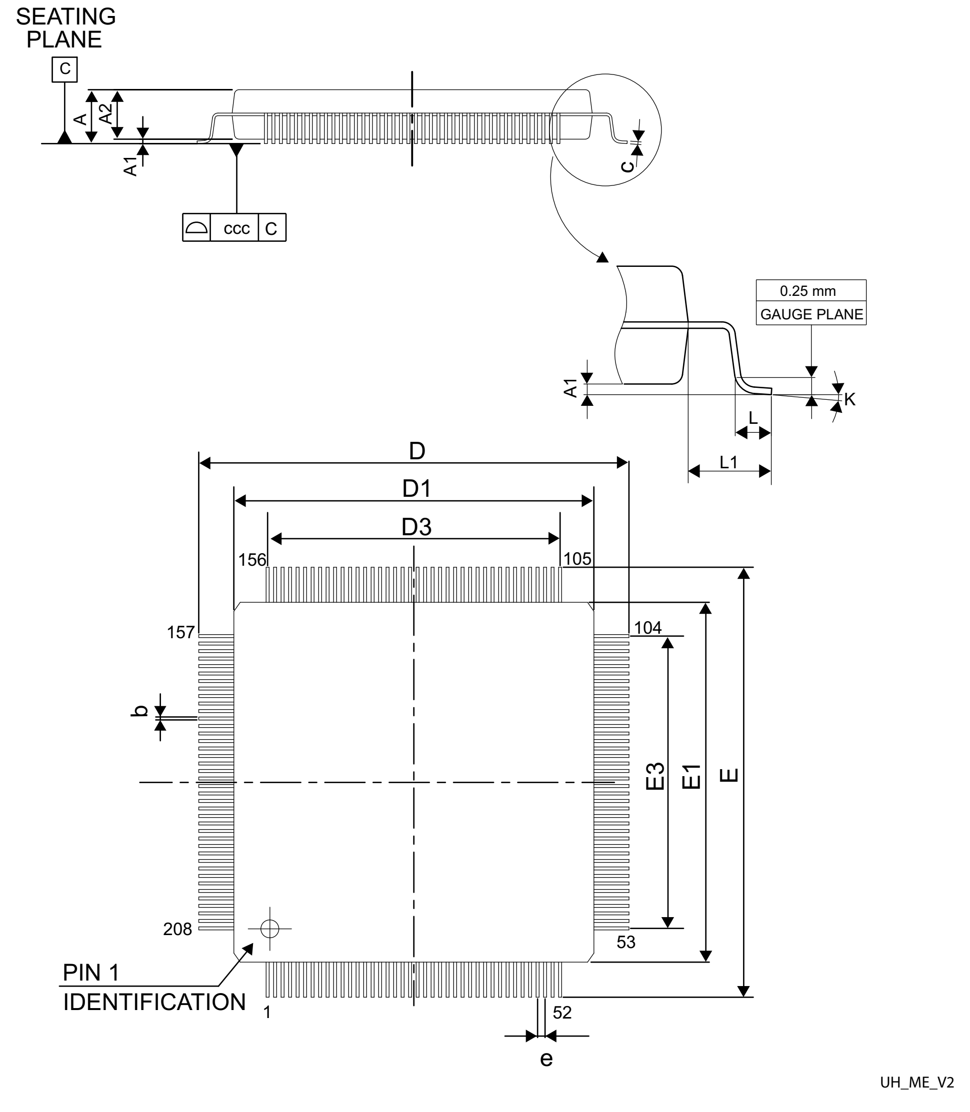
Table 110. LQPF100 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

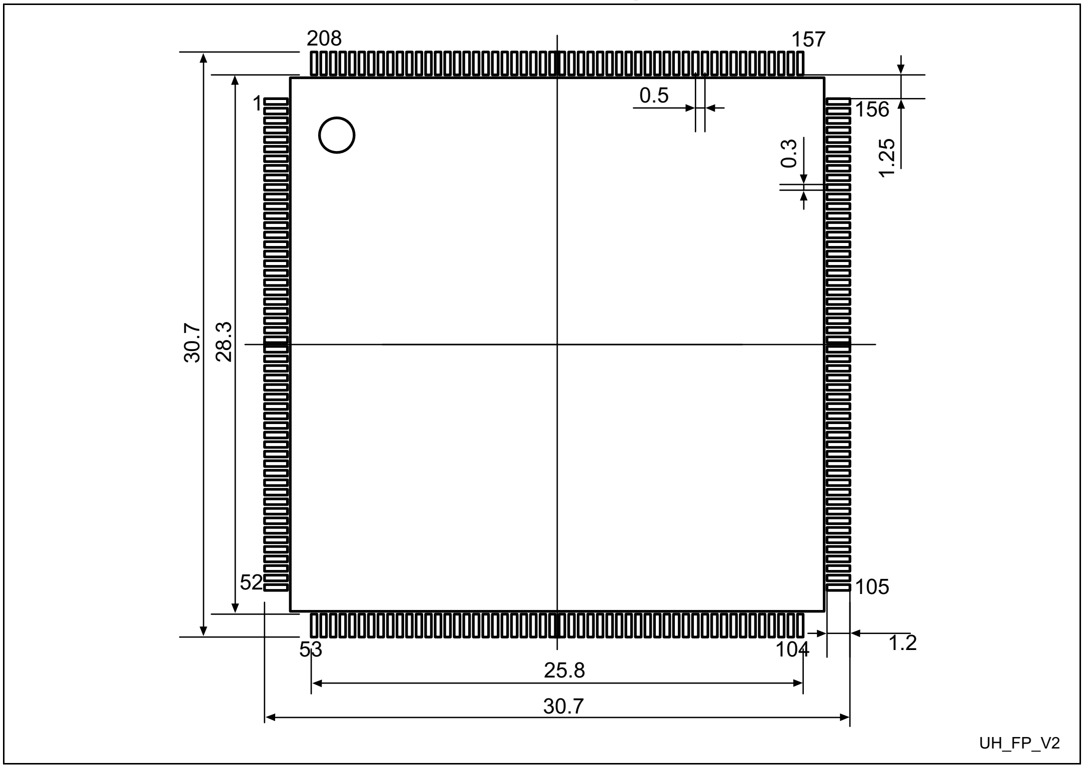
7.5 LQFP208 package information

Figure 92. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline



1. Drawing is not to scale.

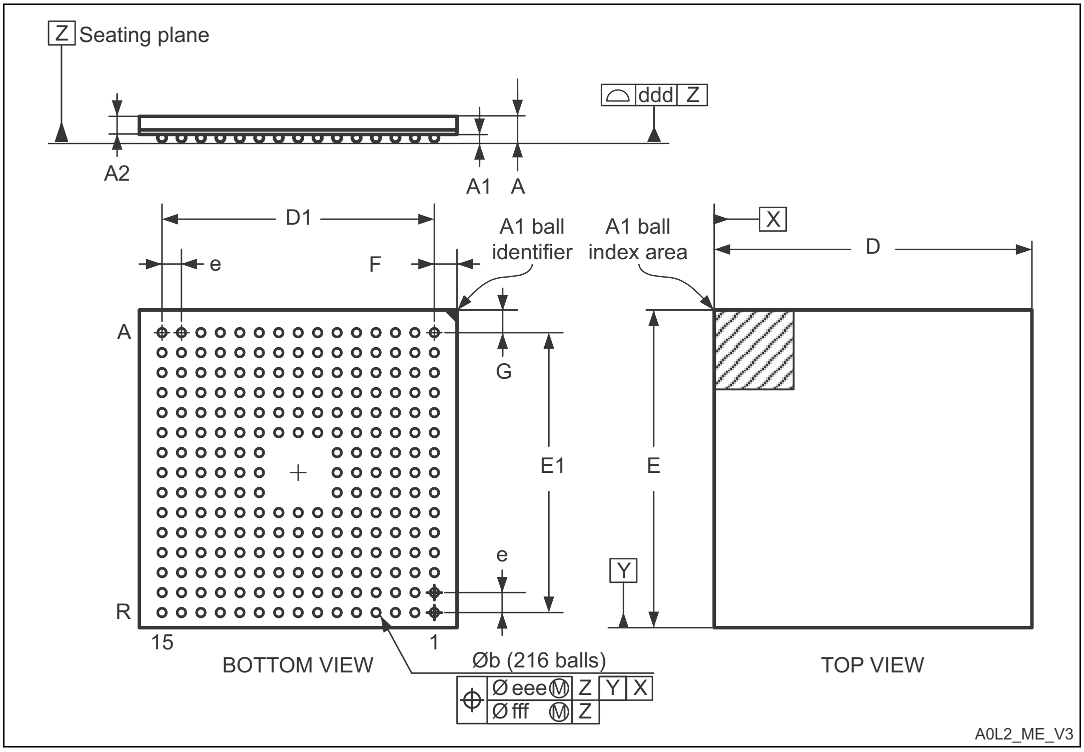
Figure 93. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.8 TFBGA216 package information

Figure 101. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039

7.9 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 121. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient WLCSP143	31.2	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA169 - 7 × 7mm / 0.5 mm pitch	52	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 124. Document revision history

Date	Revision	Changes
17-Sep-2015	6	Updated notes related to the minimum and maximum values guaranteed by design, characterization or test in production. Updated $I_{DD\_STOP\_UDM}$ in *Table 27: Typical and maximum current consumptions in Stop mode*. Removed note related to tests in production in *Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM* and *Table 26: Typical and maximum current consumption in Sleep mode*. Updated *Table 41: HSI oscillator characteristics*. *Figure 31* renamed *ACCHSI accuracy versus temperature* and updated. Updated *Figure 38: SPI timing diagram - slave mode and CPHA = 0*. Updated *Section : Ethernet characteristics*. Updated *Table 43: Main PLL characteristics*, *Table 44: PLLI2S (audio PLL) characteristics* and *Table 45: PLLISAI (audio and LCD-TFT PLL) characteristics*. Removed note 1 in *Table 75: ADC static accuracy at fADC = 18 MHz*, *Table 76: ADC static accuracy at fADC = 30 MHz* and *Table 77: ADC static accuracy at fADC = 36 MHz*. Updated $t_{d(SDCLKL\_Data)}$ and $t_{h(SDCLKL\_Data)}$ in *Table 104: SDRAM write timings*. Added *Figure 96: UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint* and *Table 117: UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 99: UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint* and *Table 119: UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)*.
30-Nov-2015	7	Updated $\|V_{SSX} - V_{SS}\|$ in *Table 14: Voltage characteristics* to add V_{REF-}. Updated $t_{d(TXEN)}$ and $t_{d(TXD)}$ minimum value in *Table 72: Dynamics characteristics: Ethernet MAC signals for RMII* and *Table 73: Dynamics characteristics: Ethernet MAC signals for MII*. Added V_{REF-} in *Table 74: ADC characteristics*. Added A1 minimum and maximum values in *Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data*. Updated *Figure 86: LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline*. Updated *Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline* and *Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data*. Updated *Figure 101: TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline* and *Table 120: TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data*.