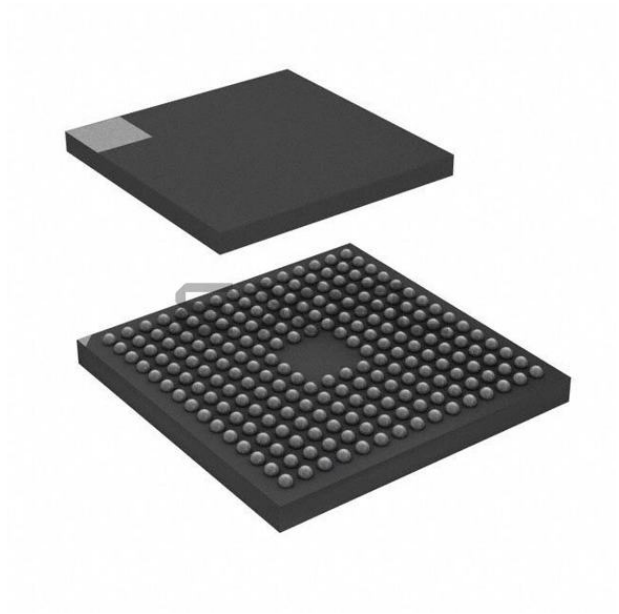

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429nih7

Table 2. STM32F427xx and STM32F429xx features and peripheral counts (continued)

Peripherals		STM32F427 Vx	STM32F429Vx	STM32F427 Zx	STM32F429Zx	STM32F427 Ax	STM32F429 Ax	STM32F427 Ix	STM32F429Ix	STM32F429Bx	STM32F429Nx
Communication interfaces	SPI / I^2S	4/2 (full duplex)(2)		6/2 (full duplex)(2)							
	I^2C	3									
	USART/ UART	4/4									
	USB OTG FS	Yes									
	USB OTG HS	Yes									
	CAN	2									
	SAI	1									
	SDIO	Yes									
Camera interface		Yes									
LCD-TFT (STM32F429xx only)		No	Yes	No	Yes	No	Yes	No	Yes		
Chrom-ART Accelerator™		Yes									
GPIOs		82		114		130		140		168	
12-bit ADC Number of channels		3									
		16		24							
12-bit DAC Number of channels		Yes 2									
Maximum CPU frequency		180 MHz									
Operating voltage		1.8 to 3.6 V(3)									
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C									
		Junction temperature: –40 to + 125 °C									
Packages		LQFP100		WLCSP143 LQFP144		UFBGA169		UFBGA176 LQFP176		LQFP208	TFBGA216

1. For the LQFP100 package, only FMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package. For UFBGA169 package, only SDRAM, NAND and multiplexed static memories are supported.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF)*.

3.26 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

Note: For I2S2 *full-duplex mode, I2S2_CK and I2S2_WS signals can be used only on GPIO Port B and GPIO Port D.*

3.27 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S and SAI applications. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^2S/SAI flow with an external PLL (or Codec output).

3.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

3.39 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.40 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 10-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

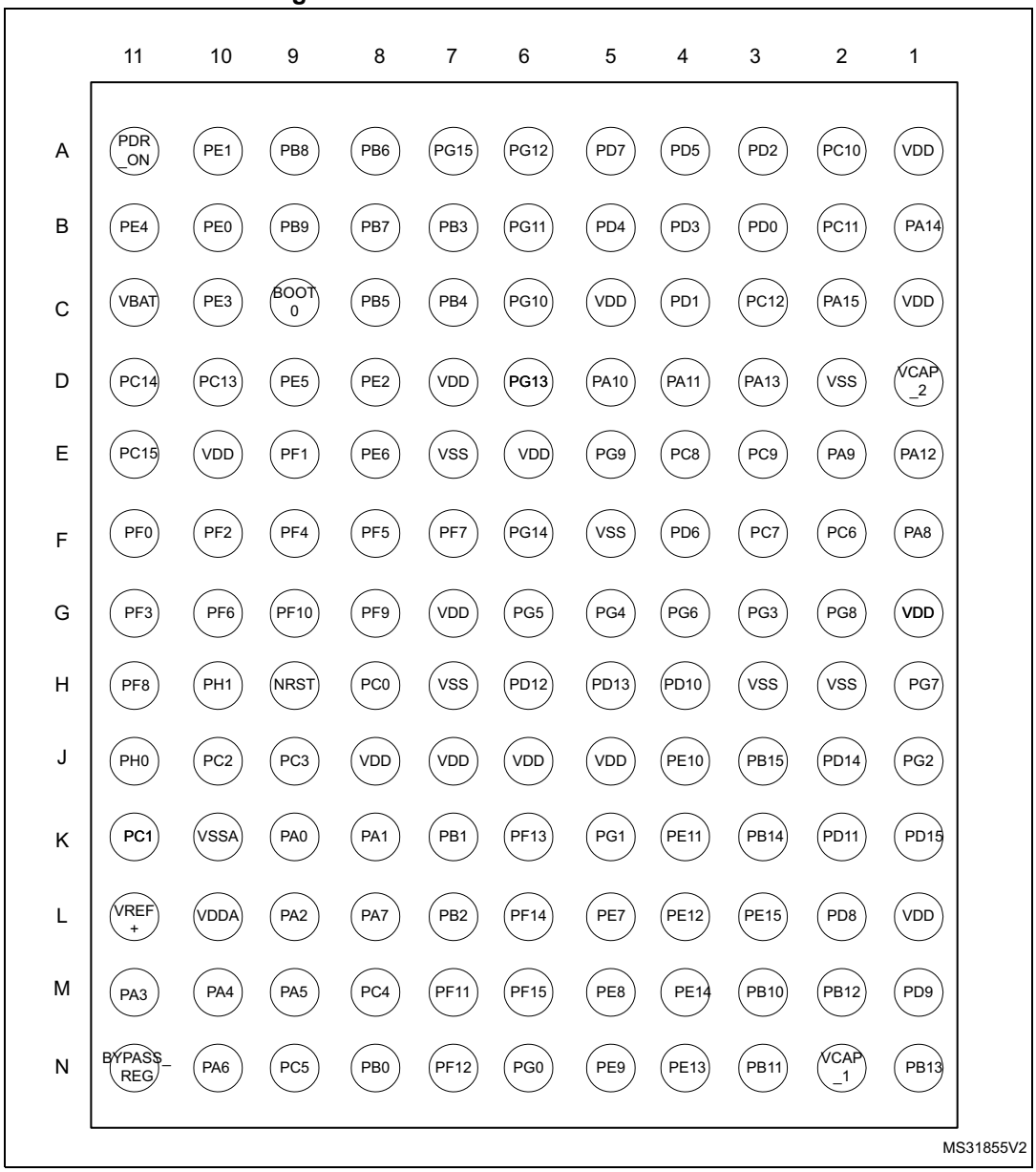
Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.41 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 12. STM32F42x WLCSP143 ballout



1. The above figure shows the package bump view.

Table 11. FMC pin definition (continued)

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	D8	DA8	D8	D8
PE12	D9	D9	DA9	D9	D9
PE13	D10	D10	DA10	D10	D10
PE14	D11	D11	DA11	D11	D11
PE15	D12	D12	DA12	D12	D12
PD8	D13	D13	DA13	D13	D13
PD9	D14	D14	DA14	D14	D14
PD10	D15	D15	DA15	D15	D15
PH8		D16			D16
PH9		D17			D17
PH10		D18			D18
PH11		D19			D19
PH12		D20			D20
PH13		D21			D21
PH14		D22			D22
PH15		D23			D23
PI0		D24			D24
PI1		D25			D25
PI2		D26			D26
PI3		D27			D27
PI6		D28			D28
PI7		D29			D29
PI9		D30			D30
PI10		D31			D31
PD7		NE1	NE1	NCE2	
PG9		NE2	NE2	NCE3	
PG10	NCE4_1	NE3	NE3		
PG11	NCE4_2				
PG12		NE4	NE4		
PD3		CLK	CLK		
PD4	NOE	NOE	NOE	NOE	
PD5	NWE	NWE	NWE	NWE	
PD6	NWAIT	NWAIT	NWAIT	NWAIT	
PB7		NL(NADV)	NL(NADV)		

Table 12. STM32F427xx and STM32F429xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4001 6C00- 0x4001 FFFF	Reserved
APB2	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 5C00 - 0x4001 67FF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

6.3.5 Reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 22. reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis		-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis		-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis		-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	POR reset temporization		0.5	1.5	3.0	ms

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART accelerator is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 180 MHz (Scale1 + over-drive ON), f_{HCLK} = 144 MHz (Scale 2), f_{HCLK} = 120 MHz (Scale 3)"
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 35. Peripheral current consumption

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 180 MHz)	GPIOA	2.50	2.36	2.08	µA/MHz
	GPIOB	2.56	2.36	2.08	
	GPIOC	2.44	2.29	2.00	
	GPIOD	2.50	2.36	2.08	
	GPIOE	2.44	2.29	2.00	
	GPIOF	2.44	2.29	2.00	
	GPIOG	2.39	2.22	2.00	
	GPIOH	2.33	2.15	1.92	
	GPIOI	2.39	2.22	2.00	
	GPIOJ	2.33	2.15	1.92	
	GPIOK	2.33	2.15	1.92	
	OTG_HS+ULPI	27.00	24.86	21.92	
	CRC	0.44	0.42	0.33	
	BKPSRAM	0.78	0.69	0.58	
	DMA1	25.33	23.26	20.50	
	DMA2	24.72	22.71	20.00	
	DMA2D	28.50	26.32	23.33	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	21.56	20.07	17.75	

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 28*.

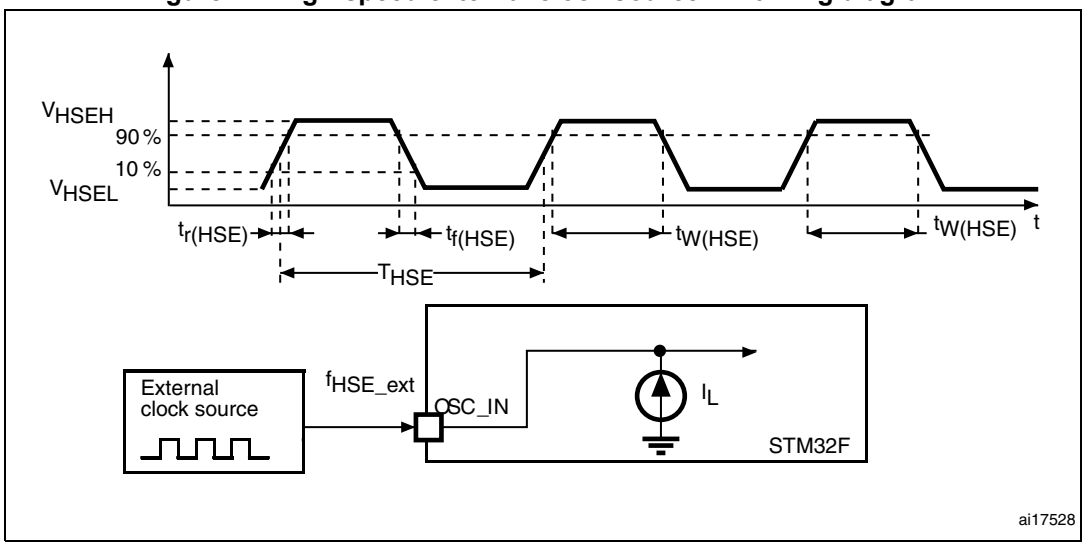
The characteristics given in *Table 38* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 38. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

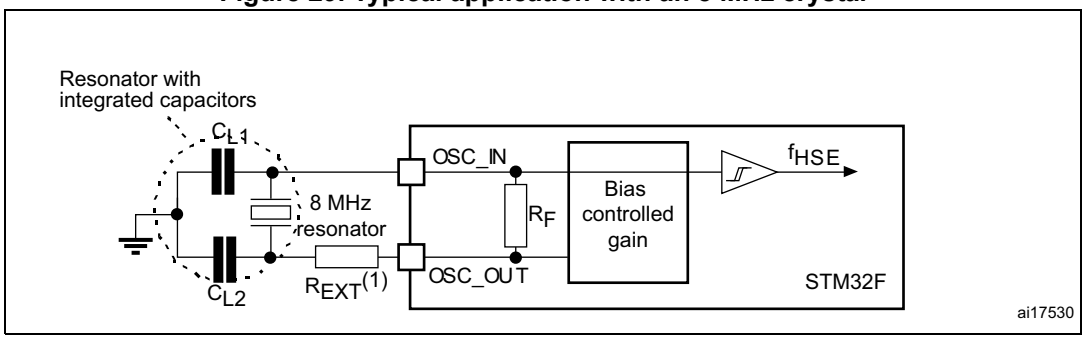
Figure 27. High-speed external clock source AC timing diagram



For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 29*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 29. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

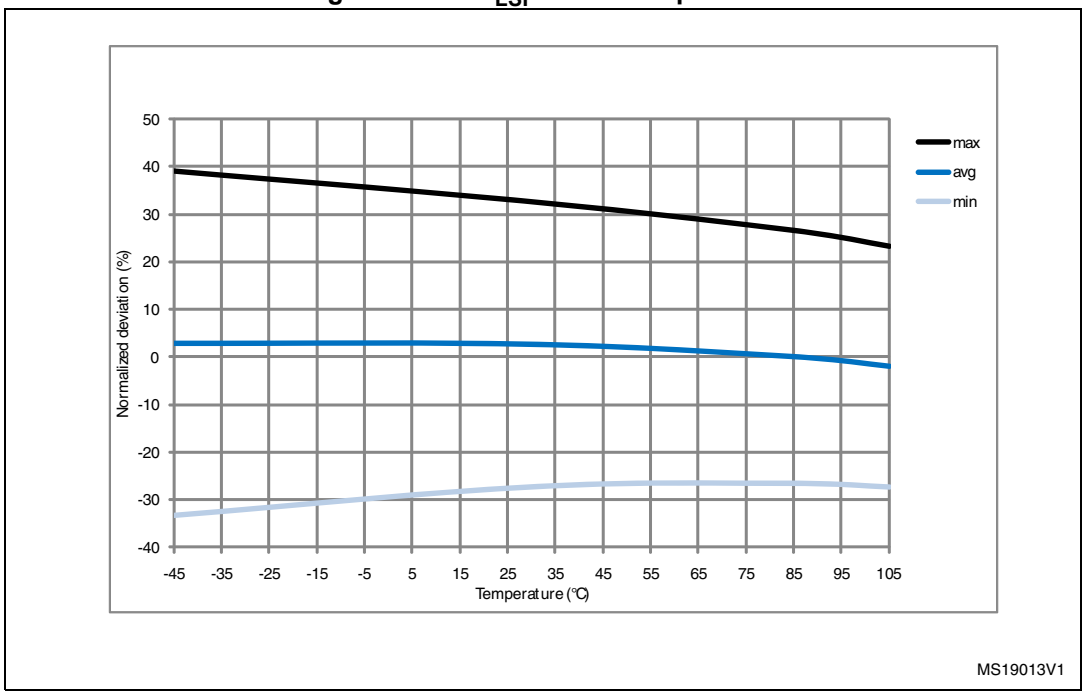
Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor		-	18.4	-	MΩ
I_{DD}	LSE current consumption		-	-	1	µA
ACC_{LSE} (2)	LSE accuracy		− 500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Startup	-	-	0.56	µA/V
$t_{SU(LSE)}$ (3)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. Refer to application note AN2867.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 32. ACC_{LSI} versus temperature



6.3.11 PLL characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 43. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)		0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock		24	-	180	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock		-	48	75	MHz
f_{VCO_OUT}	PLL VCO output		100	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 100 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 56: I/O static characteristics*).

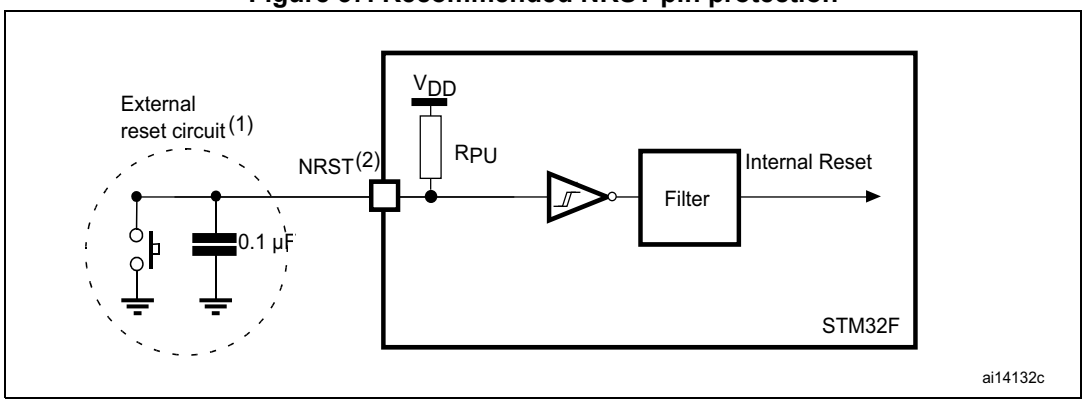
Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 59. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset is not taken into account by the device.

Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms

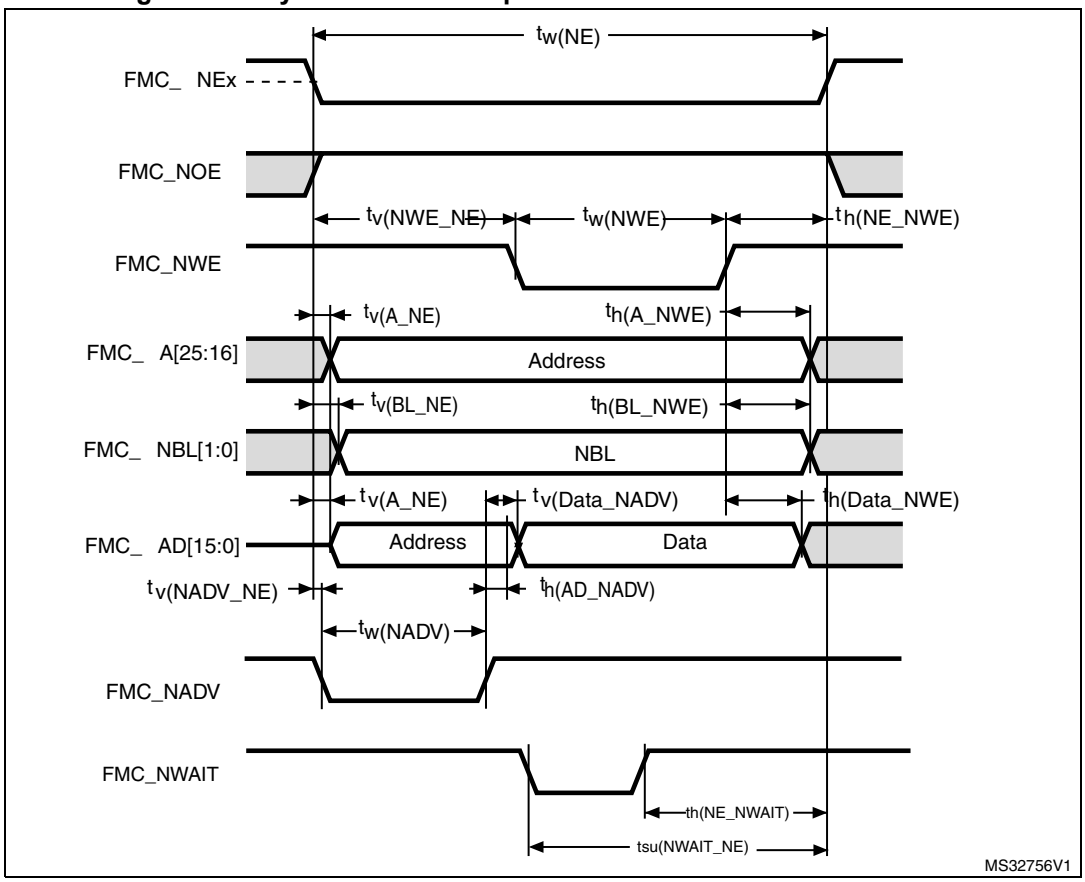
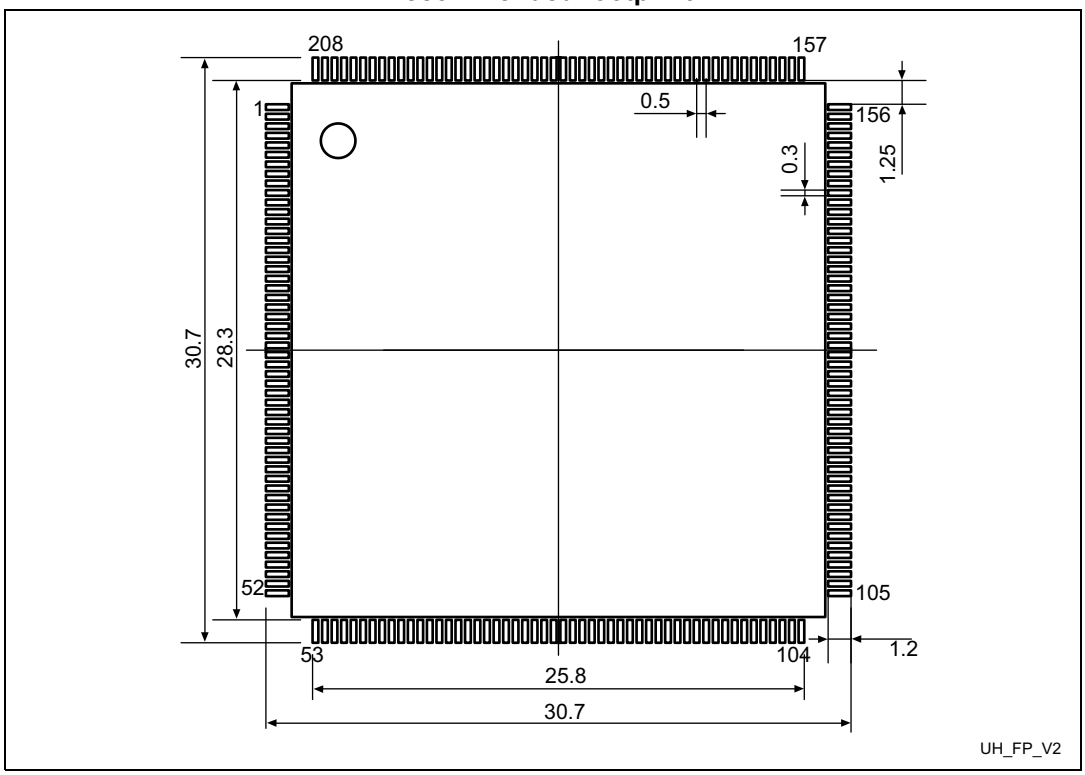


Table 92. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	ns
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{HCLK} - 2$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	ns
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK}+1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

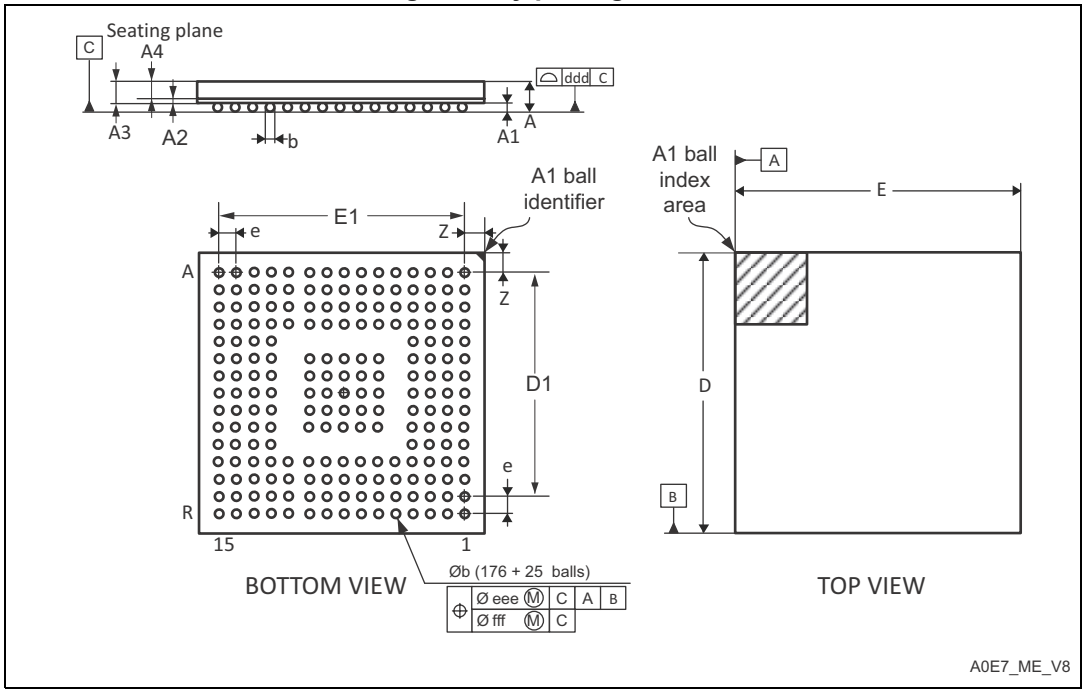
Figure 93. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.7 UFBGA176+25 package information

Figure 98. UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.
- The over-drive mode is not supported.

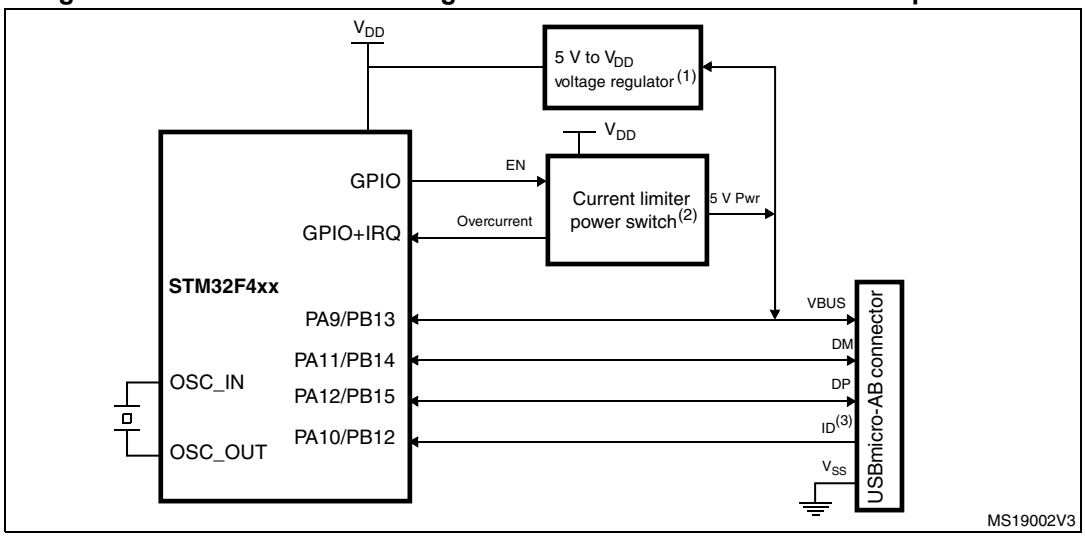
A.1 Operating conditions

Table 123. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz(4)	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.17.1: Internal reset ON*).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

Figure 105. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.