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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429vet6

Figure 2. Compatible board design between STM32F10xx/STM32F2xx/STM32F4xx for LQFP144 package

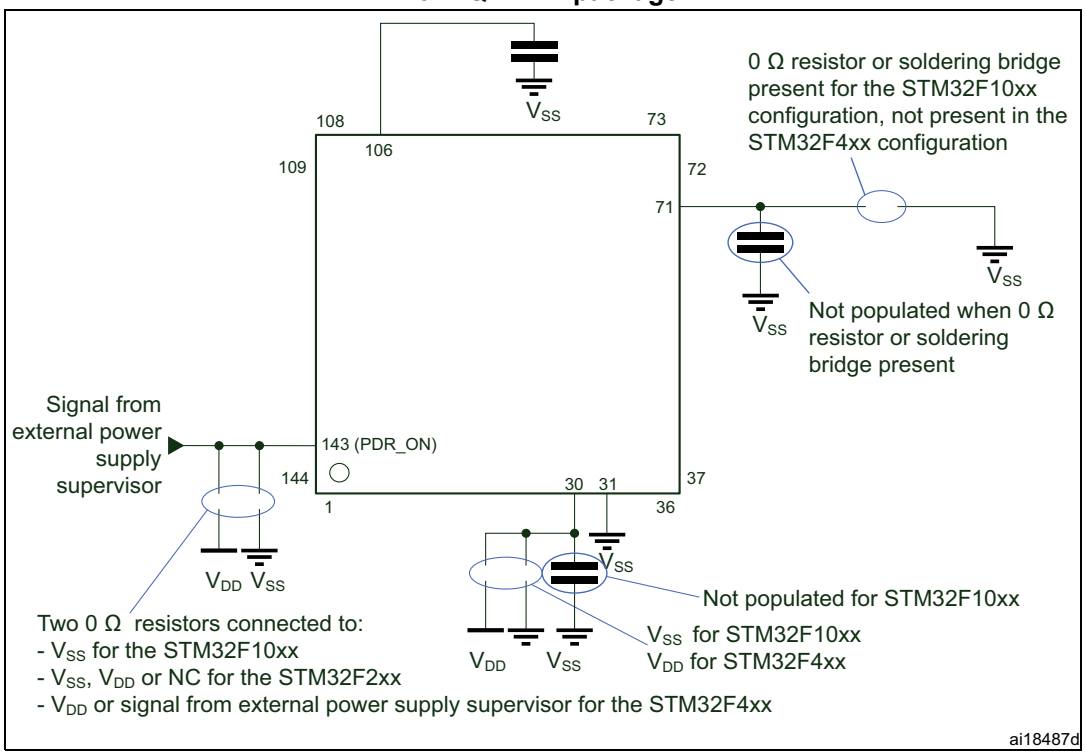
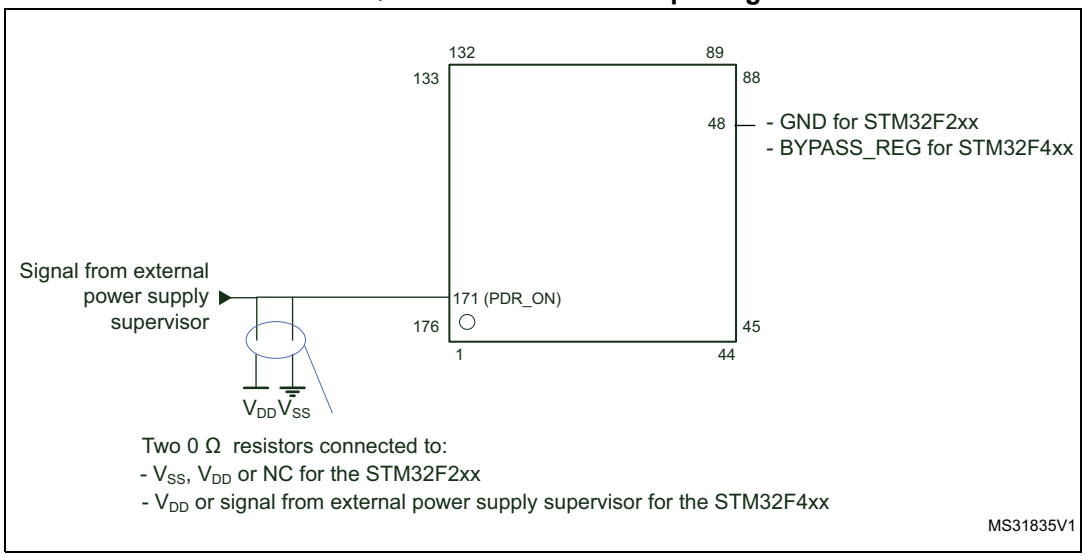


Figure 3. Compatible board design between STM32F2xx and STM32F4xx for LQFP176 and UFBGA176 packages



3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F42x devices (see *Table 6* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F42x include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

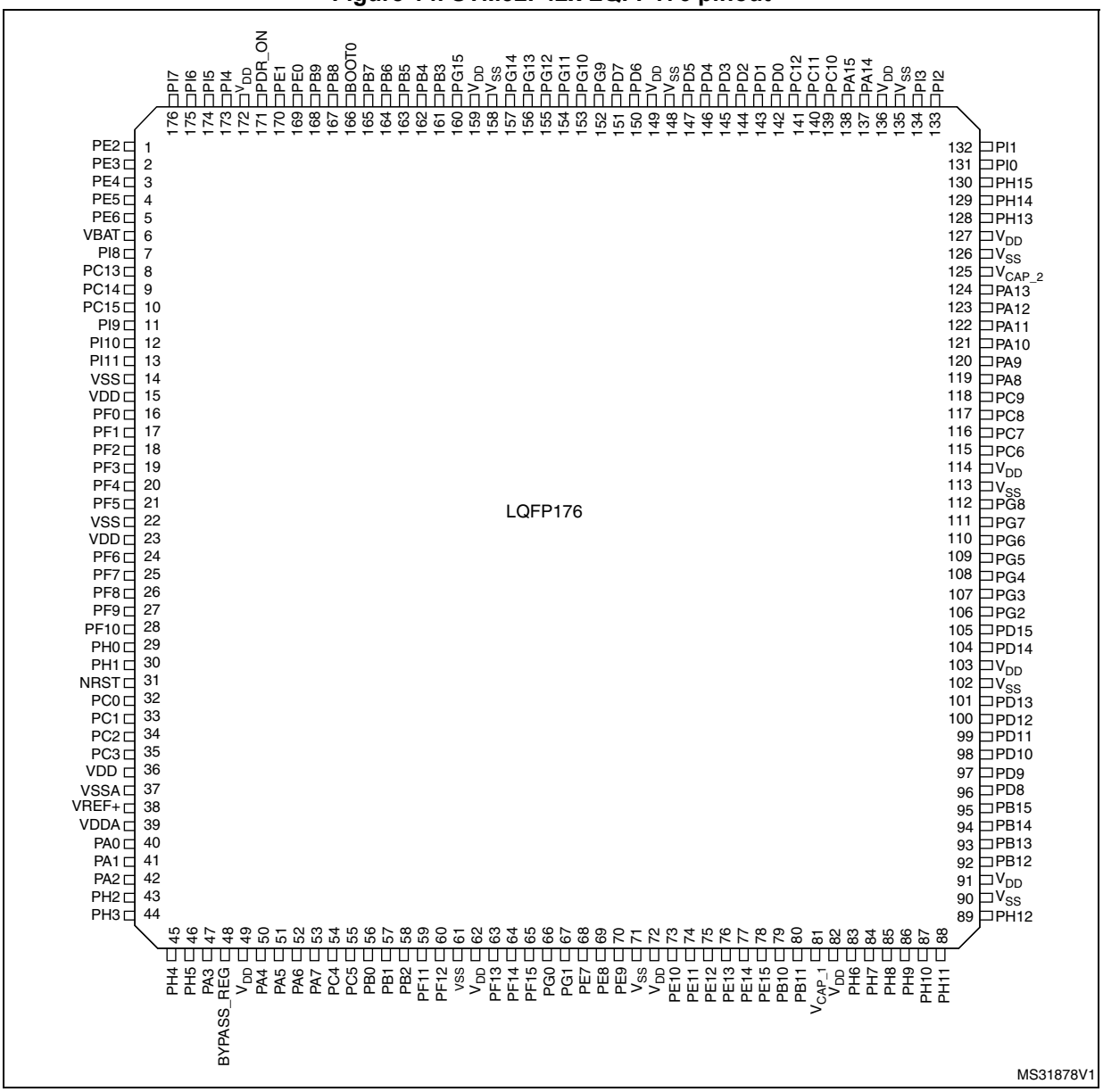
  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.22.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

Figure 14. STM32F42x LQFP176 pinout



1. The above figure shows the package top view.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
38	58	N7	R8	68	L5	79	R8	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, FMC_D4, EVENTOUT	-
39	59	J8	P8	69	M5	80	N9	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, FMC_D5, EVENTOUT	-
40	60	K8	P9	70	N5	81	P9	PE9	I/O	FT	-	TIM1_CH1, FMC_D6, EVENTOUT	-
-	61	J6	M9	71	H3	82	K8	V_{SS}	S		-		-
-	62	G10	N9	72	J5	83	L9	V_{DD}	S		-		-
41	63	L8	R9	73	J4	84	R9	PE10	I/O	FT	-	TIM1_CH2N, FMC_D7, EVENTOUT	-
42	64	M8	P10	74	K4	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, FMC_D8, LCD_G3, EVENTOUT	-
43	65	N8	R10	75	L4	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, FMC_D9, LCD_B4, EVENTOUT	-
44	66	H9	N11	76	N4	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, FMC_D10, LCD_DE, EVENTOUT	-
45	67	J9	P11	77	M4	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, FMC_D11, LCD_CLK, EVENTOUT	-
46	68	K9	R11	78	L3	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
47	69	L9	R12	79	M3	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
48	70	M9	R13	80	N3	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port D	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1/FMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	FMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	FMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	UART8_Rx	-	-	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	-	-	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	-	-	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	-	-	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	-	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT

Table 22. reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are sbject to general operating conditions for T_A.

Table 23. Over-drive switching characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	µs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

6.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 36* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	6	-	CPU clock cycle
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	13.6	-	µs
		Main regulator is ON and Flash memory in Deep power down mode	93	111	
		Low power regulator is ON	22	32	
		Low power regulator is ON and Flash memory in Deep power down mode	103	126	
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	105	128	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	125	155	
tWUSTDBY (2)(3)	Wakeup from Standby mode		318	412	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first
3. $t_{WUSTDBY}$ maximum value is given at –40 °C.

Table 44. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

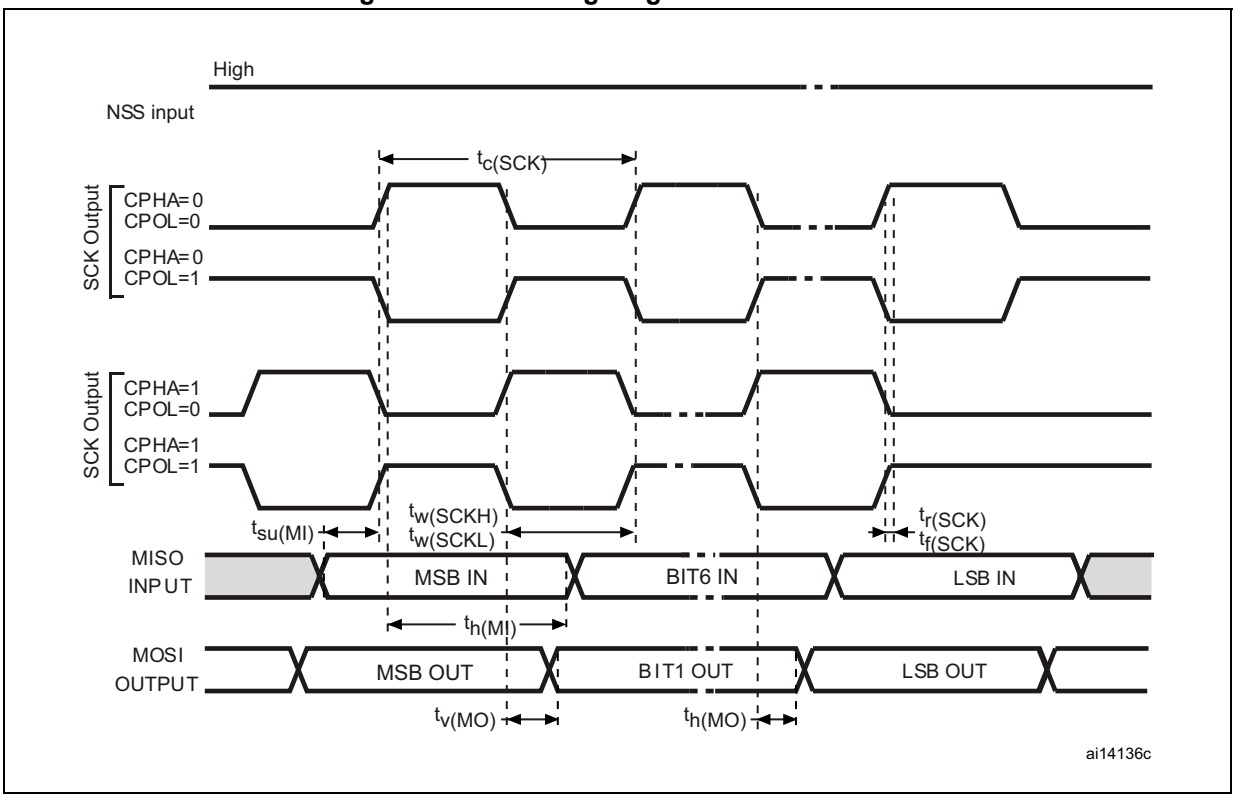
1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)			0.95(2)	1	2.10	MHz
f_{PLLSAI_OUT}	PLLSAI multiplier output clock			-	-	216	MHz
f_{VCO_OUT}	PLLSAI VCO output			100	-	432	MHz
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Main SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLSAI)}$(4)	PLLSAI power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}$(4)	PLLSAI power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Figure 40. SPI timing diagram - master mode



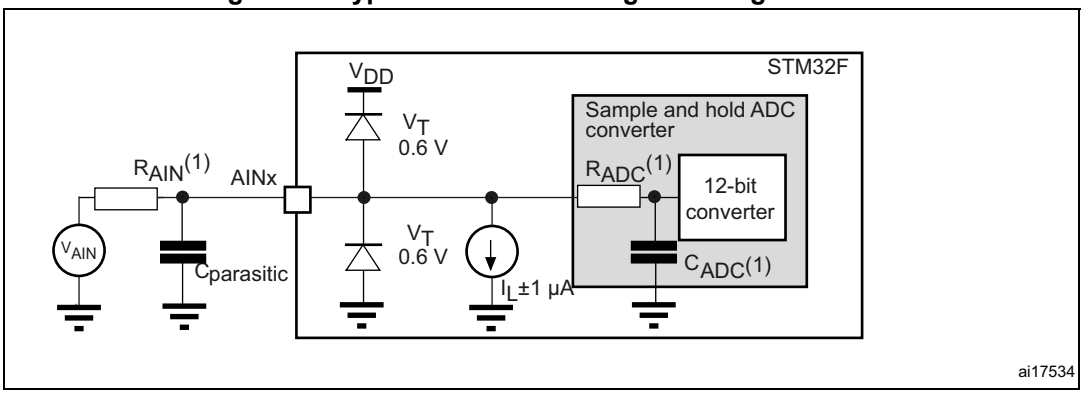
6.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 74* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 17*.

Table 74. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA}-V_{REF+} < 1.2$ V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance		-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
			3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Figure 51. Typical connection diagram using the ADC

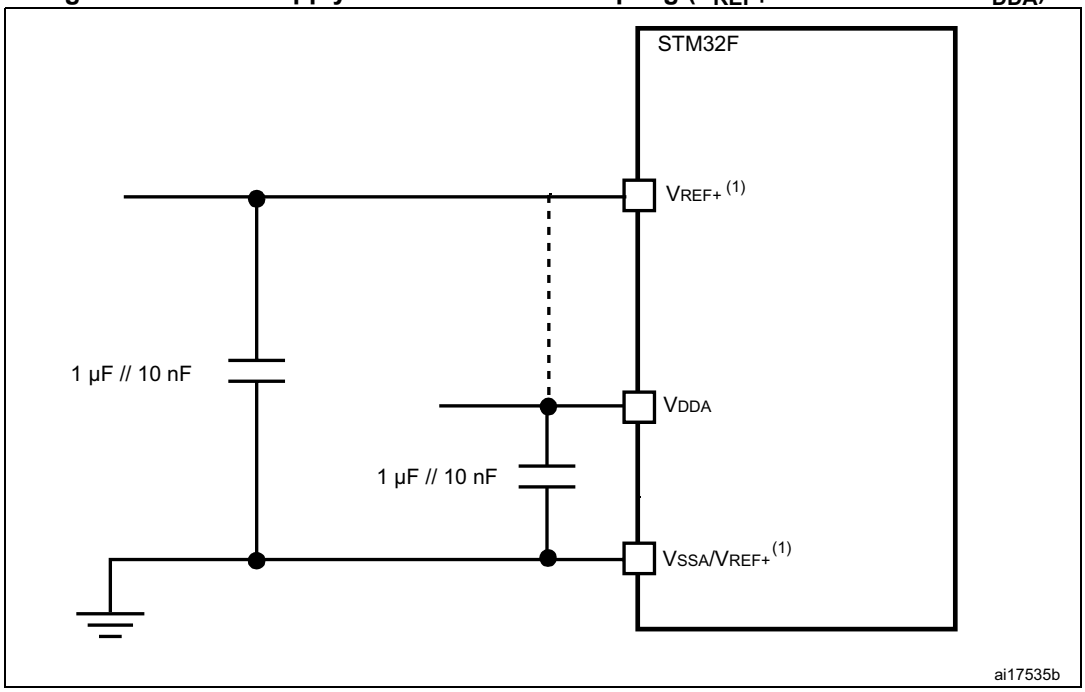


1. Refer to *Table 74* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

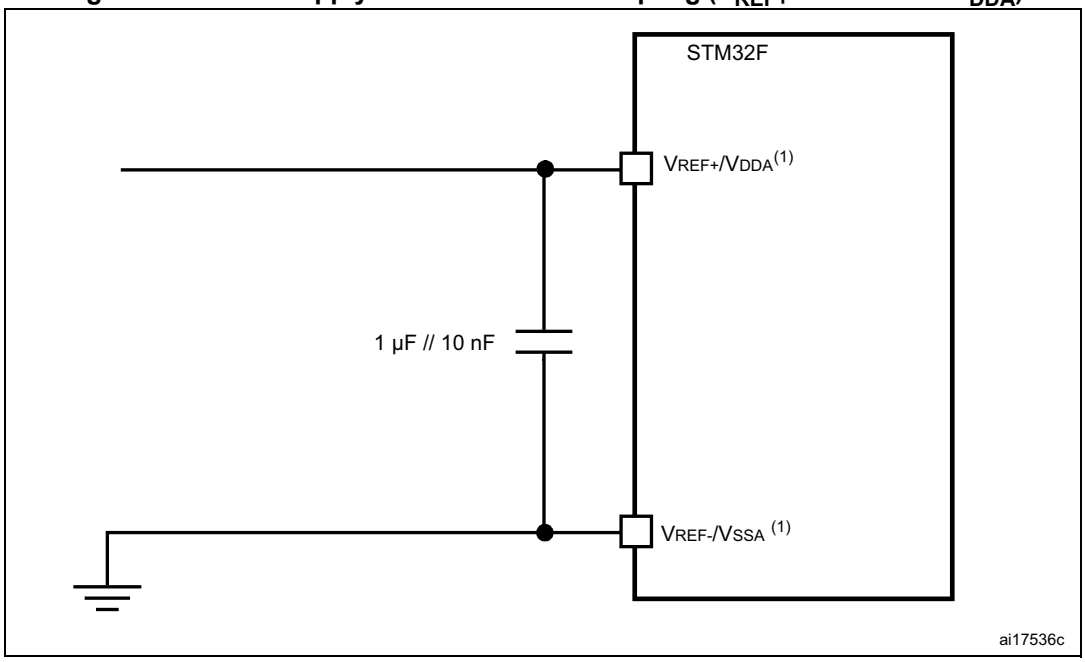
Power supply decoupling should be performed as shown in *Figure 52* or *Figure 53*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 52. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 53. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.22 Temperature sensor characteristics

Table 80. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5		mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76		V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 81. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

Table 95. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, VDD range= 2.7 to 3.6 V	$2T_{HCLK} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	ns
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}	-	ns
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	ns
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	ns
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK}-0.5$	-	ns
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	ns
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	ns
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	ns
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK}-0.5$	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Figure 71. NAND controller waveforms for common memory read access

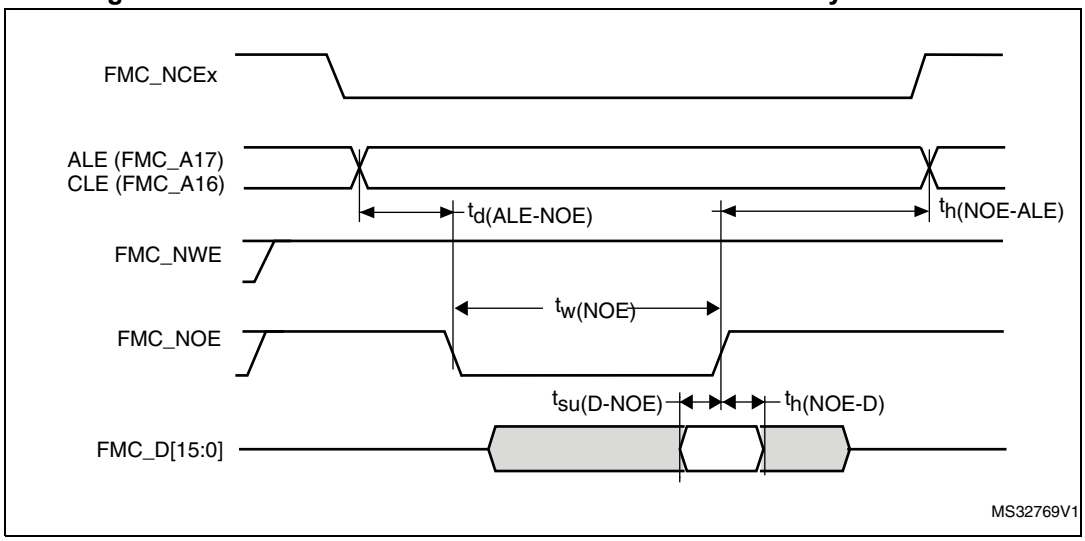


Figure 72. NAND controller waveforms for common memory write access

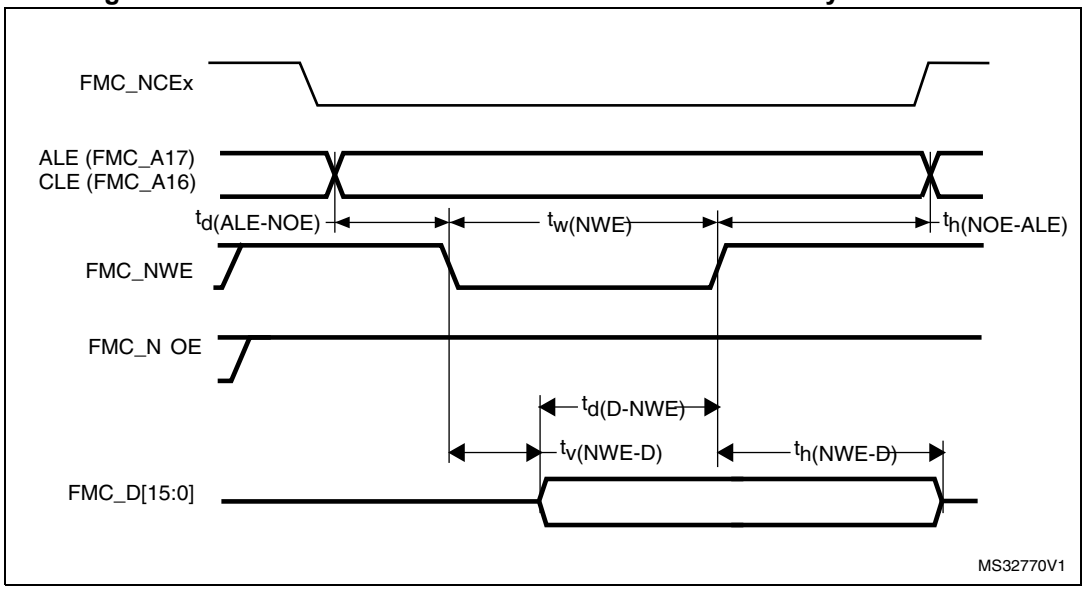


Table 100. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK}+0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	9	-	ns
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	ns
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{HCLK} - 0.5$	ns
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK} - 2$	-	ns

1. C_L = 30 pF.

Table 112. WLCSP143 recommended PCB design rules (0.4 mm pitch)

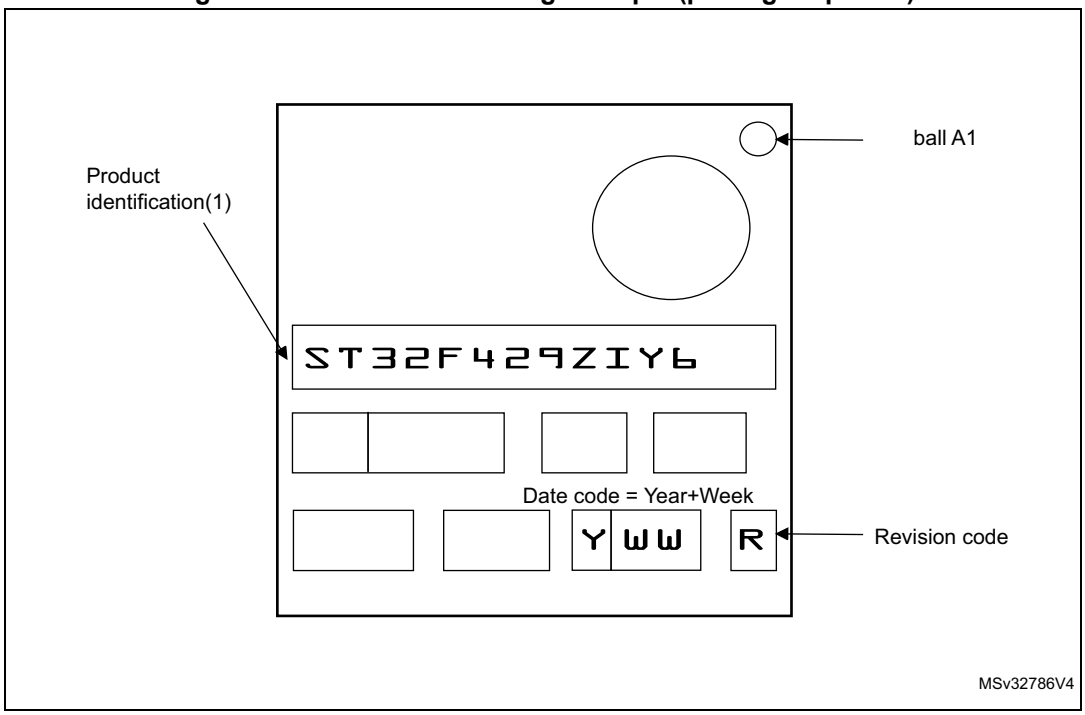
Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Device marking for WLCSP143

The following figure gives an example of topside marking orientation versus ball A 1 identifier location.

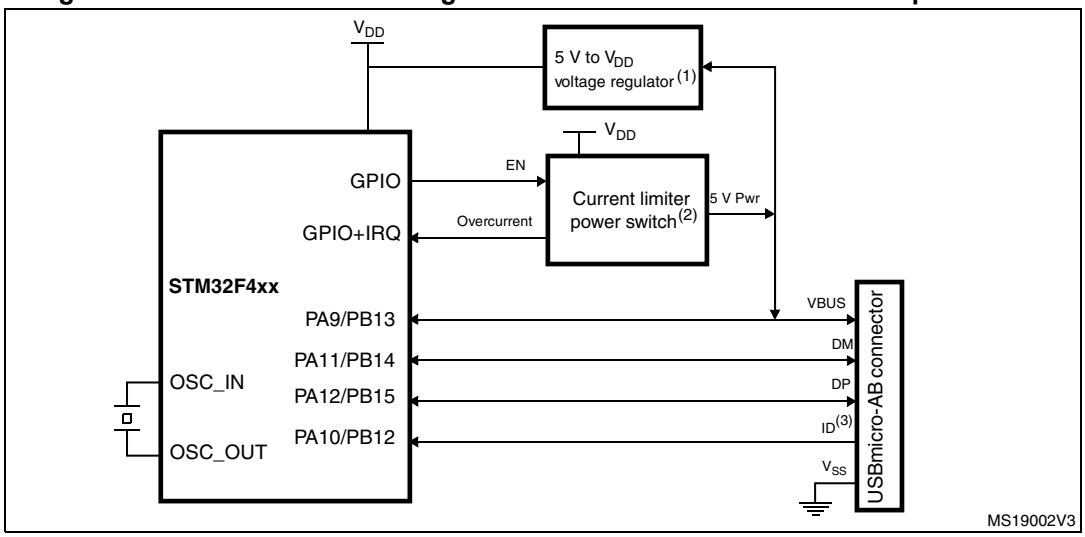
Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 85. WLCSP143 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Figure 105. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Table 124. Document revision history

Date	Revision	Changes
24-Jan-2014	3	Added STM32F429xE part numbers featuring 512 Mbytes of Flash memory and UFBGA169 package. Added LPSDR SDRAM. Changed INTN into INTR in *Figure 4: STM32F427xx and STM32F429xx block diagram*. Added note 4 in *Table 2: STM32F427xx and STM32F429xx features and peripheral counts*. Updated *Section 3.15: Boot modes*. Updated for PA4 and PA5 in *Table 10: STM32F427xx and STM32F429xx pin and ball definitions*. Added V_{IN} for BOOT0 pins in *Table 14: Voltage characteristics*. Updated Note *6.*, added Note *1.*,and updated maximum V_{IN} for B pins in *Table 17: General operating conditions*. Updated maximum Flash memory access frequency with wait states for V_{DD} =1.8 to 2.1 V in *Table 18: Limitations depending on the operating power supply range*. Updated *Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM* and *Table 25: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Table 30: Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), VDD=1.7 V*, *Table 31: Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)*, and *Table 32: Typical current consumption in Sleep mode, regulator ON, VDD=1.7 V*. Updated *Table 57: Output voltage characteristics*. Updated *Table 58: I/O AC characteristics*. Added *Figure 35*. Updated $t_{h(SDA)}$, $t_{r(SDA)}$ and $t_{r(SCL)}$ and added t_{SP} in *Table 61: I^2C characteristics*. Updated f_{SCK} in *Table 62: SPI dynamic characteristics*. Updated *Table 70: Dynamic characteristics: USB ULPI*. Updated *Section 6.3.26: FMC characteristics* conditions. Updated *Figure 73: SDRAM read access waveforms (CL = 1)* and *Figure 74: SDRAM write access waveforms*. Added *Table 103: LPSDR SDRAM read timings* and *Table 105: LPSDR SDRAM write timings*. Updated *Table 102: SDRAM read timings* and *Table 104: SDRAM write timings* and added note *2.Table 108: Dynamic characteristics: SD / MMC characteristics*.