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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429vet6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429vet6tr</a>

Table 1. Device summary

Reference	Part number
STM32F427xx	STM32F427VG, STM32F427ZG, STM32F427IG, STM32F427AG, STM32F427VI, STM32F427ZI, STM32F427II, STM32F427AI
STM32F429xx	STM32F429VG, STM32F429ZG, STM32F429IG, STM32F429BG, STM32F429NG, STM32F429AG, STM32F429VI, STM32F429ZI, STM32F429II,, STM32F429BI, STM32F429NI, STM32F429AI, STM32F429VE, STM32F429ZE, STM32F429IE, STM32F429BE, STM32F429NE

## 3 Functional overview

### 3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F42x family is compatible with all ARM tools and software.

*Figure 4* shows the general block diagram of the STM32F42x family.

*Note:* Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

### 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

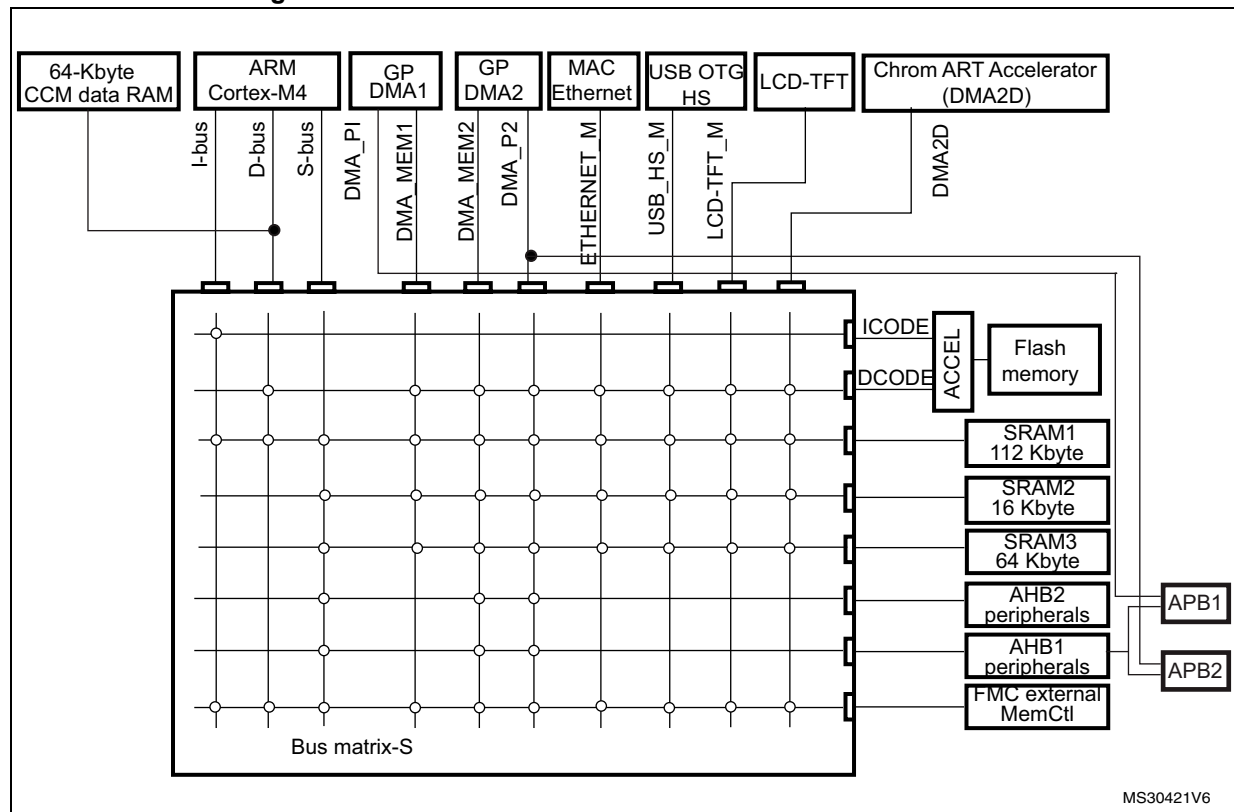
### 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

Figure 5. STM32F427xx and STM32F429xx Multi-AHB matrix



### 3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$  or  $V_{BOR}$ , without the need for an external reset circuit.

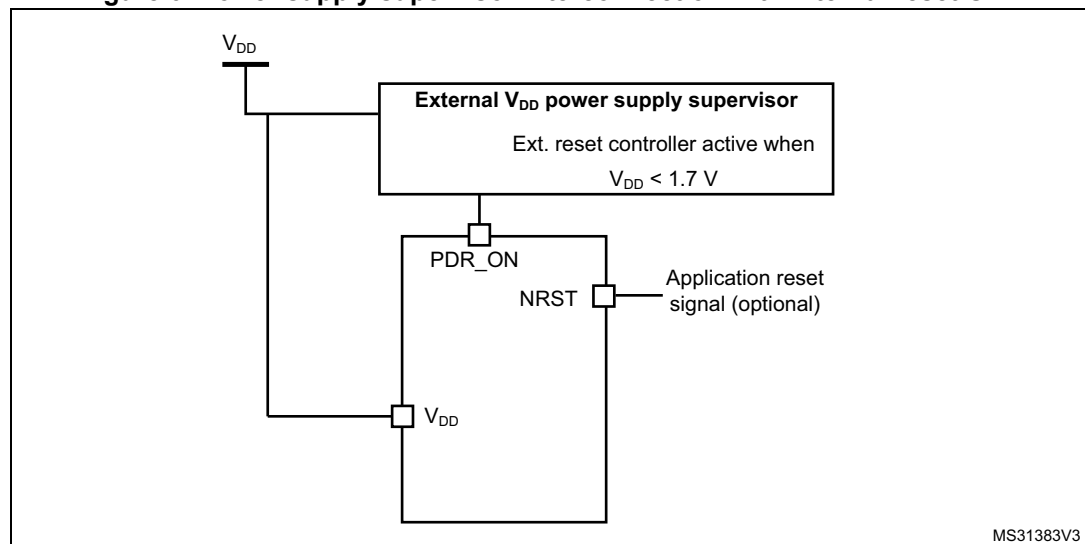
The device also features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR\_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR\_ON pin.

An external power supply supervisor should monitor  $V_{DD}$  and should maintain the device in reset mode as long as  $V_{DD}$  is below a specified threshold. PDR\_ON should be connected to this external power supply supervisor. Refer to [Figure 6: Power supply supervisor interconnection with internal reset OFF](#).

**Figure 6. Power supply supervisor interconnection with internal reset OFF**



The  $V_{DD}$  specified threshold, below which the device must be maintained under reset, is 1.7 V (see [Figure 7](#)).

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- $V_{BAT}$  functionality is no more available and  $V_{BAT}$  pin should be connected to  $V_{DD}$ .

All packages, except for the LQFP100, allow to disable the internal reset through the PDR\_ON signal.

### 3.26 Inter-integrated sound (I<sup>2</sup>S)

Two standard I<sup>2</sup>S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I<sup>2</sup>S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

*Note: For I2S2 full-duplex mode, I2S2\_CK and I2S2\_WS signals can be used only on GPIO Port B and GPIO Port D.*

### 3.27 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

### 3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I<sup>2</sup>S and SAI applications. It allows to achieve error-free I<sup>2</sup>S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I<sup>2</sup>S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I<sup>2</sup>S/SAI flow with an external PLL (or Codec output).

### 3.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

### 3.33 Universal serial bus on-the-go full-speed (OTG\_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of  $320 \times 35$  bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

### 3.34 Universal serial bus on-the-go high-speed (OTG\_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of  $1 \text{ Kbit} \times 35$  with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
4	4	D1	B2	4	D9	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	D2	B3	5	E8	5	B2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	V <sub>SS</sub>	S	-	-	-	-
-	-	-	-	-	-	-	F5	V <sub>DD</sub>	S	-	-	-	-
6	6	E5	C1	6	C11	6	C1	V <sub>BAT</sub>	S	-	-	-	-
-	-	NC (2)	D2	7	-	7	C2	PI8	I/O	FT	(3) (4)	EVENTOUT	TAMP_2
7	7	E4	D1	8	D10	8	D1	PC13	I/O	FT	(3) (4)	EVENTOUT	TAMP_1
8	8	E1	E1	9	D11	9	E1	PC14- OSC32_IN (PC14)	I/O	FT	(3) (4)	EVENTOUT	OSC32_IN (5)
9	9	F1	F1	10	E11	10	F1	PC15- OSC32_OUT (PC15)	I/O	FT	(3) (4)	EVENTOUT	OSC32_OUT <sup>(5)</sup>
-	-	-	-	-	-	-	G5	V <sub>DD</sub>	S	-	-	-	-
-	-	E2	D3	11	-	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	E3	12	-	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	NC (2)	E4	13	-	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	F6	F2	14	E7	14	F2	V <sub>SS</sub>	S	-	-	-	-
-	-	F4	F3	15	E10	15	F4	V <sub>DD</sub>	S	-	-	-	-



Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
-	91	G11	J15	110	G4	133	J15	PG6	I/O	FT	-	FMC_INT2, DCMI_D12, LCD_R7, EVENTOUT	-
-	92	G12	J14	111	H1	134	J14	PG7	I/O	FT	-	USART6_CK, FMC_INT3, DCMI_D13, LCD_CLK, EVENTOUT	-
-	93	F13	H14	112	G2	135	H14	PG8	I/O	FT	-	SPI6_NSS, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT	-
-	94	J7	G12	113	D2	136	G10	V <sub>SS</sub>	S		-	-	-
-	95	E6	H13	114	G1	137	G11	V <sub>DD</sub>	S		-	-	-
63	96	F9	H15	115	F2	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	97	F10	G15	116	F3	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	98	F11	G14	117	E4	140	G14	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-
66	99	F12	F14	118	E3	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, SDIO_D1, DCMI_D3, EVENTOUT	-
67	100	E13	F15	119	F1	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port F	PF8	-	-	-	-	-	SPI5_ MISO	SAI1_ SCK_B	-	-	TIM13_CH1	-	-	FMC_ NIOWR	-	-	EVEN TOUT
	PF9	-	-	-	-	-	SPI5_ MOSI	SAI1_ FS_B	-	-	TIM14_CH1	-	-	FMC_CD	-	-	EVEN TOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FMC_INTR	DCMI_ D11	LCD_DE	EVEN TOUT
	PF11	-	-	-	-	-	SPI5_ MOSI	-	-	-	-	-	-	FMC_ SDNRAS	DCMI_ D12	-	EVEN TOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVEN TOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	EVEN TOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	EVEN TOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	EVEN TOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVEN TOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVEN TOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVEN TOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVEN TOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/ FMC_BA0	-	-	EVEN TOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVEN TOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FMC_INT2	DCMI_ D12	LCD_R7	EVEN TOUT
	PG7	-	-	-	-	-	-	-	-	USART6_ CK	-	-	-	FMC_INT3	DCMI_ D13	LCD_CLK	EVEN TOUT
	PG8	-	-	-	-	-	SPI6_ NSS	-	-	USART6_ RTS	-	-	ETH_PPS_ OUT	FMC_SDC LK	-	-	EVEN TOUT

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4008 0000 - 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00 - 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	DMA2D
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	Reserved
	0x4002 6800 - 0x4002 7FFF	
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

**Table 22. reset and power control block characteristics (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{RUSH}^{(1)}$	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
$E_{RUSH}^{(1)}$	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	$V_{DD} = 1.7\text{ V}$ , $T_A = 105\text{ }^{\circ}\text{C}$ , $I_{RUSH} = 171\text{ mA}$ for $31\text{ }\mu\text{s}$	-	-	5.4	$\mu\text{C}$

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from  $V_{BAT}$ ) to the instant when first instruction is read by the user application code.

### 6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in [Table 23](#). They are subject to general operating conditions for  $T_A$ .

**Table 23. Over-drive switching characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	$\mu\text{s}$
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

**Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)**

Symbol	Parameter	Conditions	f <sub>HCLK</sub> (MHz)	Typ	Max <sup>(1)</sup>			Unit
					TA=25 °C	TA=85 °C	TA=105 °C	
I <sub>DD</sub>	Supply current in RUN mode	All Peripherals enabled <sup>(2)(3)</sup>	180	103	112	140	151	mA
			168	98	107	126	144	
			150	87	95	112	128	
			144	85	92	108	124	
			120	66	71	85	99	
			90	54	58	69	80	
			60	37	39	47	55	
			30	20	24	39	51	
			25	17	21	35	48	
			16	12	16	30	42	
			8	7	11	24	37	
			4	5	8	22	35	
			2	3	7	21	34	
		All Peripherals disabled <sup>(3)</sup>	180	57	62	87	106	
			168	50	54	76	93	
			150	46	50	70	86	
			144	45	49	68	84	
			120	36	41	56	69	
			90	29	34	46	57	
			60	21	24	33	41	
			30	13	17	31	44	
			25	11	15	28	41	
			16	8	12	25	38	
			8	5	9	23	35	
			4	4	7	21	34	
			2	3	6.5	20	33	

1. Guaranteed by characterization unless otherwise specified.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

3. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Figure 25. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/backup RAM OFF)

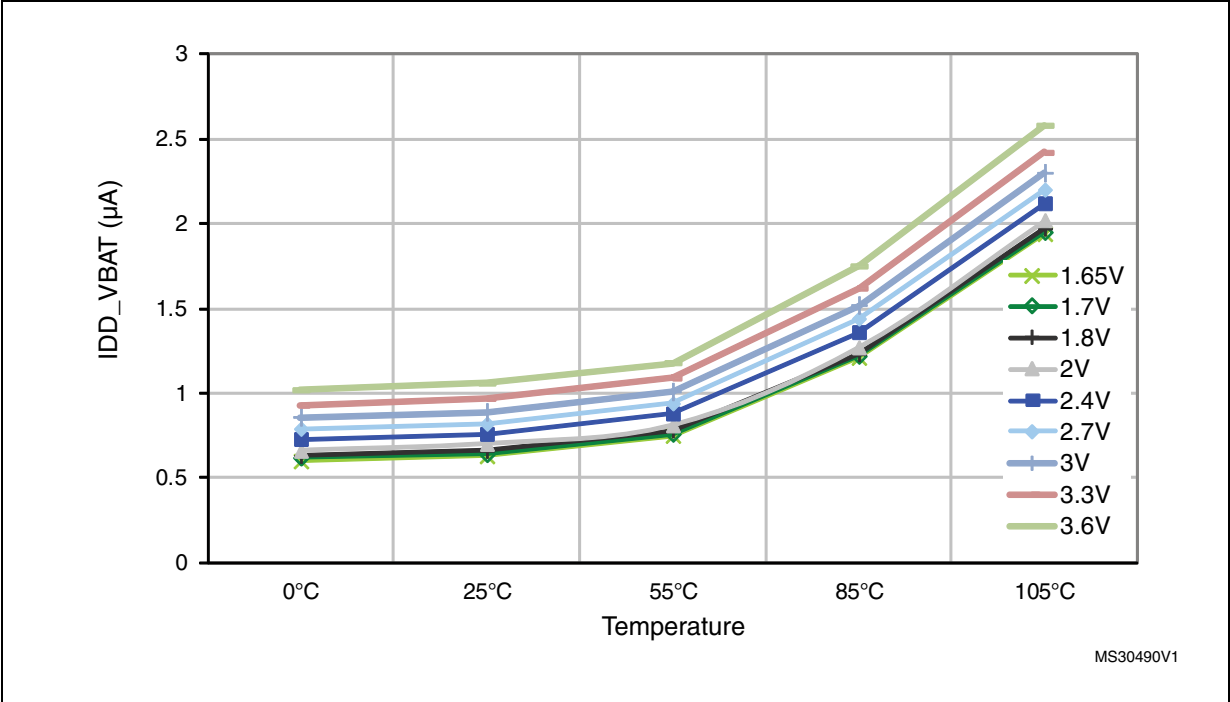
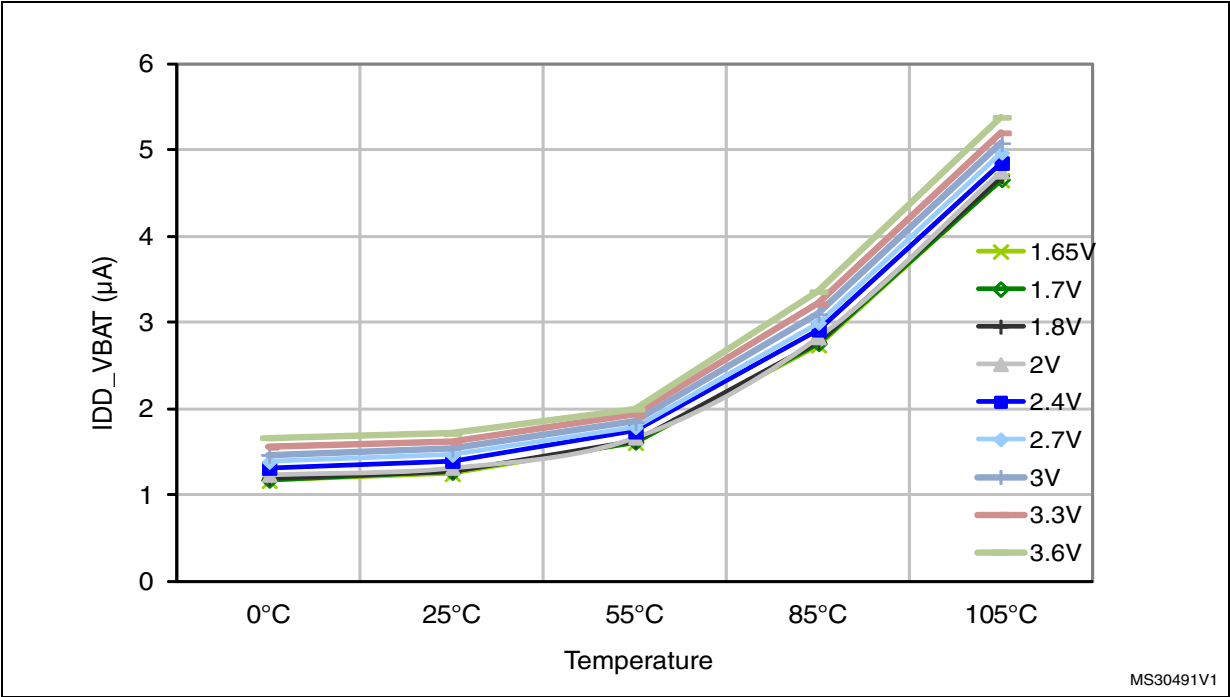


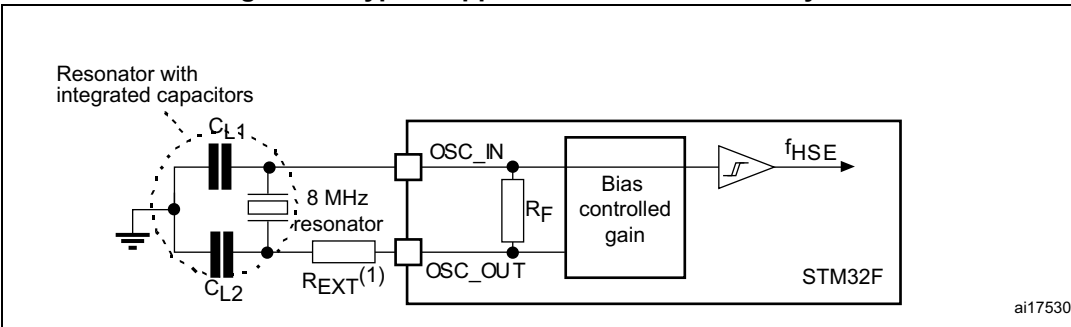
Figure 26. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/backup RAM ON)



For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 29](#)).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ .

**Note:** For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).

**Figure 29. Typical application with an 8 MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz) <sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_F$	Feedback resistor		-	18.4	-	MΩ
$I_{DD}$	LSE current consumption		-	-	1	μA
$ACC_{LSE}^{(2)}$	LSE accuracy		- 500	-	500	ppm
$G_{m\_crit\_max}$	Maximum critical crystal $g_m$	Startup	-	-	0.56	μA/V
$t_{SU(LSE)}^{(3)}$	startup time	$V_{DD}$ is stabilized	-	2	-	s

- Guaranteed by design.
- This parameter depends on the crystal used in the application. Refer to application note AN2867.
- $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Note:** For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).

Table 62. SPI dynamic characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$	SCK high and low time	Master mode, SPI presc = 2, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	$T_{PCLK} - 0.5$	$T_{PCLK}$	$T_{PCLK} + 0.5$	ns
$t_{w(SCKL)}$		Master mode, SPI presc = 2, $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	$T_{PCLK} - 2$	$T_{PCLK}$	$T_{PCLK} + 2$	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4T_{PCLK}$	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	0	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	0.5	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode, SPI presc = 2	0	-	$4T_{PCLK}$	
$t_{dis(SO)}$	Data output disable time	Slave mode, SPI1/4/5/6, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	0	-	8.5	
		Slave mode, SPI1/2/3/4/5/6 and $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	0	-	16.5	
$t_{v(SO)}$ $t_{h(SO)}$	Data output valid/hold time	Slave mode (after enable edge), SPI1/4/5/6 and $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	11	13	ns
		Slave mode (after enable edge), SPI2/3, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	14	15	
		Slave mode (after enable edge), SPI1/4/5/6, $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	15.5	19	
		Slave mode (after enable edge), SPI2/3, $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	15.5	17.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge), SPI1/4/5/6, $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	2.5	
		Master mode (after enable edge), SPI1/2/3/4/5/6, $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	4.5	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed by characterization results.

2. Maximum frequency in Slave transmitter mode is determined by the sum of  $t_{v(SO)}$  and  $t_{su(MI)}$  which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su(MI)} = 0$  while Duty(SCK) = 50%



Table 74. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_S^{(2)}$	Sampling rate ( $f_{ADC} = 30$ MHz, and $t_S = 3$ ADC cycles)	12-bit resolution Single ADC	-	-	2	Msp/s
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msp/s
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msp/s
$I_{VREF+}^{(2)}$	ADC $V_{REF}$ DC current consumption in conversion mode		-	300	500	$\mu A$
$I_{VDDA}^{(2)}$	ADC $V_{DDA}$ DC current consumption in conversion mode		-	1.6	1.8	mA

- $V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
- Guaranteed by characterization results.
- $V_{REF+}$  is internally connected to  $V_{DDA}$  and  $V_{REF-}$  is internally connected to  $V_{SSA}$ .
- $R_{ADC}$  maximum value is given for  $V_{DD}=1.7$  V, and minimum value for  $V_{DD}=3.3$  V.
- For external triggers, a delay of  $1/f_{PCLK2}$  must be added to the latency specified in [Table 74](#).

**Equation 1:  $R_{AIN}$  max formula**

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB.  $N = 12$  (from 12-bit resolution) and  $k$  is the number of sampling periods defined in the ADC\_SMPR1 register.

Table 75. ADC static accuracy at  $f_{ADC} = 18$  MHz

Symbol	Parameter	Test conditions	Typ	Max <sup>(1)</sup>	Unit
ET	Total unadjusted error	$f_{ADC} = 18$ MHz $V_{DDA} = 1.7$ to $3.6$ V $V_{REF} = 1.7$ to $3.6$ V $V_{DDA} - V_{REF} < 1.2$ V	$\pm 3$	$\pm 4$	LSB
EO	Offset error		$\pm 2$	$\pm 3$	
EG	Gain error		$\pm 1$	$\pm 3$	
ED	Differential linearity error		$\pm 1$	$\pm 2$	
EL	Integral linearity error		$\pm 2$	$\pm 3$	

- Guaranteed by characterization results.

### 6.3.26 FMC characteristics

Unless otherwise specified, the parameters given in [Table 86](#) to [Table 101](#) for the FMC interface are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 10$  except at  $V_{DD}$  range 1.7 to 2.1V where  $OSPEEDRy[1:0] = 11$
- Measurement points are done at CMOS levels:  $0.5V_{DD}$

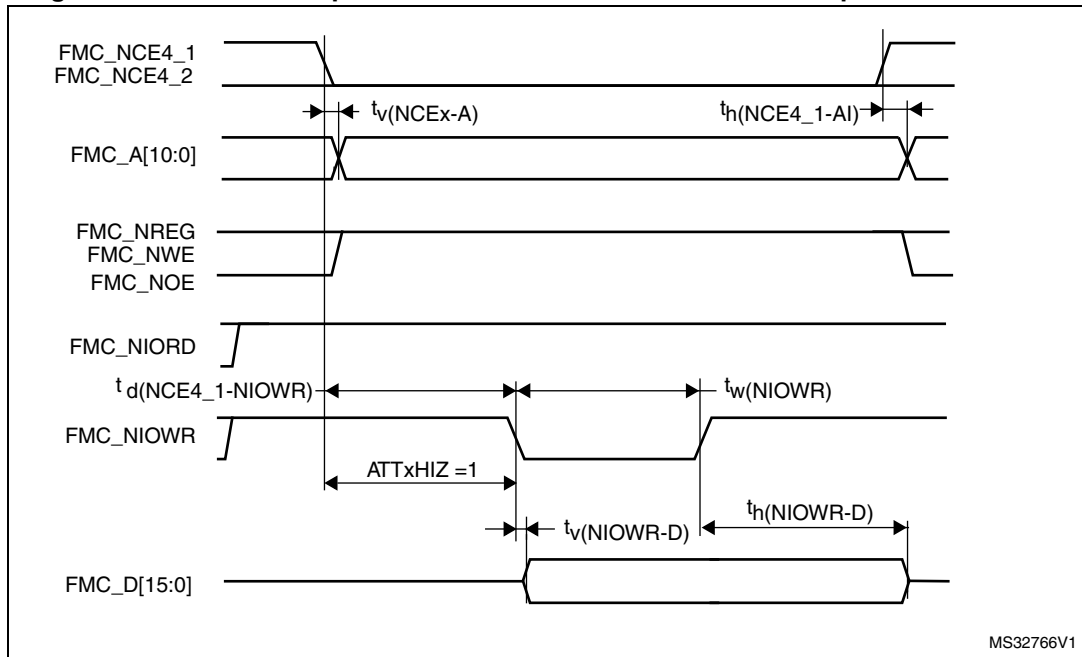
Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

#### Asynchronous waveforms and timings

[Figure 55](#) through [Figure 58](#) represent asynchronous waveforms and [Table 86](#) through [Table 93](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- For SDRAM memories,  $V_{DD}$  ranges from 2.7 to 3.6 V and maximum frequency FMC\_SDCLK = 90 MHz
- For Mobile LPDDR SDRAM memories,  $V_{DD}$  ranges from 1.7 to 1.95 V and maximum frequency FMC\_SDCLK = 84 MHz

Figure 68. PC Card/CompactFlash controller waveforms for I/O space write access

Table 98. Switching characteristics for PC Card/CF read and write cycles in attribute/common space<sup>(1)(2)</sup>

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FMC_Ncex low to FMC_Ay valid	-	0	ns
$t_{h(NCEx-AI)}$	FMC_NCEx high to FMC_Ax invalid	0	-	ns
$t_{d(NREG-NCEx)}$	FMC_NCEx low to FMC_NREG valid	-	1	ns
$t_{h(NCEx-NREG)}$	FMC_NCEx high to FMC_NREG invalid	$T_{HCLK} - 2$	-	ns
$t_{d(NCEx-NWE)}$	FMC_NCEx low to FMC_NWE low	-	$5T_{HCLK}$	ns
$t_{w(NWE)}$	FMC_NWE low width	$8T_{HCLK} - 0.5$	$8T_{HCLK} + 0.5$	ns
$t_{d(NWE-NCEx)}$	FMC_NWE high to FMC_NCEx high	$5T_{HCLK} + 1$	-	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15:0] invalid	$9T_{HCLK} - 0.5$	-	ns
$t_{d(D-NWE)}$	FMC_D[15:0] valid before FMC_NWE high	$13T_{HCLK} - 3$	-	ns
$t_{d(NCEx-NOE)}$	FMC_NCEx low to FMC_NOE low	-	$5T_{HCLK}$	ns
$t_{w(NOE)}$	FMC_NOE low width	$8T_{HCLK} - 0.5$	$8T_{HCLK} + 0.5$	ns
$t_{d(NOE-NCEx)}$	FMC_NOE high to FMC_NCEx high	$5T_{HCLK} - 1$	-	ns
$t_{su(D-NOE)}$	FMC_D[15:0] valid data before FMC_NOE high	$T_{HCLK}$	-	ns
$t_{h(NOE-D)}$	FMC_NOE high to FMC_D[15:0] invalid	0	-	ns

1.  $C_L = 30$  pF.

2. Guaranteed by characterization results.



**Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

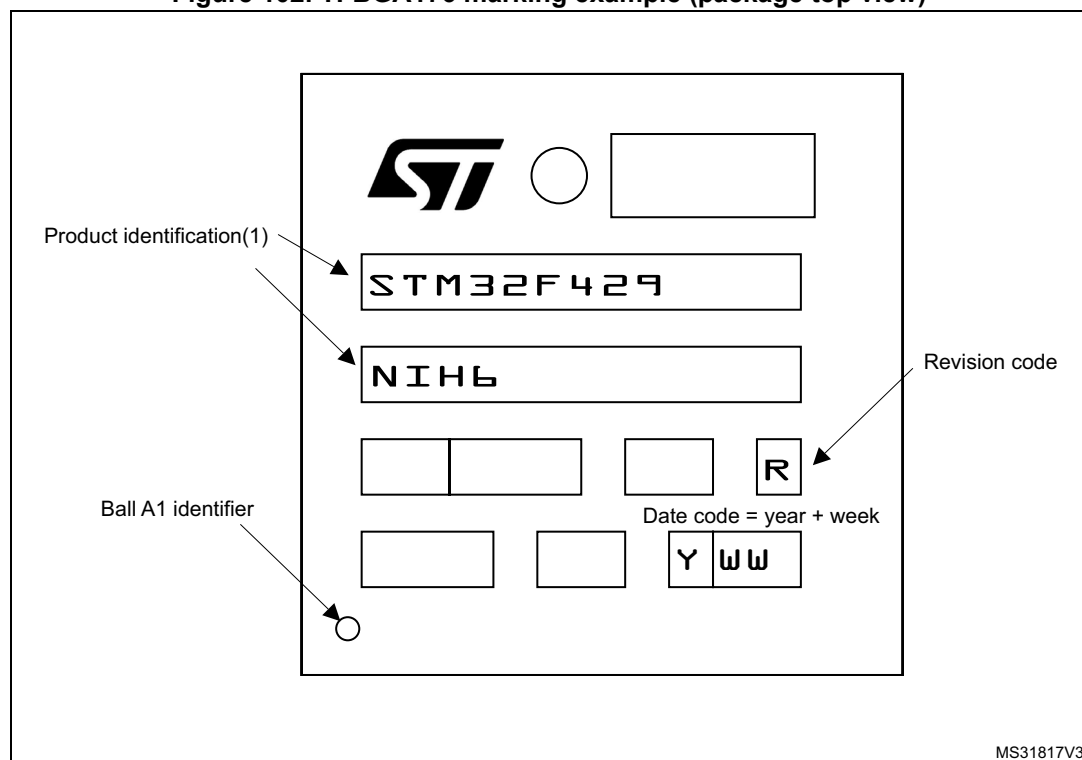
1. Values in inches are converted from mm and rounded to 4 decimal digits.

### Device marking for TFBGA176

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

**Figure 102. TFBGA176 marking example (package top view)**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.