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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429vit6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429vit6</a>

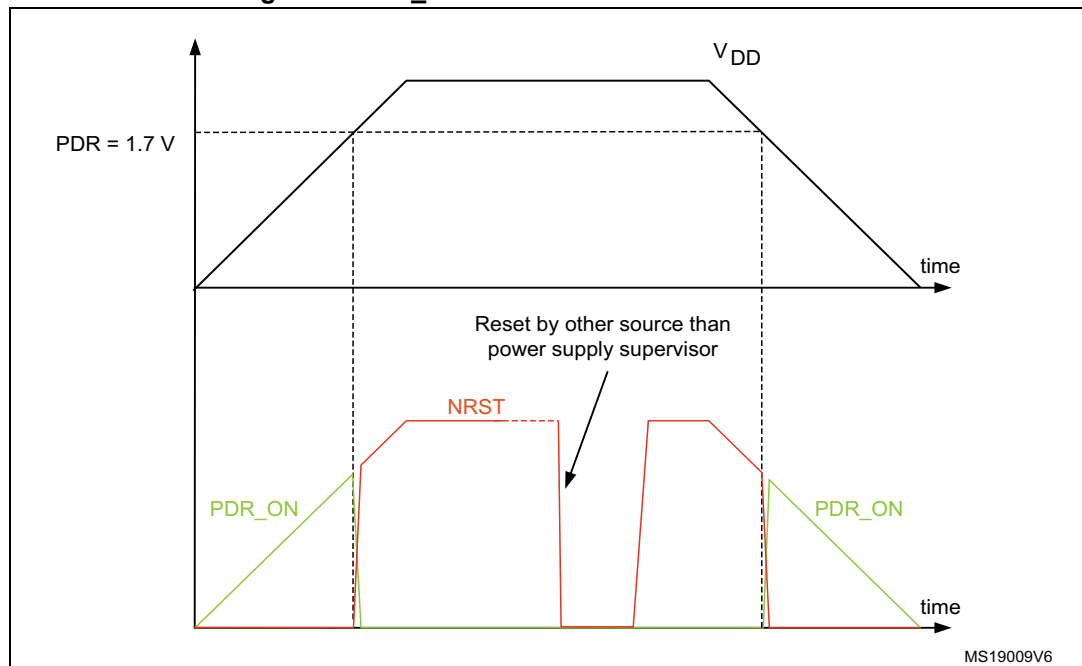
# 1 Introduction

This datasheet provides the description of the STM32F427xx and STM32F429xx line of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F427xx and STM32F429xx datasheet should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex<sup>®</sup>-M4 core, please refer to the Cortex<sup>®</sup>-M4 programming manual (PM0214), available from [www.st.com](http://www.st.com).

Figure 7. PDR\_ON control with internal reset OFF



### 3.18 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

#### 3.18.1 Regulator ON

On packages embedding the BYPASS\_REG pin, the regulator is enabled by holding BYPASS\_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode
 

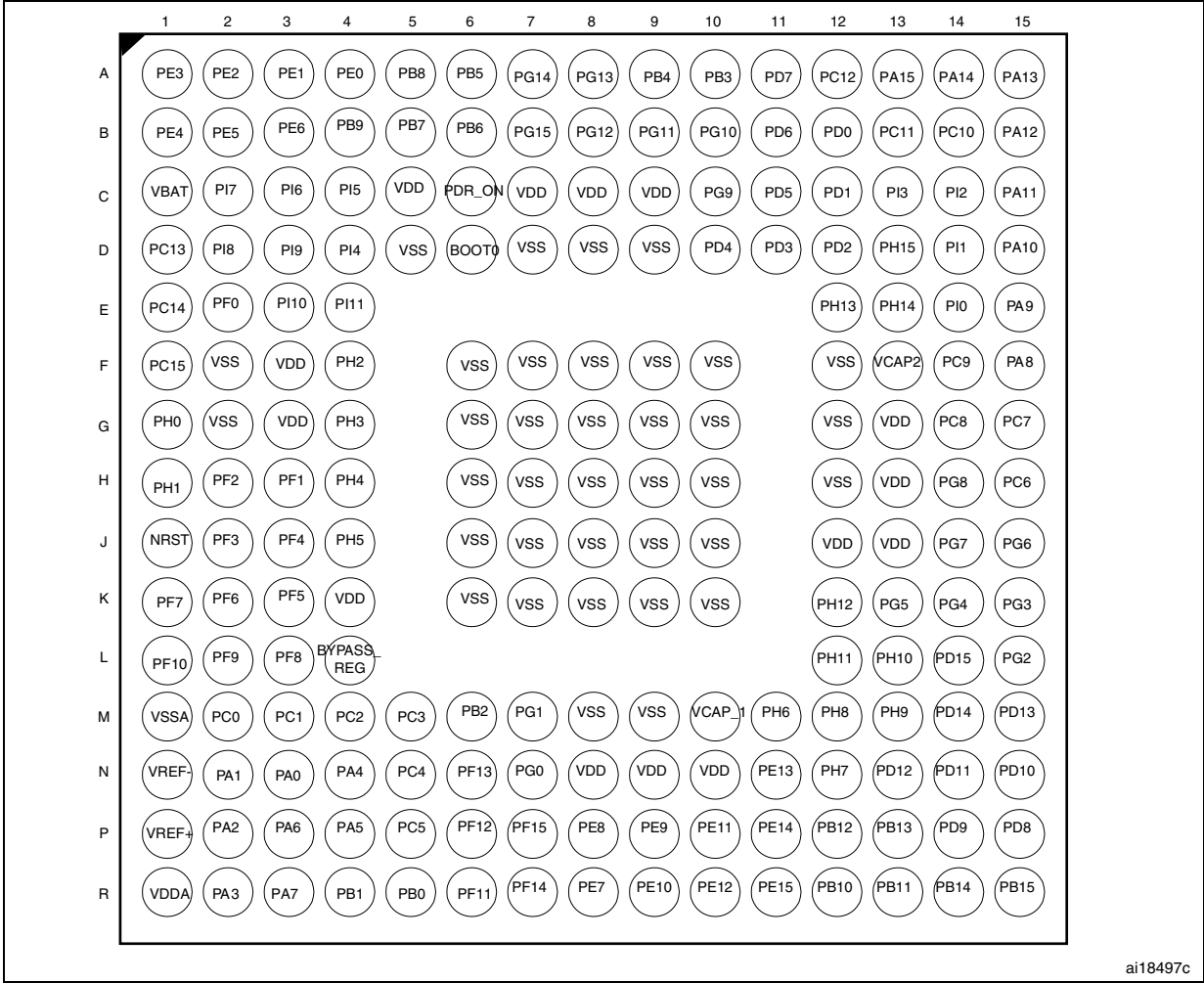
The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) <sup>(1)</sup>
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	90	180
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	90	180
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	90	180
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	45	90/180
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	45	90/180
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	45	90/180

1. The maximum timer clock is either 90 or 180 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.

Figure 17. STM32F42x UFBGA176 ballout



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1. The above figure shows the package top view.

## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ }^{\circ}\text{C}$  and  $T_A = T_{A\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$  (for the  $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\sigma$ ).

#### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 20](#).

#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 21](#).

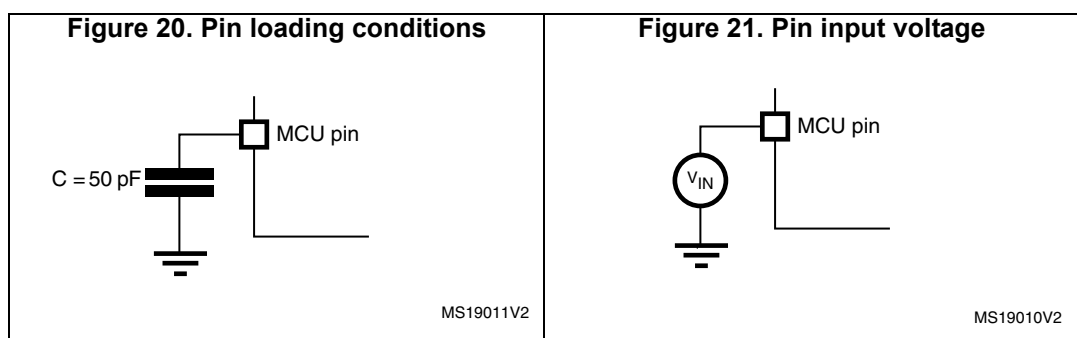


Table 27. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>				Unit
			T <sub>A</sub> = 25 °C	V <sub>DD</sub> = 3.6 V				
				T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C		
I <sub>DD_STOP_NM</sub> (normal mode)	Supply current in Stop mode with voltage regulator in main regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.40	1.50	14.00	25.00	mA	
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.35	1.50	14.00	25.00		
	Supply current in Stop mode with voltage regulator in Low Power regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.29	1.10	10.00	18.00		
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.23	1.10	10.00	18.00		
I <sub>DD_STOP_UDM</sub> (under-drive mode)	Supply current in Stop mode with voltage regulator in main regulator and under-drive mode	Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.19	0.50	6.00	9.00		
	Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode	Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.10	0.40	4.00	7.00		

1. Data based on characterization, tested in production.

Figure 25. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/backup RAM OFF)

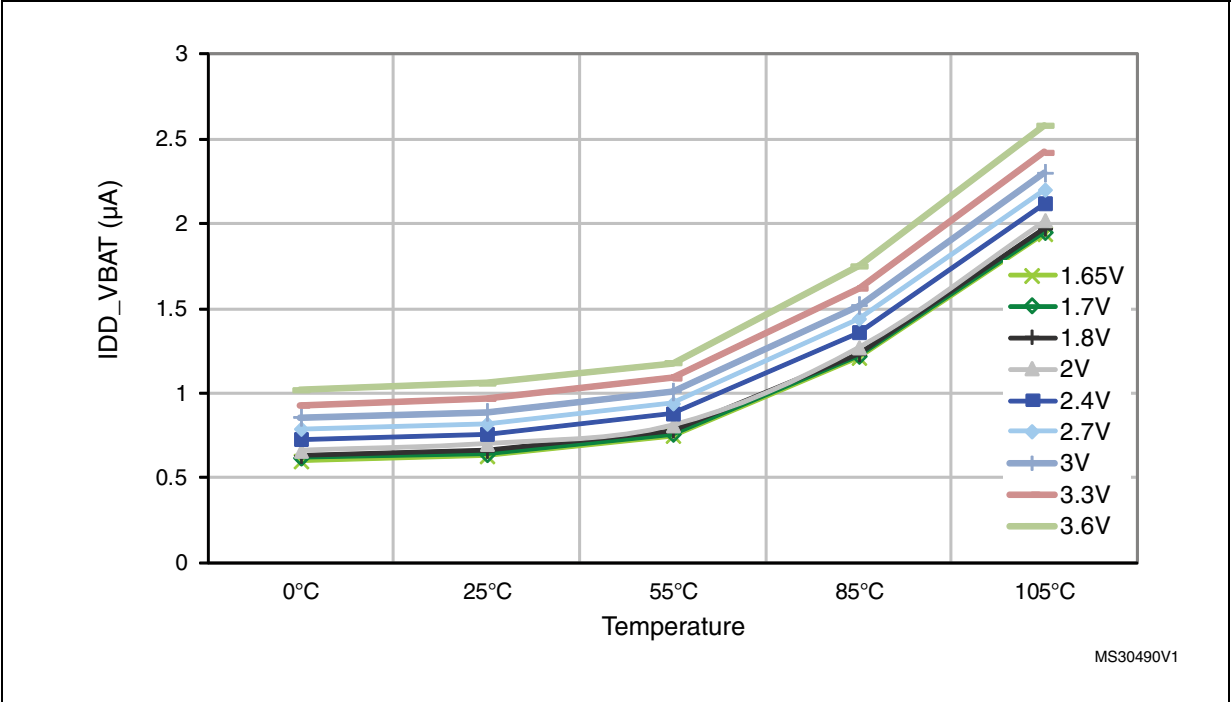


Figure 26. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/backup RAM ON)

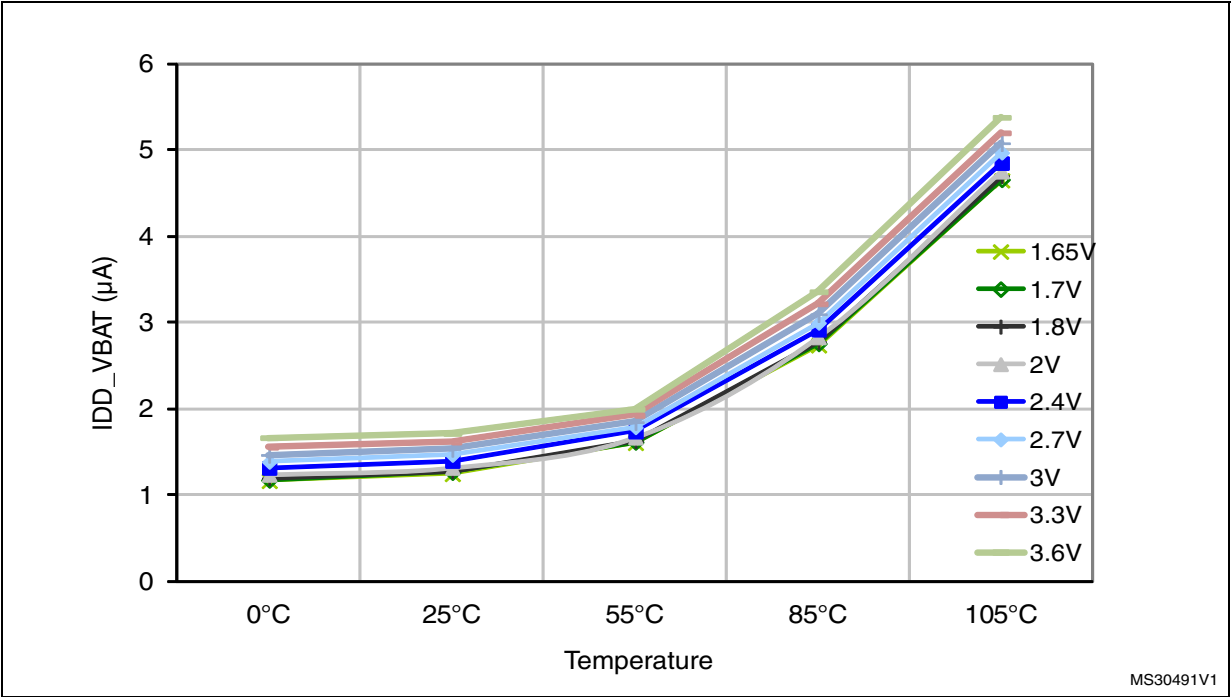
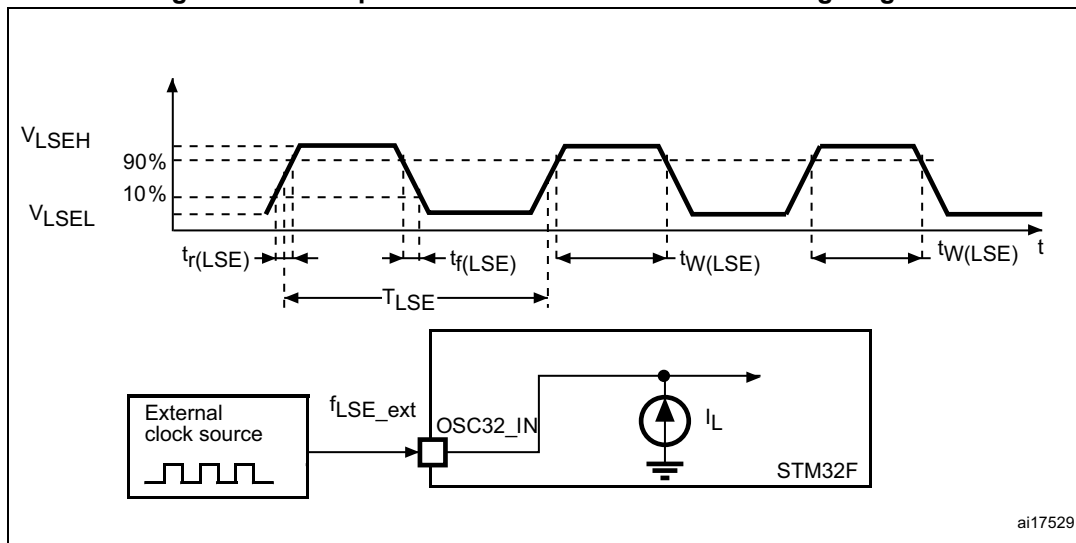




Figure 28. Low-speed external clock source AC timing diagram



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### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 39](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. HSE 4-26 MHz oscillator characteristics <sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	-	26	MHz
$R_F$	Feedback resistor		-	200	-	k $\Omega$
$I_{DD}$	HSE current consumption	$V_{DD}=3.3\text{ V}$ , ESR= 30 $\Omega$ , $C_L=5\text{ pF}@25\text{ MHz}$	-	450	-	$\mu\text{A}$
		$V_{DD}=3.3\text{ V}$ , ESR= 30 $\Omega$ , $C_L=10\text{ pF}@25\text{ MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy		- 500	-	500	ppm
$G_{m\_crit\_max}$	Maximum critical crystal $g_m$	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	$V_{DD}$ is stabilized	-	2	-	ms

1. Guaranteed by design.

2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.

3.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

### 6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 52: EMI characteristics](#)). It is available only on the main PLL.

**Table 46. SSCG parameters constraint**

Symbol	Parameter	Min	Typ	Max <sup>(1)</sup>	Unit
$f_{Mod}$	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15} - 1$	-

1. Guaranteed by design.

#### Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL\_IN}} / (4 \times f_{\text{Mod}})]$$

$f_{\text{PLL\_IN}}$  and  $f_{\text{Mod}}$  must be expressed in Hz.

As an example:

If  $f_{\text{PLL\_IN}} = 1 \text{ MHz}$ , and  $f_{\text{MOD}} = 1 \text{ kHz}$ , the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

#### Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLLN}] / (100 \times 5 \times \text{MODEPER})$$

$f_{\text{VCO\_OUT}}$  must be expressed in MHz.

With a modulation depth (md) =  $\pm 2\%$  (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240] / (100 \times 5 \times 250) = 126 \text{md}(\text{quantitized})\%$$

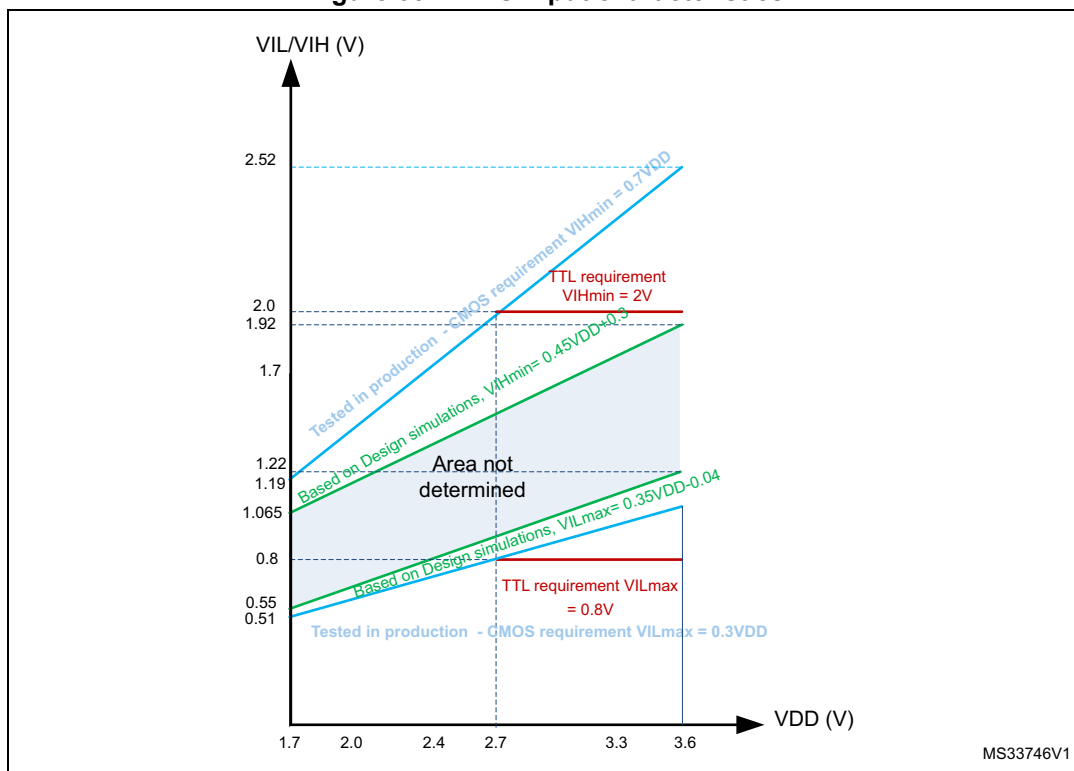
An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLLN})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

Figure 35. FT I/O input characteristics



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ) except PC13, PC14, PC15 and PI8 which can sink or source up to  $\pm 3$  mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#). In particular:

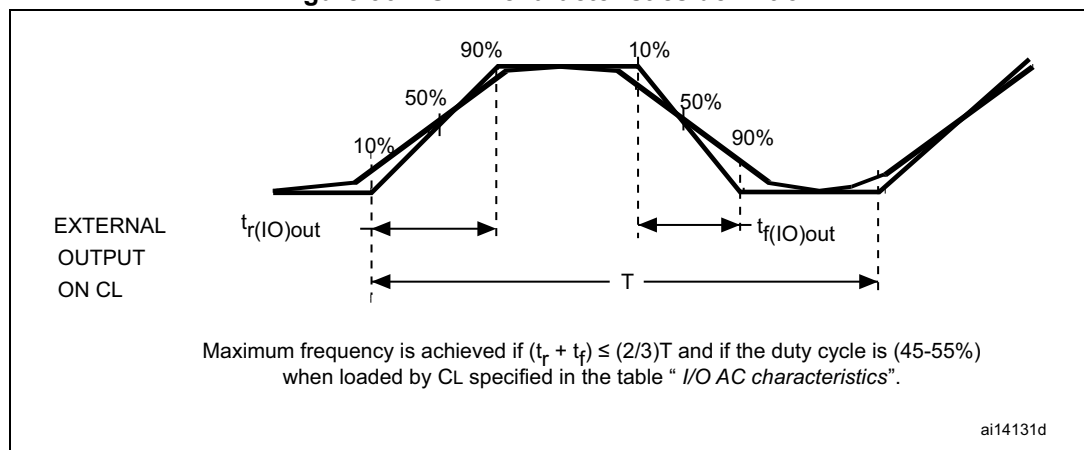
- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 15](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 15](#)).

Table 58. I/O AC characteristics<sup>(1)(2)</sup> (continued)

OSPEEDRy [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(3)</sup>	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 <sup>(4)</sup>	MHz
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	180 <sup>(4)</sup>	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	100	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	72.5	
	$t_{f(\text{IO})\text{out}} /$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	ns
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	6	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	7	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	2.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	3.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx\_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in [Figure 36](#).
4. For maximum frequencies above 50 MHz and  $V_{DD} > 2.4 \text{ V}$ , the compensation cell should be used.

Figure 36. I/O AC characteristics definition



### 6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 56: I/O static characteristics](#)).

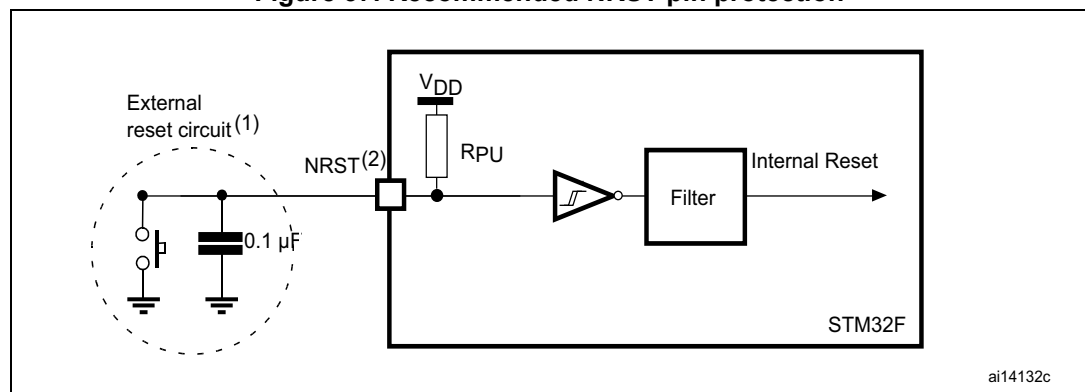
Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#).

**Table 59. NRST pin characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{PU}$	Weak pull-up equivalent resistor <sup>(1)</sup>	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$V_{DD} > 2.7\text{ V}$	300	-	-	ns
$T_{NRST\_OUT}$	Generated reset pulse duration	Internal Reset source	20	-	-	$\mu s$

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

**Figure 37. Recommended NRST pin protection**



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 59](#). Otherwise the reset is not taken into account by the device.

Figure 38. SPI timing diagram - slave mode and CPHA = 0

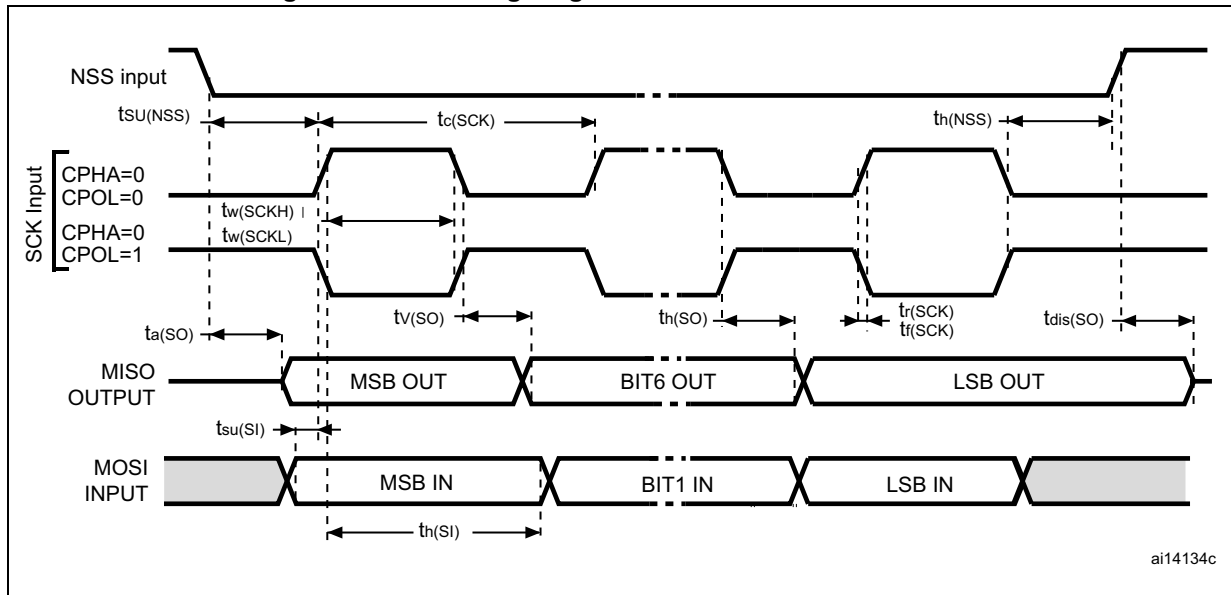
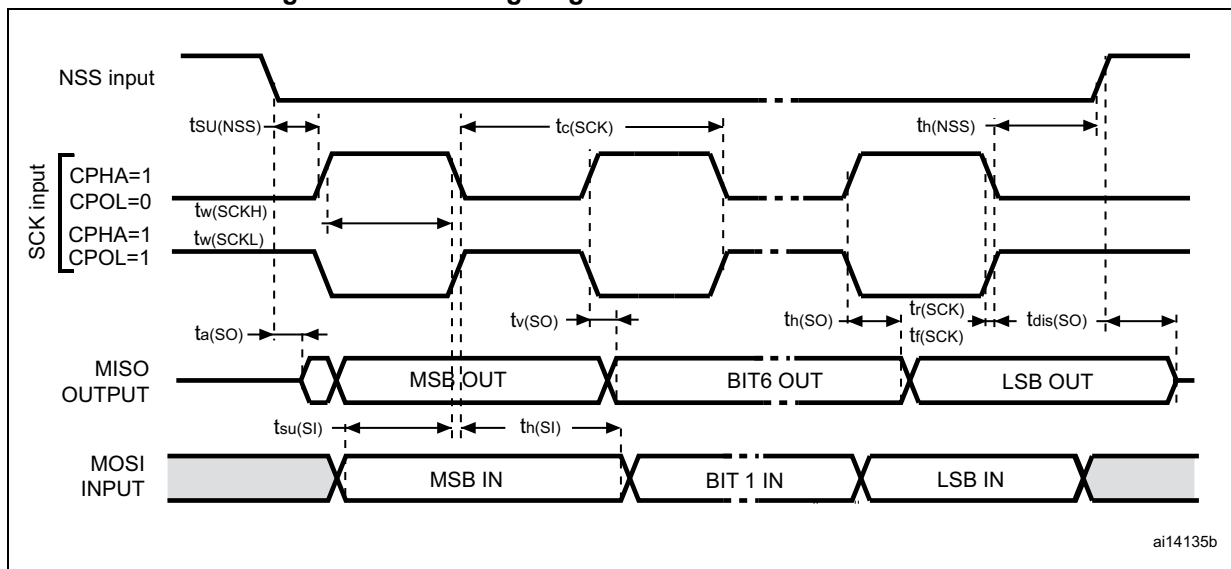


Figure 39. SPI timing diagram - slave mode and CPHA = 1



### Ethernet characteristics

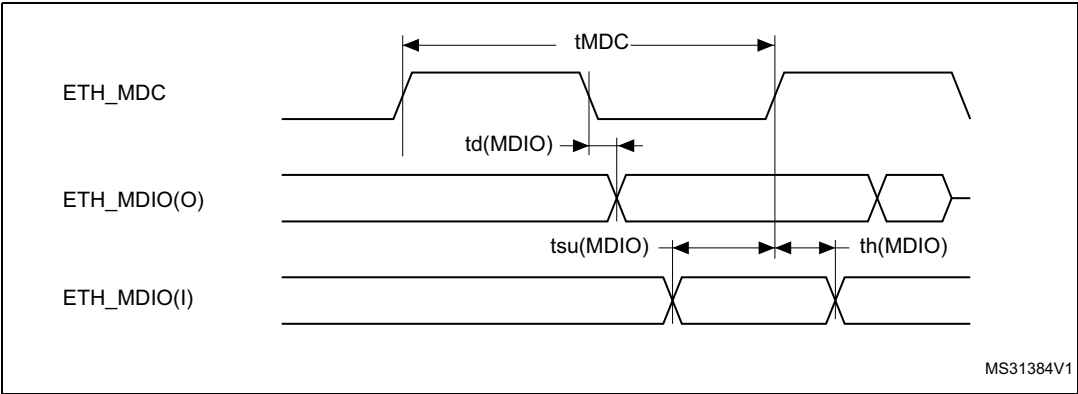
Unless otherwise specified, the parameters given in [Table 71](#), [Table 72](#) and [Table 73](#) for SMI, RMII and MII are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency summarized in [Table 17](#) with the following configuration:

- Output speed is set to  $OSPEEDRy[1:0] = 10$
- Capacitive load  $C = 30 \text{ pF}$  for  $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$
- Capacitive load  $C = 20 \text{ pF}$  for  $1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$
- Measurement points are done at CMOS levels:  $0.5V_{DD}$ .

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

[Table 71](#) gives the list of Ethernet MAC signals for the SMI (station management interface) and [Figure 47](#) shows the corresponding timing diagram.

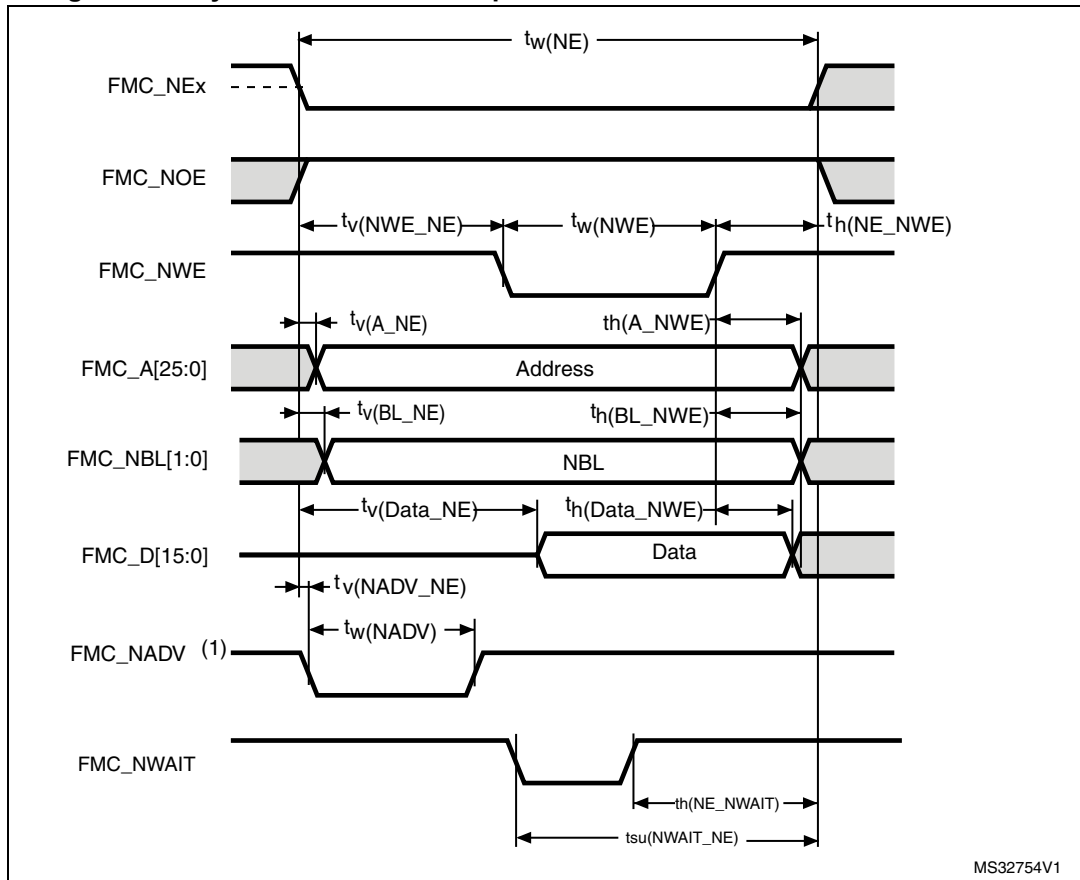
**Figure 47. Ethernet SMI timing diagram**



**Table 71. Dynamics characteristics: Ethernet MAC signals for SMI<sup>(1)</sup>**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{MDC}$	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_d(MDIO)$	Write data valid time	6	10	13	
$t_{su}(MDIO)$	Read data setup time	12	-	-	
$t_h(MDIO)$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

**Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**

1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

**Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$T_{HCLK}$	$T_{HCLK}+0.5$	ns
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} + 1.5$	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+2$	ns
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	ns
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+0.5$	ns

1.  $C_L = 30$  pF.

2. Guaranteed by characterization results.

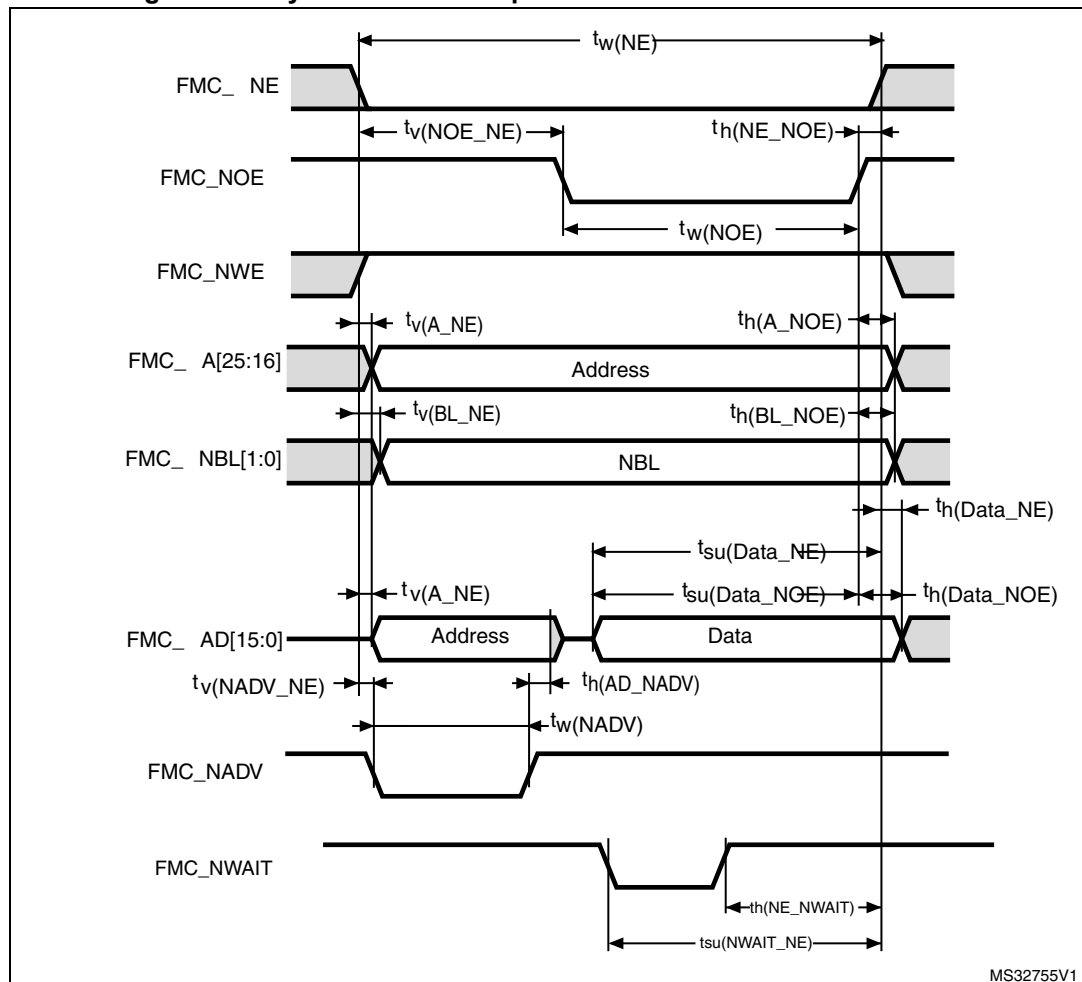


**Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+1$	$8T_{HCLK}+2$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}-1$	$6T_{HCLK}+2$	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$		ns

1.  $C_L = 30$  pF.

2. Guaranteed by characterization results.

**Figure 57. Asynchronous multiplexed PSRAM/NOR read waveforms**

**Table 102. SDRAM read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. CL = 30 pF on data and address lines. CL=15pF on FMC\_SDCLK.

2. Guaranteed by characterization results.

**Table 103. LPSDR SDRAM read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	1	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	1	-	

1. CL = 10 pF.

2. Guaranteed by characterization results.

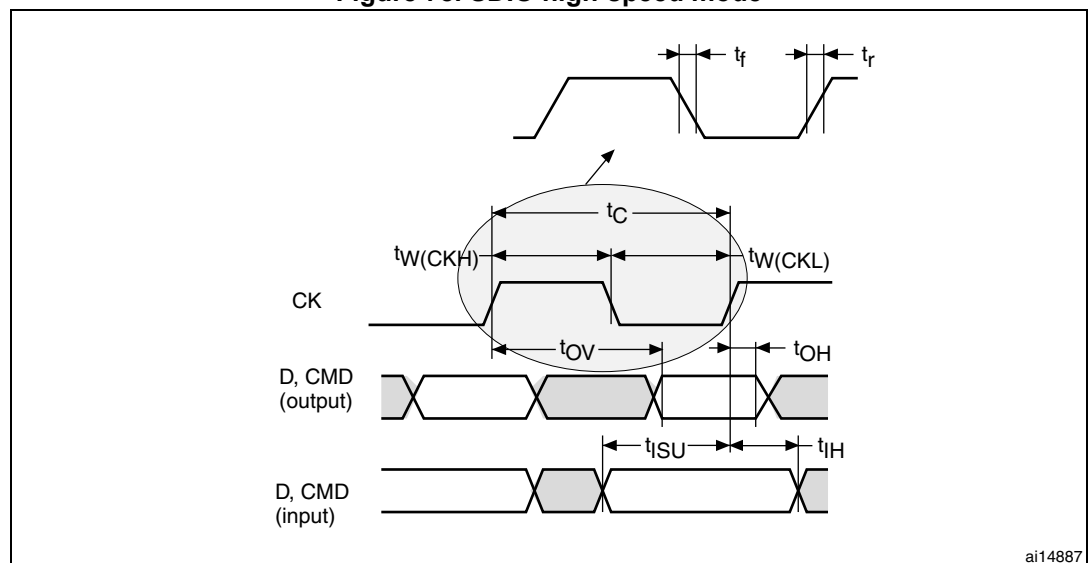
### 6.3.29 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 108](#) for the SDIO/MMC interface are derived from tests performed under the ambient temperature,  $f_{PCLK2}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#), with the following configuration:

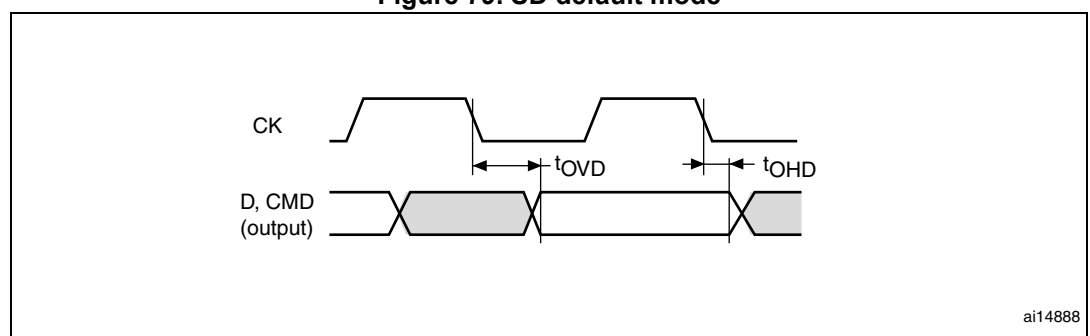
- Output speed is set to  $OSPEEDRy[1:0] = 10$
- Capacitive load  $C = 30$  pF
- Measurement points are done at CMOS levels:  $0.5V_{DD}$

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

**Figure 78. SDIO high-speed mode**



**Figure 79. SD default mode**

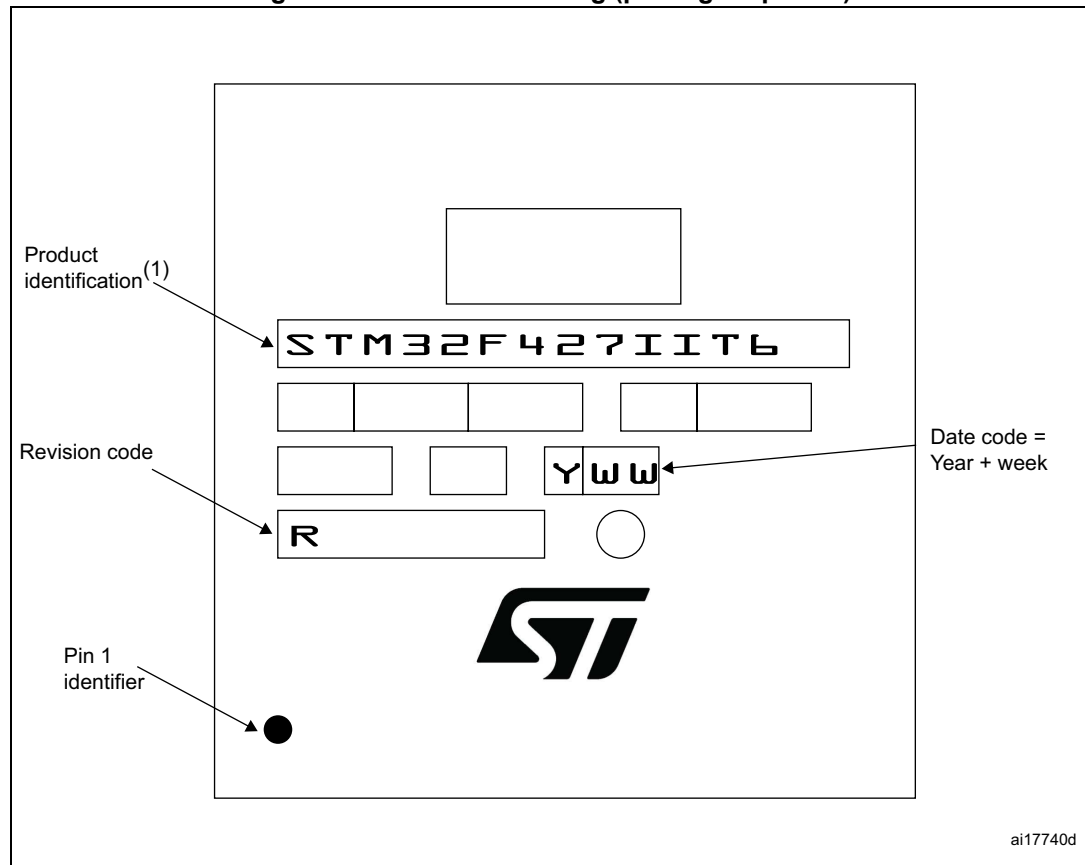


### Device marking for LQFP176

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

**Figure 91. LQFP176 marking (package top view)**



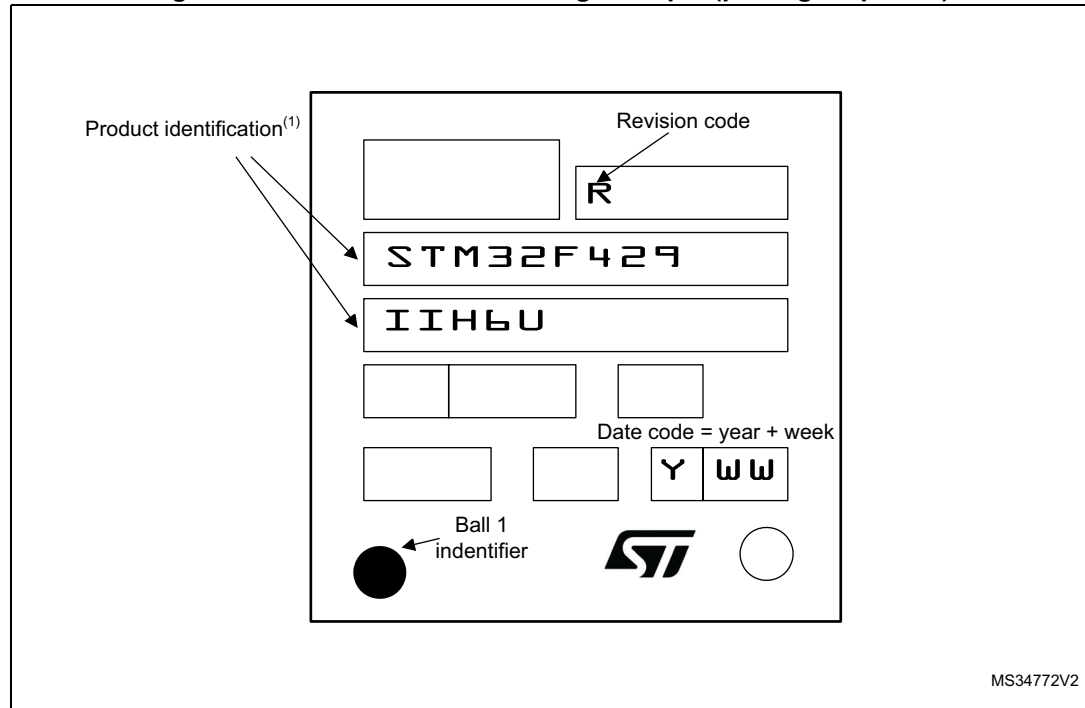
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

### Device marking for UFBGA176+25

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

**Figure 100. UFBGA176+25 marking example (package top view)**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.